FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-29115-2E

Spread Spectrum Clock Generator

MB88154

■ DESCRIPTION

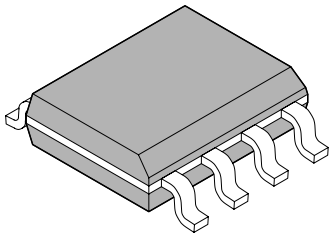
MB88154 is a clock generator for EMI (Electro Magnetic Interference) reduction. The peak of unnecessary radiation noise (EMI) can be attenuated by making the oscillation frequency slightly modulate periodically with the internal modulator. It corresponds to both of the center spread which modulates input frequency as Middle Centered and down spread which modulates so as not to exceed input frequency.

■ FEATURE

- Input frequency : 16.6 MHz to 67 MHz
- Output frequency: 16.6 MHz to 67 MHz (One time input frequency)
- Modulation rate can select from ± 0.5%, ± 1.0%, ± 1.5% or – 1.0%, – 2.0%, – 3.0%. (For center spread / down spread.)
- Equipped with crystal oscillation circuit: Range of oscillation 16.6 M MHz to 48 MHz
- The external clock can be input: 16.6 MHz to 67 MHz
- Modulation clock output Duty : 40% to 60%
- Modulation clock Cycle-Cycle Jitter : Less than 100 ps
- Low current consumption by CMOS process : 5.0 mA (24 MHz : Typ-sample, no load)
- Power supply voltage : 3.3 V ± 0.3 V
- Operating temperature : – 40 °C to +85 °C
- Package : SOP 8-pin

■ PACKAGE

8-pin plastic SOP



(FPT-8P-M02)

FUJITSU

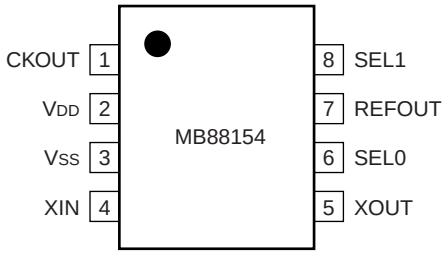
■ PRODUCT LINEUP

MB88154 has two kinds of input frequency, and two kinds of modulation type (center/down spread), total four line-ups.

Product	Input/Output frequency	Modulation type
MB88154-102	33 MHz to 67 MHz	Down
MB88154-103	16.6 MHz to 40 MHz	
MB88154-112	33 MHz to 67 MHz	Center
MB88154-113	16.6 MHz to 40 MHz	

■ PIN ASSIGNMENT

TOP VIEW

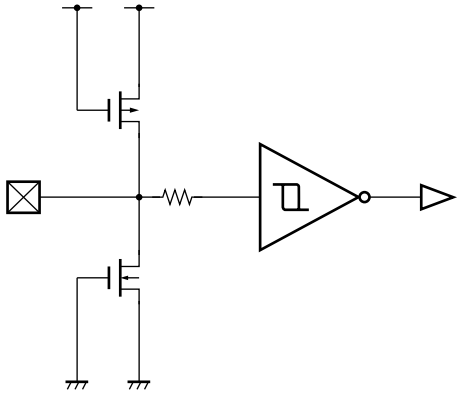
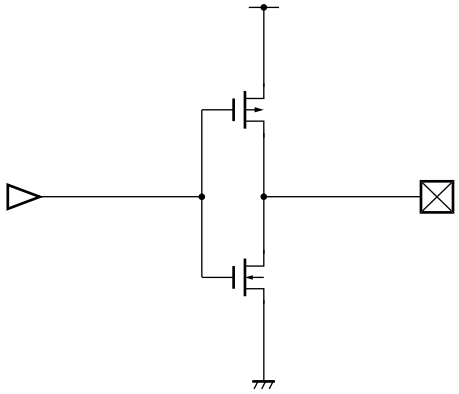


FPT-8P-M02

■ PIN DESCRIPTION

Pin name	I/O	Pin no.	Description
CKOUT	O	1	Modulated clock output pin
V_{DD}	—	2	Power supply voltage pin
V_{SS}	—	3	GND pin
XIN	I	4	Crystal resonator connection pin/clock input pin
XOUT	O	5	Crystal resonator connection pin
SEL0	I	6	Modulation rate setting pin
REFOUT	O	7	Non-modulated clock output pin
SEL1	I	8	Modulation rate setting pin

■ I/O CIRCUIT TYPE

Pin	Circuit type	Remarks
SEL0 SEL1		• CMOS hysteresis input
CKOUT REFOUT		• CMOS output • I_{OL} = 3 mA

Note : For XIN and XOUT pins, see “■OSCILLATION CIRCUIT”

■ HANDLING DEVICES

Preventing Latchup

A latchup can occur if, on this device, (a) a voltage higher than V_{DD} or a voltage lower than V_{SS} is applied to an input or output pin or (b) a voltage higher than the rating is applied between V_{DD} and V_{SS}. The latchup, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use this device, be very careful not to exceed the maximum rating.

Handling unused pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, using a pull-up or pull-down resistor.

Unused output pin should be opened.

The attention when the external clock is used

Input the clock to XIN pin, and XOUT pin should be opened when you use the external clock.

Please pay attention so that an overshoot and an undershoot do not occur to an input clock of XIN pin.

Power supply pins

Please design connecting the power supply pin of this device by as low impedance as possible from the current supply source.

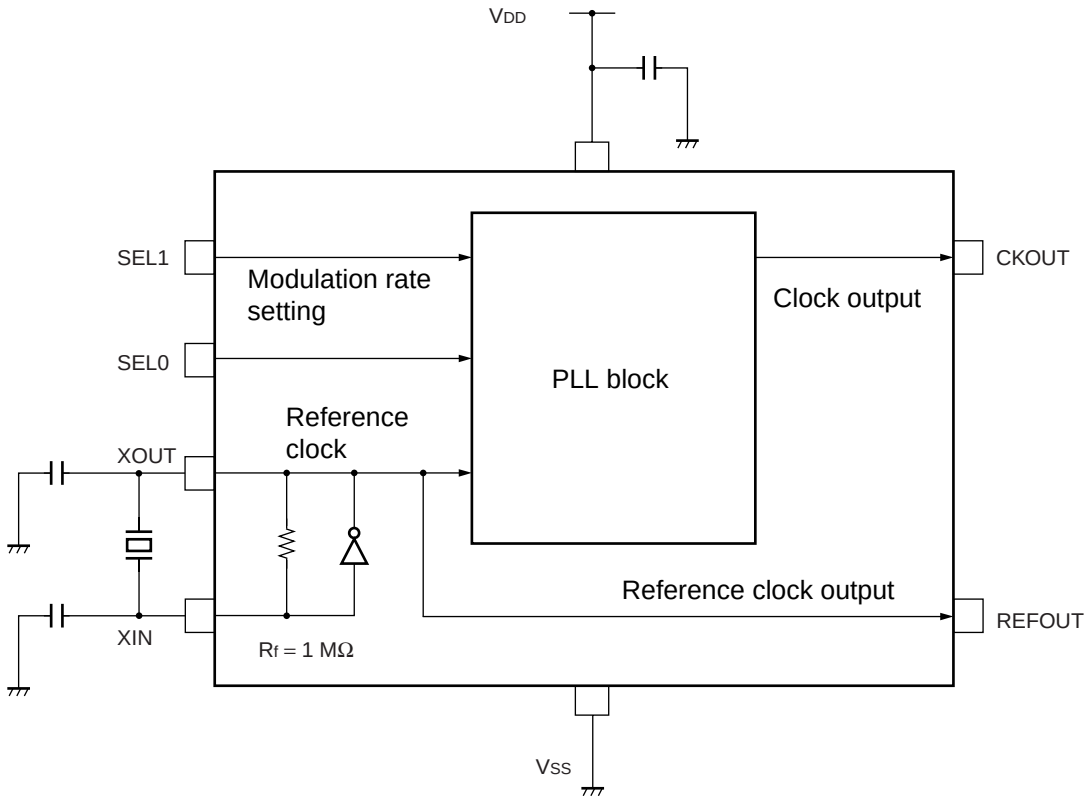
We recommend connecting electrolytic capacitor (about 10 μF) and the ceramic capacitor (about 0.01 μF) in parallel between V_{SS} and V_{DD} near the device, as a bypass capacitor.

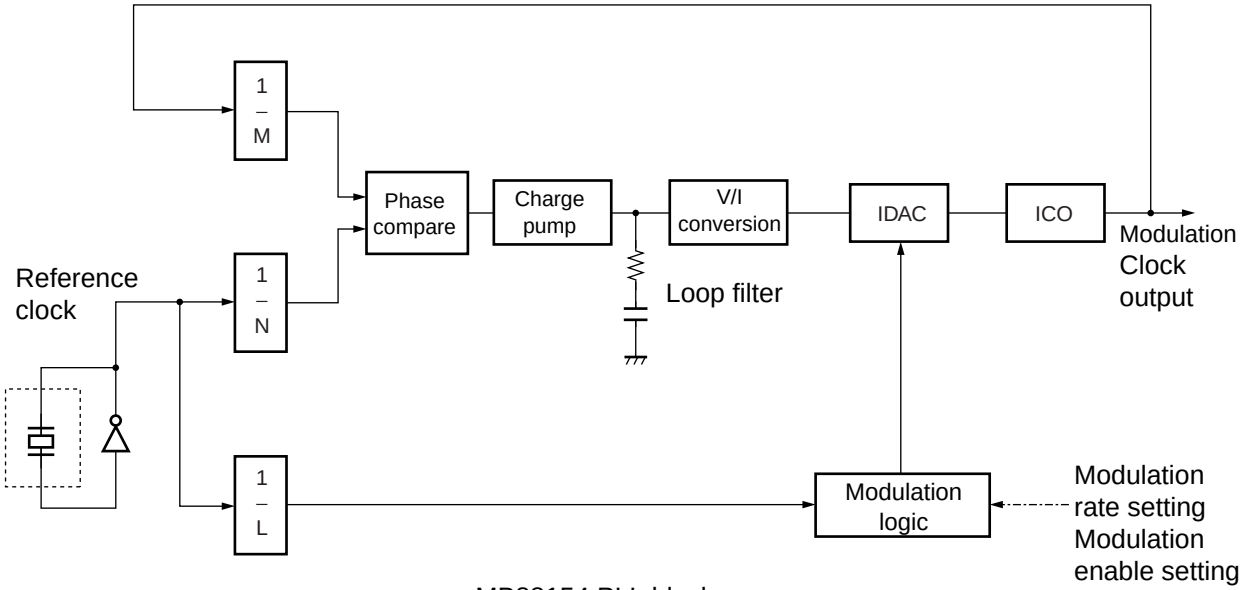
Oscillation circuit

Noise near the XIN and XOUT pins may cause the device to malfunction. Design printed circuit boards so that electric wiring of XIN or XOUT pin and the resonator do not intersect other wiring.

Design the printed circuit board that surrounds the XIN and XOUT pins with ground.

■ BLOCK DIAGRAM





MB88154 PLL block

A glitchless IDAC (current output D/A converter) provides precise modulation, thereby dramatically reducing EMI.

■ PIN SETTING

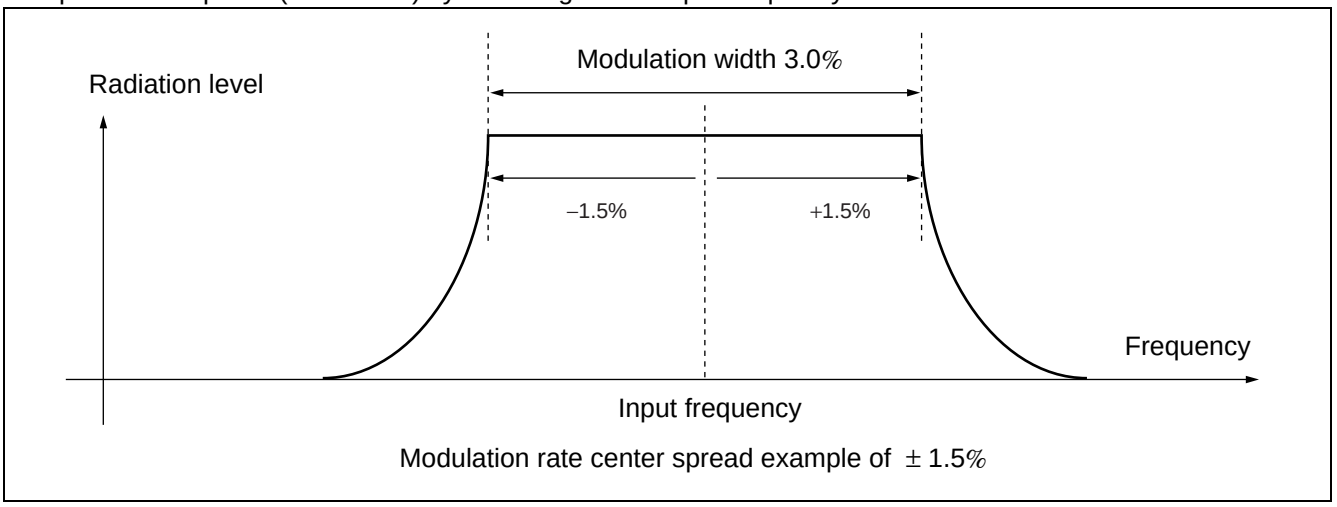
SEL 0, SEL 1 Modulation rate setting

SEL1	SEL0	modulation rate	
		MB88154-102, MB88154-103	MB88154-112, MB88154-113
		Down spread	Center spread
L	L	– 1.0%	± 0.5%
L	H	– 2.0%	± 1.0%
H	L	– 3.0%	± 1.5%
H	H	No spread	No spread

Notes :
- The modulation rate can be changed at the level of the pin. Spectrum does not spread when “H” level is set to SEL0 and SEL1 pin. The clock with low jitter can be obtained.
- When changing the modulation rate setting, the stabilization wait time for the modulation clock is required. The stabilization wait time for the modulation clock take the maximum value of “■ ELECTRICAL CHARACTERISTICS • AC Characteristics Lock-Up time”.

• Center spread

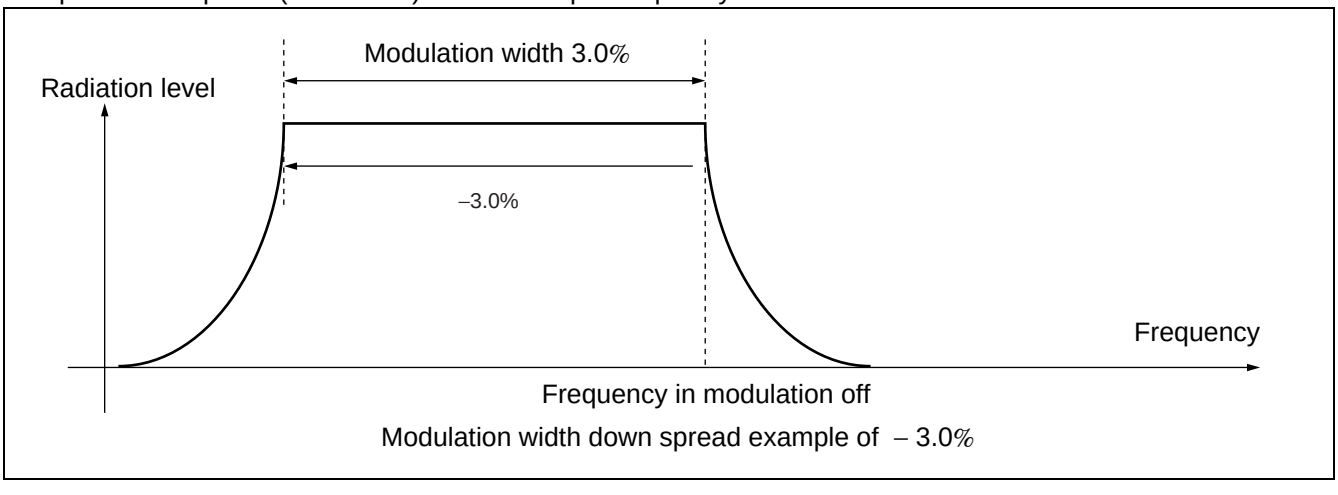
Spectrum is spread (modulated) by centering on the input frequency.



Modulation rate center spread example of ± 1.5%

• Down spread

Spectrum is spread (modulated) below the input frequency.



Modulation width down spread example of – 3.0%

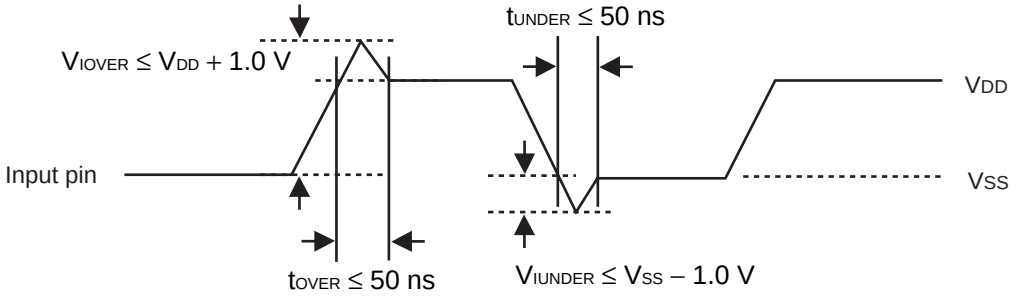
■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	– 0.5	+ 4.0	V
Input voltage*	V_I	V_{SS} – 0.5	V_{DD} + 0.5	V
Output voltage*	V_O	V_{SS} – 0.5	V_{DD} + 0.5	V
Storage temperature	T_{ST}	– 55	+ 125	°C
Operation junction temperature	T_J	– 40	+ 125	°C
Output current	I_O	– 14	+ 14	mA
Overshoot	V_{IOVER}	—	V_{DD} + 1.0 (t_{OVER} ≤ 50 ns)	V
Undershoot	V_{IUNDER}	V_{SS} – 1.0 (t_{UNDER} ≤ 50 ns)	—	V

* : The parameter is based on V_{SS} = 0.0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Overshoot/Undershoot



■ RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0.0 V)

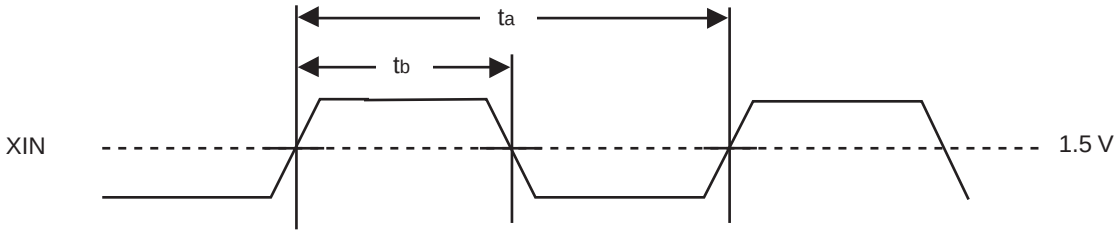
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply voltage	V_{DD}	V_{DD}	—	3.0	3.3	3.6	V
"H" level input voltage	V_{IH}	XIN, SEL0, SEL1	—	$V_{DD} \times 0.80$	—	$V_{DD} + 0.3$	V
"L" level input voltage	V_{IL}		—	V_{SS}	—	$V_{DD} \times 0.20$	V
Input clock duty cycle	t_{DCI}	XIN	16.6 MHz to 67 MHz	40	50	60	%
Operating temperature	Ta	—	—	− 40	—	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

Input clock duty cycle ($t_{DCI} = t_b/t_a$)



■ ELECTRICAL CHARACTERISTICS

• DC Characteristics

($Ta = -40\ °C$ to $+85\ °C$, $V_{DD} = 3.3\ V \pm 0.3\ V$, $V_{SS} = 0.0\ V$)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply current	I_{CC}	V_{DD}	no load capacitance at 24 MHz output	—	5.0	7.0	mA
Output voltage	V_{OH}	CKOUT, REFOUT	"H" level output $I_{OH} = -3$ mA	$V_{DD} - 0.5$	—	V_{DD}	V
	V_{OL}		"L" level output $I_{OL} = 3$ mA	V_{SS}	—	0.4	V
Output impedance	Z_O	CKOUT, REFOUT	16.6 MHz to 67 MHz	—	70	—	Ω
Input capacitance	C_{IN}	XIN, SEL0, SEL1	$Ta = +25\ °C$, $V_{DD} = V_I = 0.0\ V$, $f = 1$ MHz	—	—	16	pF

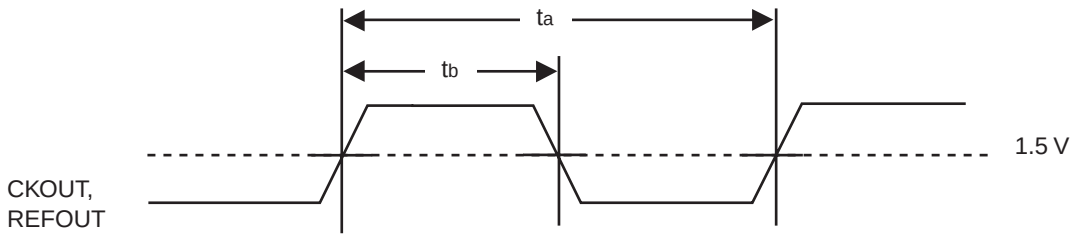
• AC Characteristics

($Ta = -40\ °C$ to $+85\ °C$, $V_{DD} = 3.3\ V \pm 0.3\ V$, $V_{SS} = 0.0\ V$)

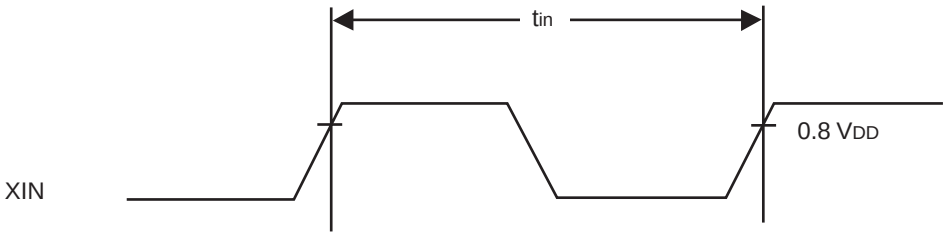
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Oscillation frequency	f_x	XIN, XOUT	Fundamental oscillation	16.6	—	40	MHz
			3rd over-tone oscillation	40	—	48	
Input frequency	f_{in}	XIN	MB88154-103/113	16.6	—	40	MHz
			MB88154-102/112	33	—	67	
Output frequency	f_{OUT}	CKOUT, REFOUT	MB88154-103/113	16.6	—	40	MHz
			MB88154-102/112	33	—	67	
Output slew rate	SR	CKOUT, REFOUT	0.4 V to 2.4 V load capacitance 15 pF	0.3	—	2.0	V/ns
Output clock duty cycle	t_{DCC}	CKOUT	1.5 V	40	—	60	%
	t_{DCR}	REFOUT	1.5 V	$t_{DCI} - 10$*	—	$t_{DCI} + 10$*	%
Modulation frequency	f_{MOD}	CKOUT	—	—	12.5	—	kHz
Lock-Up time	t_{LK}	CKOUT	—	—	2	5	ms
Cycle-cycle jitter	t_{JC}	CKOUT	No load capacitance, $Ta = +25\ °C$, $V_{DD} = 3.3\ V$, Standard deviation σ	—	—	100	ps

* : Duty of the REFOUT output is guaranteed only for the following A and B because it depends on t_{DCI} of input clock duty.
A. Resonator : When resonator is connected with XIN and XOUT and oscillates normally.
B. External clock input : The input level is Full - swing ($V_{SS} - V_{DD}$).

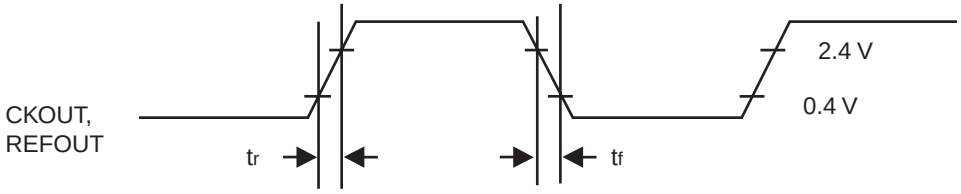
■ OUTPUT CLOCK DUTY CYCLE (t_{DCC}, $t_{DCR} = t_b/t_a$)



■ INPUT FREQUENCY ($f_{in} = 1/t_{in}$)

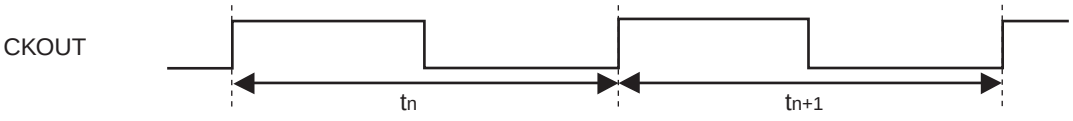


■ OUTPUT SLEW RATE (SR)



Note : SR = (2.4–0.4) /t_r, SR = (2.4–0.4) /t_f

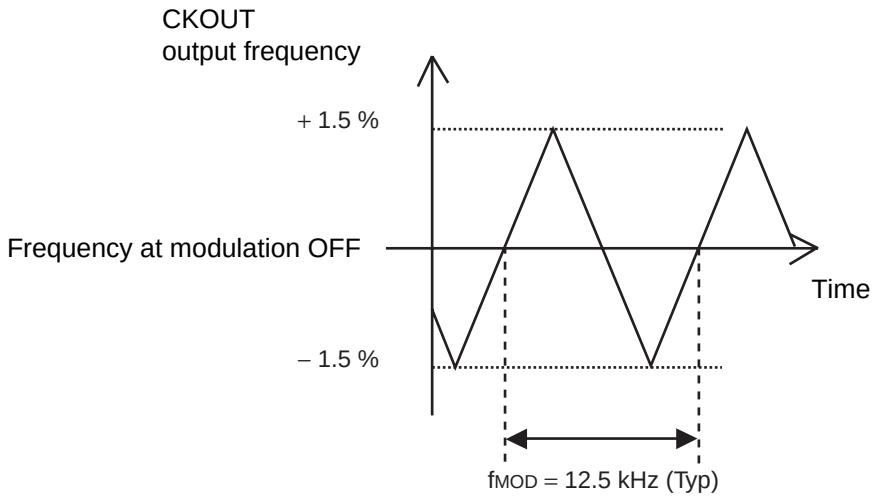
■ CYCLE-CYCLE JITTER ($t_{JC} = | t_n - t_{n+1} |$)



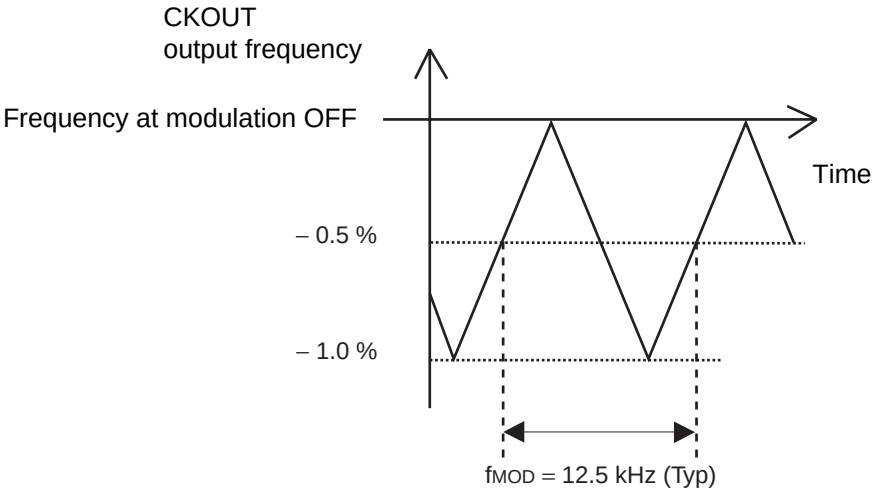
Note : Cycle-cycle jitter is defined the difference between a certain cycle and immediately after (or, immediately before) .

■ MODULATION WAVEFORM

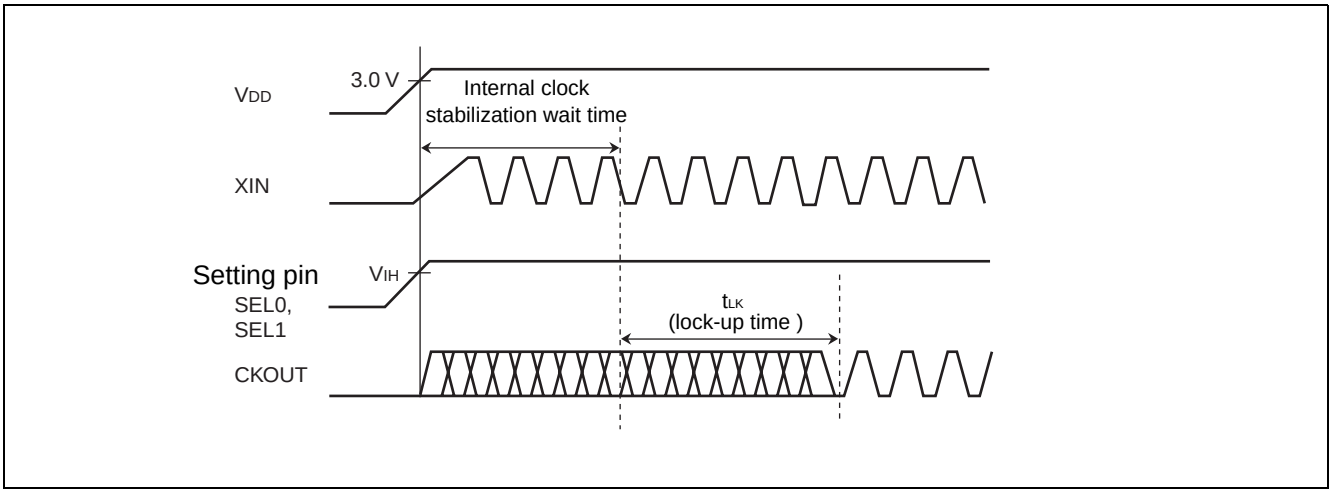
• ±1.5% modulation rate, Example of center spread



• –1.0% modulation rate, Example of down spread



■ LOCK-UP TIME



If the setting pin is fixed at the “H” or “L” level, the maximum time after the power is turned on until the set clock signal is output from CKOUT pin is (the stabilization wait time of input clock to XIN pin) + (the lock-up time “t_{LK}”). For the input clock stabilization time, check the characteristics of the resonator or oscillator used.

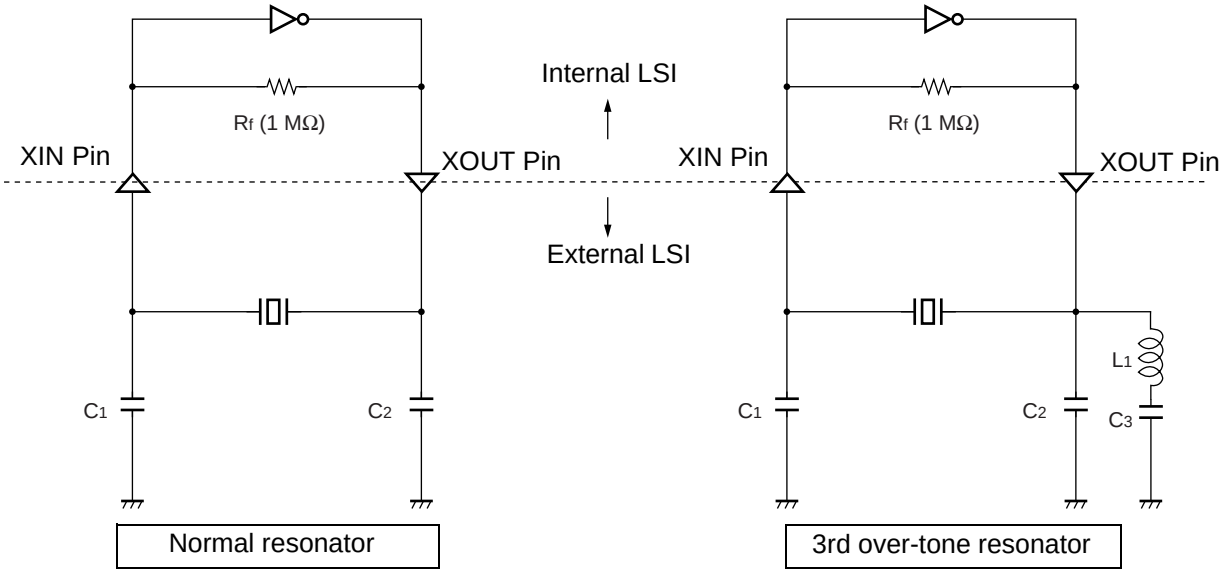
Note : When the pin setting is changed, the CKOUT pin output clock stabilization time is required. Until the output clock signal becomes stable, the output frequency, output clock duty cycle, modulation period, and cycle-cycle jitter cannot be guaranteed. It is therefore advisable to perform processing such as cancelling a reset of the device at the succeeding stage after the lock-up time.

■ OSCILLATION CIRCUIT

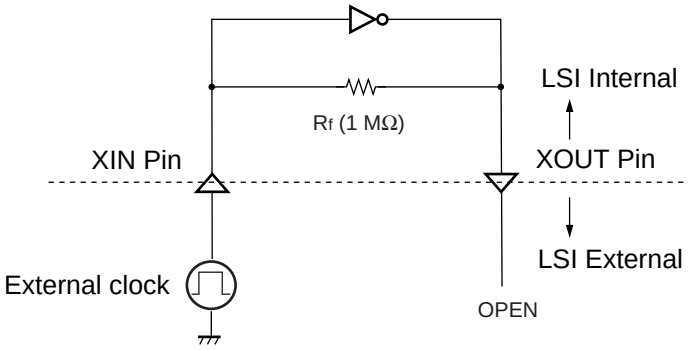
The left side of figures below shows the connection example about general resonator. The oscillation circuit has the built-in feedback resistance (1 MΩ) . The value of capacity (C_1 and C_2) is required adjusting to the most suitable value of an individual resonator.

The right side of figures below shows the example of connecting for the 3rd over-tone resonator. The value of capacity (C_1, C_2 and C_3) and inductance (L_1) is needed adjusting to the most suitable value of an individual resonator. The most suitable value is different by individual resonator. Please refer to the resonator manufacturer which use for the most suitable value. When an external clock is used (the resonator is not used) , input the clock to XIN pin and do not connect anything with XOUT.

• When using a resonator

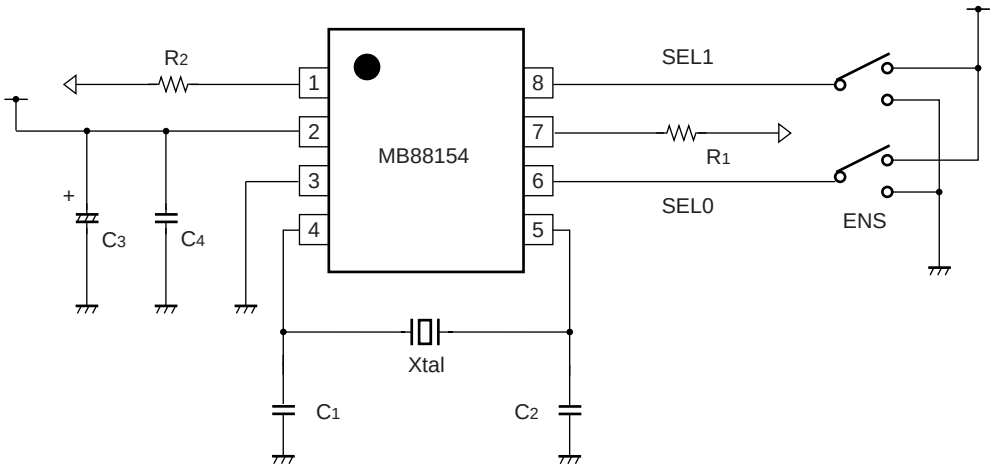


• When using an external clock



Note : Note that a jitter characteristic of an input clock may cause an affect a cycle-cycle jitter characteristic.

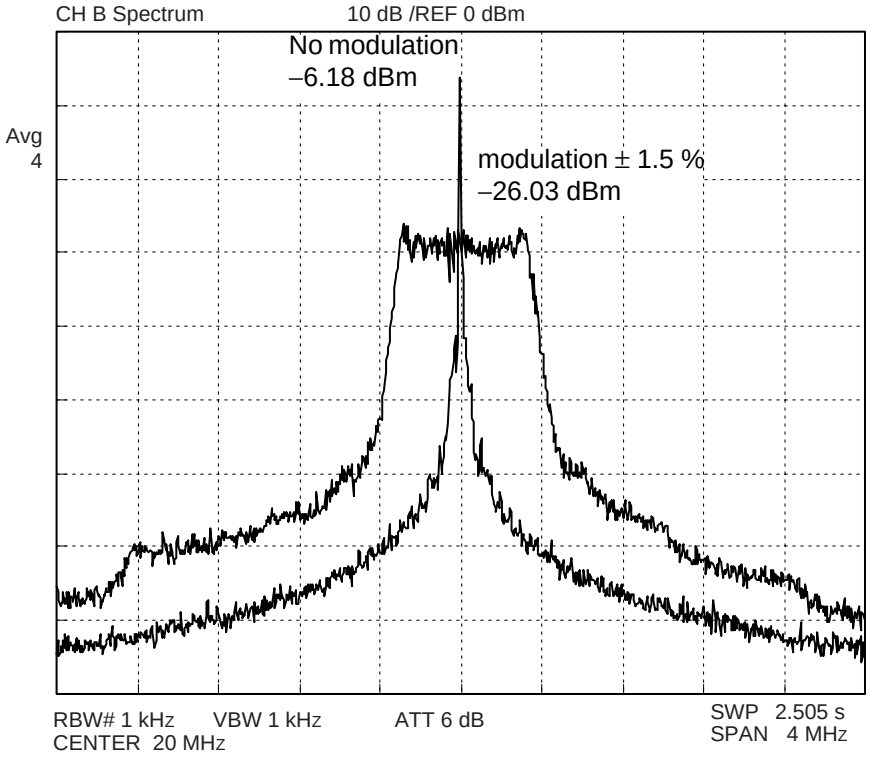
■ INTERCONNECTION CIRCUIT EXAMPLE



C_1, C_2	: Oscillation stabilization capacitance (see "■OSCILLATION CIRCUIT".)
C_3	: Capacitor of 10 μF or higher
C_4	: Capacitor about 0.01 μF (connect a capacitor of good high frequency property (ex. laminated ceramic capacitor) to close to this device.)
R_1, R_2	: Impedance matching resistor for board pattern

■ EXAMPLE CHARACTERISTICS

The condition of the examples of the characteristic is shown as follows: Input frequency = 20 MHz (Output frequency = 20 MHz : Using MB88154-113), Power - supply voltage = 3.3 V, None load capacity.
Modulation rate = ± 1.5% (center spread)
Spectrum analyzer HP4396B is connected with CKOUT. The result of the measurement with RBW = 1 kHz (ATT use for – 6dB).



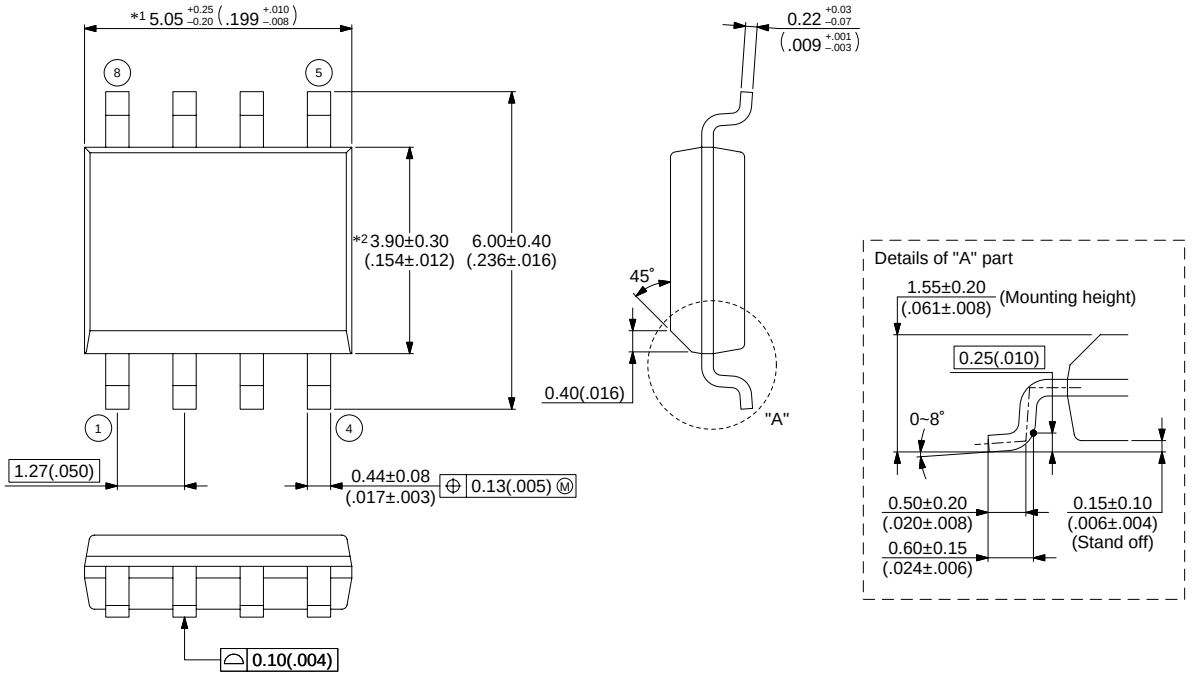
■ ORDERING INFORMATION

Part number	Input/Output frequency	Modulation type	Package	Remarks
MB88154PNF-G-102-JNE1	33 MHz to 67 MHz	Down	8-pin plastic SOP (FPT-8P-M02)	
MB88154PNF-G-103-JNE1	16.6 MHz to 40 MHz	Down		
MB88154PNF-G-112-JNE1	33 MHz to 67 MHz	Center		
MB88154PNF-G-113-JNE1	16.6 MHz to 40 MHz	Center		
MB88154PNF-G-102-JN-EFE1	33 MHz to 67 MHz	Down	8-pin plastic SOP (FPT-8P-M02)	Emboss taping (EF type)
MB88154PNF-G-103-JN-EFE1	16.6 MHz to 40 MHz	Down		
MB88154PNF-G-112-JN-EFE1	33 MHz to 67 MHz	Center		
MB88154PNF-G-113-JN-EFE1	16.6 MHz to 40 MHz	Center		
MB88154PNF-G-102-JN-ERE1	33 MHz to 67 MHz	Down	8-pin plastic SOP (FPT-8P-M02)	Emboss taping (ER type)
MB88154PNF-G-103-JN-ERE1	16.6 MHz to 40 MHz	Down		
MB88154PNF-G-112-JN-ERE1	33 MHz to 67 MHz	Center		
MB88154PNF-G-113-JN-ERE1	16.6 MHz to 40 MHz	Center		

■ PACKAGE DIMENSION

8-pin plastic SOP
(FPT-8P-M02)

Note 1) *1 : These dimensions include resin protrusion.
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches)
Note : The values in parentheses are reference values.

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