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Edition 3.0

FUJITSU

DATA SHEET

MB87073
CMOS PLL FREQUENCY SYNTHESIZER

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CMOS SERIAL INPUT PHASE-LOCKED-LOOP (PLL) FREQUENCY SYNTHESIZER

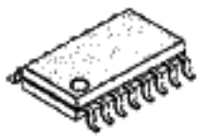
The Fujitsu MB87073, fabricated in advanced CMOS technology, is a serial input PLL frequency synthesizer.

The MB87073 contains an inverter for oscillator, a programmable reference divider, a divide factor of programmable reference divider control circuit, a phase detector, a charge pump, a 18-bit shift register, a 18-bit latch, a programmable divider (a binary 7-bit swallow counter, a binary 11-bit programmable counter), and a control generator for an external dual modulus prescaler.

When supplemented with a loop filter and VCO, the MB87073 contains the necessary circuit to make up PLL frequency synthesizer. Typically, a dual modulus prescaler such as the MB501L can be added, allowing input frequency operation up to 1.1GHz.

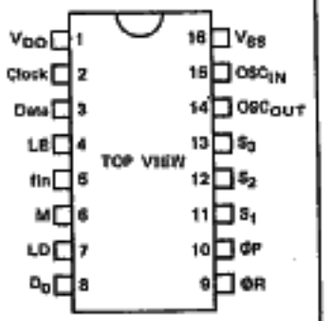
- Single power supply voltage:
  V_{DD} = 2.7 to 5.5V
- Wide temperature range:
  T_A = −40 to 85°C
- 13MHz typical input capability @5V (f_{in} input)
- On-chip inverter for oscillator
- 8 divide factors for programmable reference divider is selected by S_1, S_2 and S_3 input (1/8, 1/16, 1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048)
- Programmable 18-bit divider with input amplifier consisting of:
  Binary 7-bit swallow counter
  Binary 11-bit programmable counter
- 2 type of phase detector output
  On-chip charge pump output
  Output for external charge pump
- Easy interface to Fujitsu dual modulus prescaler

PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M02

PIN ASSIGNMENT



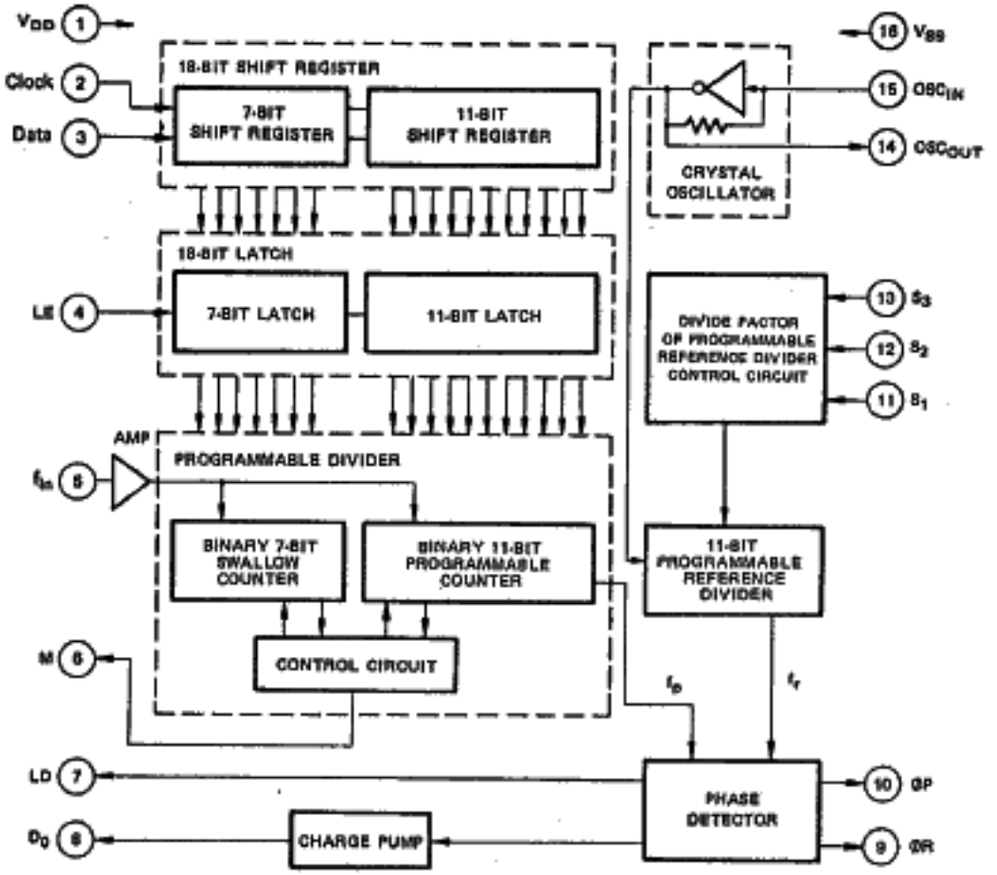
ABSOLUTE MAXIMUM RATING (See NOTE) (V_{SS} = 0V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS}−0.5 to V_{SS}+7.0	V
Input Voltage	V_{IN}	V_{SS}−0.5 to V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}−0.5 to V_{DD}+0.5	V
Output Current	I_{OUT}	±10	mA
Open-drain Output	V_{OOP}	V_{SS}−0.5 to V_{DD}+3.0	V
Operating Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB87073 BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	V_{DD}	—	Power supply voltage input.
2	Clock	I	Clock signal input for 18-bit shift register. Each rising edge of the clock shifts one bit of the data into the shifter register.
3	Data	I	Serial data input for 18-bit shift register. This data is used for setting the divide factor of programmable divider.
4	LE	I	Load enable input. When this pin is high level (high active), the data stored in the 18-bit shift register is transferred to 18-bit latch.
5	f_{in}	I	Input for programmable divider from VCO or prescaler output. This input involves bias circuit and amplifier. The connection with external dual modulus prescaler should be an AC connection.
6	M	O	Control output for external dual modulus prescaler. The connection to the prescaler should be DC connection. This output level is synchronized with falling edge of fin input signal (pin #5). Pulse Swallow Function: MB501L M = High: Preset modulus factor 64 or 128 M = Low: Preset modulus factor 65 or 129
7	LD	O	Output of phase detector. It is high level when f_r and f_p are equal, and then the loop is locked. Otherwise it outputs negative pulse signal.
8	D_O	O	Three-state charge pump output of the phase detector. The mode of D_O is changed by the combination of programmable reference divider output frequency f_r and programmable divider output frequency f_p as listed below: $f_r > f_p$: Drive mode (D_O = High level) $f_r = f_p$: High-impedance mode $f_r < f_p$: Sink mode (D_O = Low level)
9 10	ØR ØP	O O	Phase detector outputs for an external charge pump. The mode of ØR and ØP are changed by the combination of programmable reference divider output frequency f_r and programmable divider output frequency f_p as listed below: ØR ØP $f_r > f_p$: Low : Low $f_r = f_p$: Low : High-Impedance $f_r < f_p$: High : High-Impedance *ØP is a N-channel open drain output.

PIN DESCRIPTION (continued)

Pin No.	Symbol	I/O	Description
11 12 13	S_1 S_2 S_3	I I I	Control input for programmable reference divider. The combination of these inputs provides 8 kinds of divide factor for the programmable reference divider.
14	OSC_{OUT}	O	Output pin for crystal oscillator. Output of the inverting amplifier. This pin should be open when an external oscillator is used.
15	OSC_{IN}	I	Input pin for crystal oscillator. Input to the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as AC coupled when an external oscillator is used. For large amplitude signals (standard CMOS levels) DC coupling may also be used.
16	V_{SS}	—	Ground

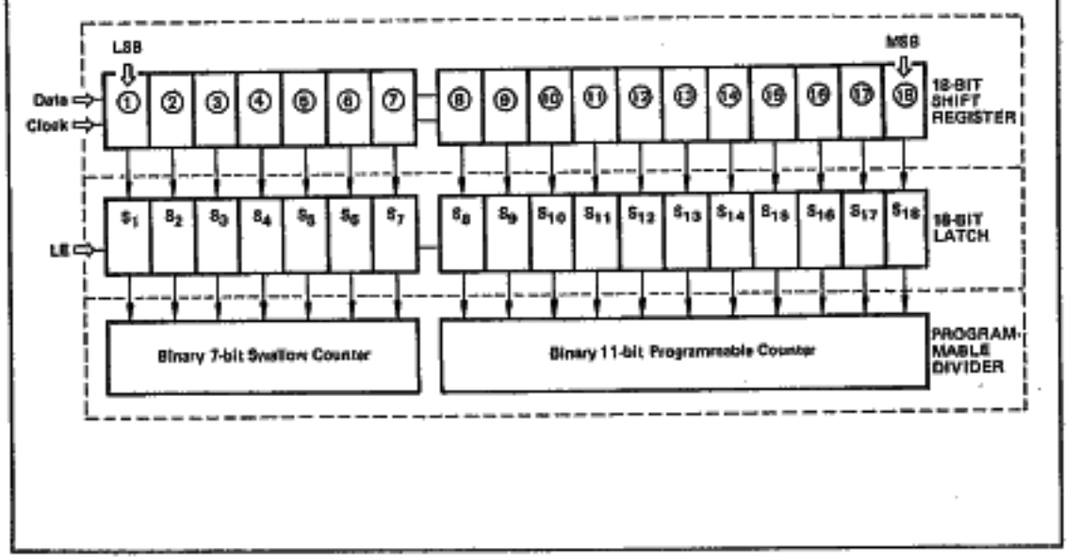
Divide Factor / Sn	1/8	1/16	1/64	1/128	1/256	1/512	1/1024	1/2048
S_1	0	1	0	1	0	1	0	1
S_2	0	0	1	1	0	0	1	1
S_3	0	0	0	0	1	1	1	1

FUNCTIONAL DESCRIPTION

DIVIDE FACTOR OF PROGRAMMABLE DIVIDER

Serial data of binary code is input to Data pin. These data are loaded into the 18-bit shift register from MSB. When load enable signal LE is high, the data stored in the 18-bit shift register is transferred to the 18-bit latch.
The data ① to ⑦ set a divide factor of the binary 7-bit swallow counter and data ⑧ to ⑱ set a divide factor of binary 11-bit programmable counter. In other words, serial data is equivalent to the divide factor of programmable divider.

Fig. 2 – BLOCK DIAGRAM OF PROGRAMMABLE DIVIDER



Binary 7-bit Swallow Counter Data Input

⑦	⑥	⑤	④	③	②	①	Divide Factor A
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	127

Note: Devide factor A: 0 to 127
Depending upon the divide factor set input (SW) of external prescaler, the input data should be as follows.
Example MB501L
SW = H (64/65) : Bit 7 of shift register (7) should be zero.

Binary 11-bit Programmable Counter Data Input

⑱	⑰	⑯	⑮	⑭	⑬	⑫	⑪	⑩	⑨	⑧	Divide Factor N
0	0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	0	0	1	1	0	6
0	0	0	0	0	0	0	0	1	1	1	7
•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	1	1	1	2047

Note: Divide factor less than 5 is prohibited.
Divide factor N: 5 to 2047

PULSE SWALLOW FUNCTION

$$f_{VCO} = [(N \times M) + A] \times f_r \quad (A < N)$$

f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
N : Preset divide factor of binary 11-bit programmable counter (5 to 2047)
M : Preset modulus factor of external dual modulus prescaler (e.g. 64 in 64/65 mode, 128 in 128/129 mode of an MB501L prescaler)
A : Preset divide factor of binary 7-bit swallow counter (0 to 127)
f_r : Output frequency of the programmable reference divider

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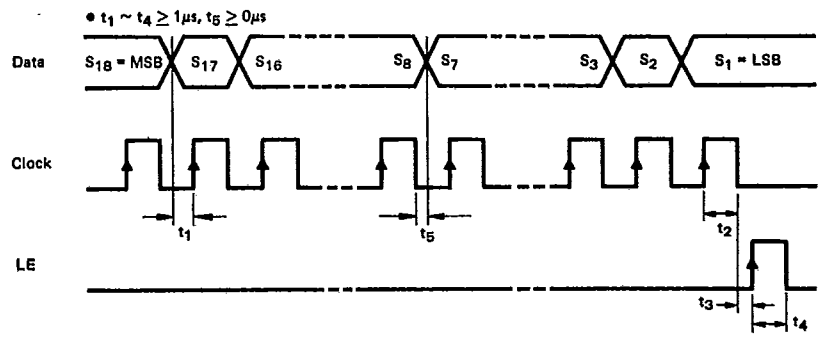
TIMING CHART



Clock: Clock signal input for the 18-bit shift register.
Each rising edge of the clock shifts one bit of data into the shift register.
Data : Serial data for the 18-bit shift register is input.
LE : Load enable input.
When LE is high (high active), the data stored in the 18-bit shift register is transferred to the 18-bit latch.
The 18-bit data is used for setting a divide factor of the programmable divider.

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	2.7		5.5	V
Input Voltage	V_{IN}	V_{SS}		V_{DD}	V
Operating Temperature	T_A	-40		+85	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V, V_{SS} = 0V, T_A = −40 to 85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}		2.1			V
Low-level Input Voltage		V_{IL}				0.9	
Input Sensitivity	f_{in}	V_{fpp}	Amplitude in AC coupling, sine wave	0.8			V_{P-P}
	OSC_{IN}	V_{sin}		1.0			
High-level Input Current	Except f_{in} and OSC_{IN}	I_{IH}	$V_{IN} = V_{DD}$		1.0		μA
Low-level Input Current		I_{IL}	$V_{IN} = V_{SS}$		−1.0		
Input Current	f_{in}	I_{fin}	$V_{IN} = V_{SS}$ to V_{DD}		±30		μA
	OSC_{IN}	I_{OSC}	$V_{IN} = V_{SS}$ to V_{DD}		±30		
High-level Output Voltage	Except ØP and OSC_{OUT}	V_{OH}	I_{OH} = 0μA	2.95			V
Low-level Output Voltage		V_{OL}	I_{OL} = 0μA			0.05	
Low-level Output Voltage	ØP	V_{OLP}	I_{OL} = 0.8mA			0.8	V
High-level Output Voltage	OSC_{OUT}	V_{OHX}	I_{OH} = 0μA	2.50			
Low-level Output Voltage		V_{OLX}	I_{OL} = 0μA			0.50	
High-level Output Current	Except ØP and OSC_{OUT}	I_{OH}	V_{OH} = 2.0V	−0.5			mA
Low-level Output Current		I_{OL}	V_{OL} = 0.8V	0.5			
N-channel Open Drain Cut Off Current	ØP	I_{OFF}	$V_O = V_{DD}$ + 3.0		1.0		μA
Power Supply Current*1		I_{DD}			2.0		mA
Max. Operating Frequency of Programmable Reference Divider		f_{maxd}		13	20		MHz
Max. Operating Frequency of Programmable Divider		f_{maxp}		10	20		MHz

Note: *1 f_{in} = 5.0MHz, 12.8MHz Crystal is connected between OSC_{IN} and OSC_{OUT}.
Inputs are connected to ground except for f_{in} and OSC_{IN}. Outputs are open.

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5.0V, V_{SS} = 0V, T_A = −40 to 85°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
High level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}		3.5			V
Low-level Input Voltage		V_{IL}				1.5	
Input Sensitivity	f_{in}	V_{fpp}	Amplitude in AC coupling, sine wave	1.0			V_{P-P}
	OSC_{IN}	V_{sin}		1.5			
High-level Input Current	Except f_{in} and OSC_{IN}	I_{IH}	$V_{IN} = V_{DD}$		1.0		μA
Low-level Input Current		I_{IL}	$V_{IN} = V_{SS}$		−1.0		
Input Current	f_{in}	I_{fin}	$V_{IN} = V_{SS}$ to V_{DD}		±50		μA
	OSC_{IN}	I_{OSC}	$V_{IN} = V_{SS}$ to V_{DD}		±50		
High-level Output Voltage	Except ØP and OSC_{OUT}	V_{OH}	I_{OH} = 0μA	4.95			V
Low-level Output Voltage		V_{OL}	I_{OL} = 0μA			0.05	
Low-level Output Voltage	ØP	V_{OLP}	I_{OL} = 2mA			1.0	V
High-level Output Voltage	OSC_{OUT}	V_{OHX}	I_{OH} = 0μA	4.50			
Low-level Output Voltage		V_{OLX}	I_{OL} = 0μA			0.50	
High-level Output Current	Except ØP and OSC_{OUT}	I_{OH}	V_{OH} = 4.0V	−1.0			mA
Low-level Output Current		I_{OL}	V_{OL} = 0.8V	1.0			
N-channel Open Drain Cut Off Current	ØP	I_{OFF}	$V_O = V_{DD}$ + 3.0		1.0		μA
Power Supply Current*1		I_{DD}			3.0		mA
Max. Operating Frequency of Programmable Reference Divider		f_{maxd}		15	25		MHz
Max. Operating Frequency of Programmable Divider		f_{maxp}		13	25		MHz

Note: *1 f_{in} = 5.0MHz, 12.8MHz Crystal is connected between OSC_{IN} and OSC_{OUT}.
Inputs are connected to ground except for f_{in} and OSC_{OUT}. Outputs are open.

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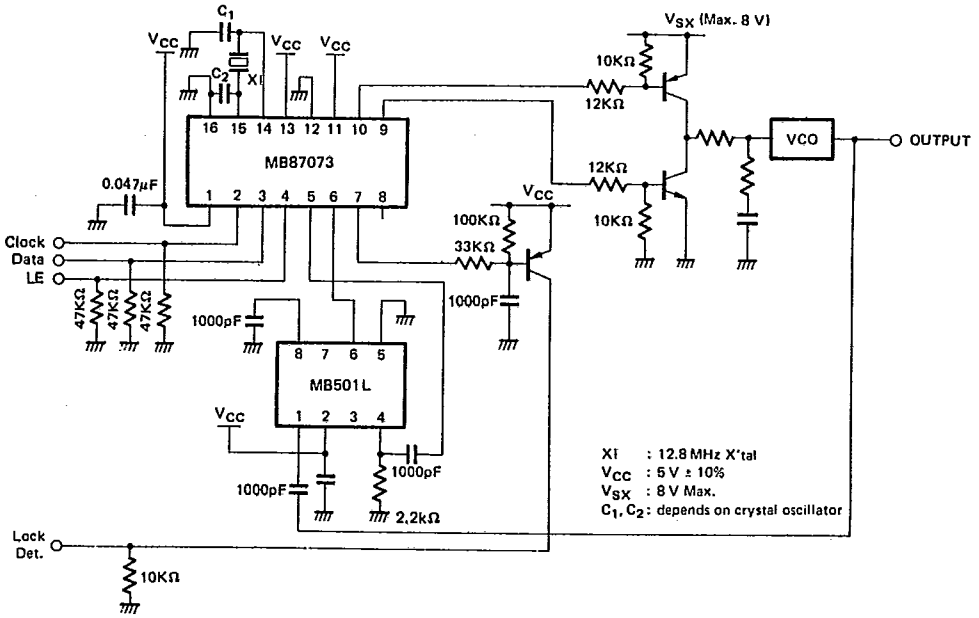
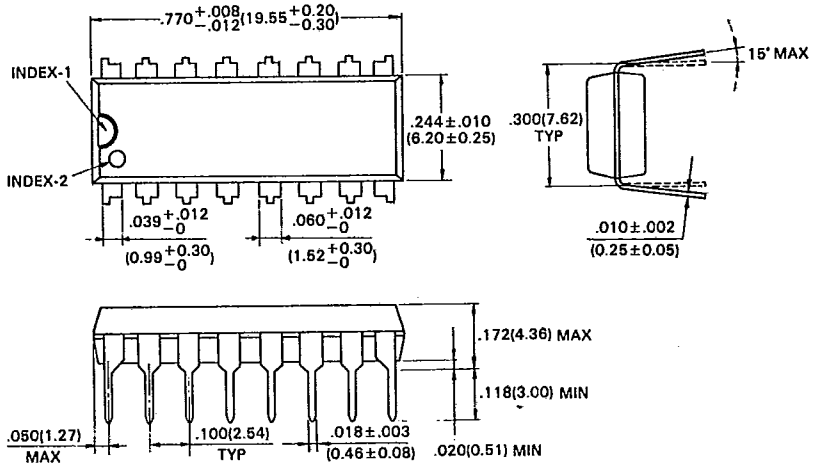
Fig. 3 – TYPICAL APPLICATION EXAMPLE



PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



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Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

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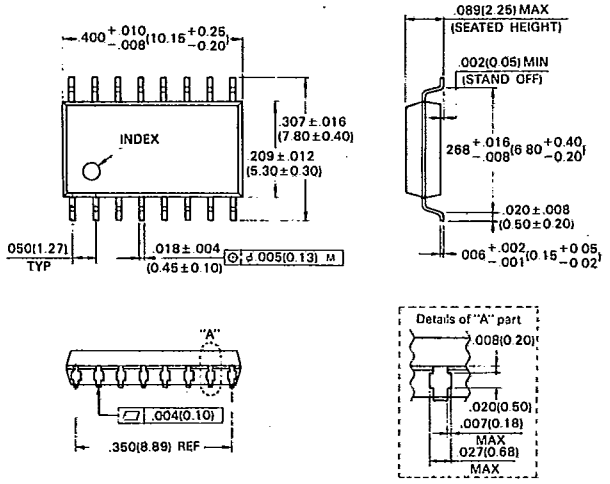
16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



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Dimensions in inches (millimeters)