

ASSP

3-Channel 10-Bit D/A Converter

MB40950

■ DESCRIPTION

The MB40950 is a 10-bit resolution high-speed digital-to-analog converter, designed for video processing applications such as TVsets and VCRs.

The MB40950 has 10-bit resolution 3 channels D/A converters. Digital data are input to the 10-bit digital input ports, and the input digital data are converted into the analog data in minimum 60 Mega sample per seconds (MSPS). The analog output voltage is provided in a range of DC +3V to +5V (2Vp-p level) .

The MB40950 is fabricated by the Fujitsu's advanced bipolar process and housed in a 48-pin plastic QFP.

The MB40950 is designed for video signal processing, and it is suitable for TVs and VCRs applications.

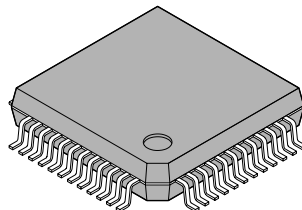
■ FEATURES

- 10-bit x 3 channels D/A converters
- Max. 60 MHz input clock frequency providing 60 MSPS data conversion rate
- Linearity error : Max. +/-0.07%
- Analog output voltage range : 3V to 5V (2Vp-p level)
- Digital input voltage level : TTL level
- On-chip reference voltage generator

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■ PACKAGE

48 pin, Plastic QFP



(FPT-48P-M15)

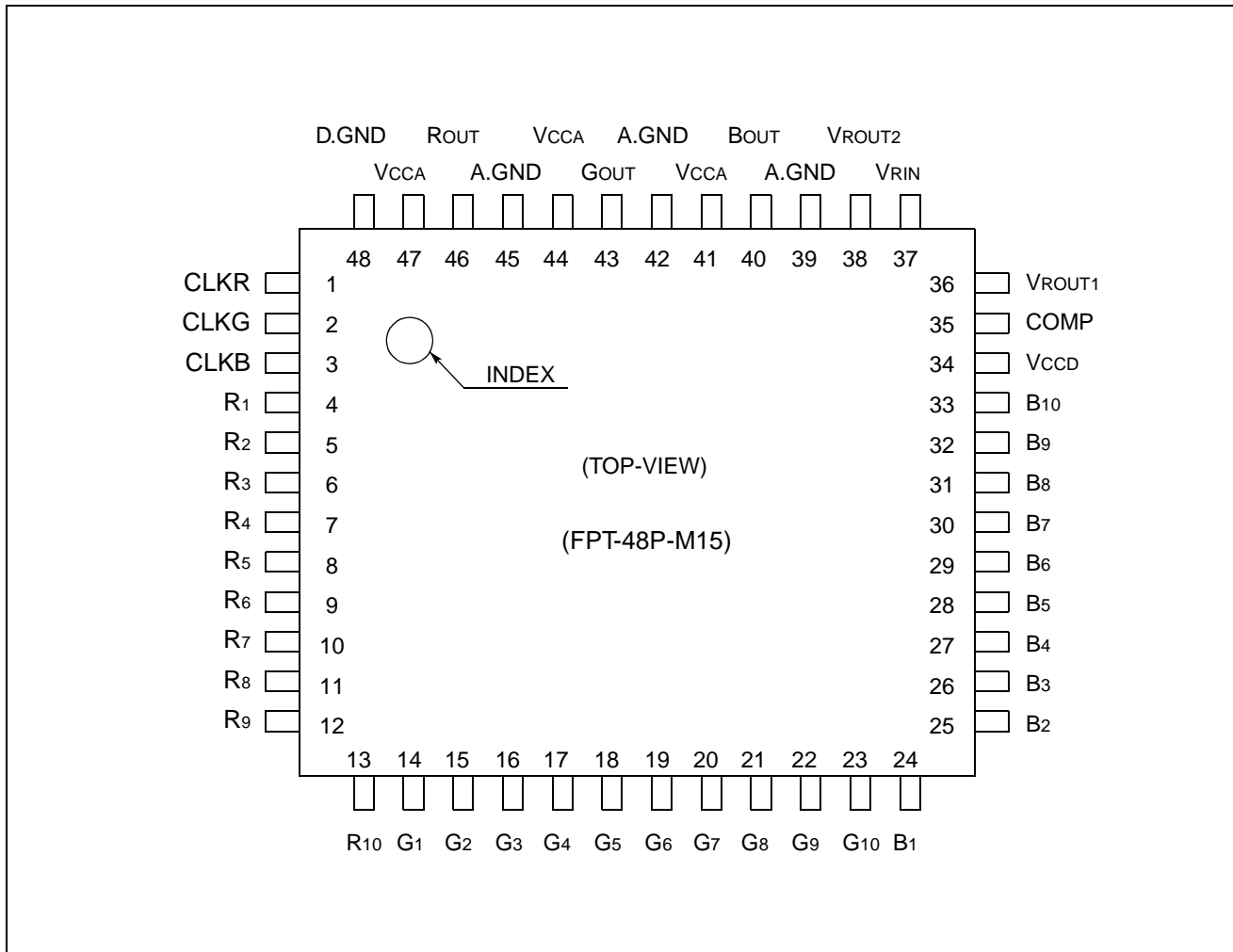
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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- Low power consumption :
 - Typical 460mW at 2Vp-p analog output voltage
 - Typical 350mW at 1Vp-p analog output voltage
- Single +5V power supply
- Operating temperature range : -20°C to +70°C
- Fujitsu's advanced bipolar process
- Package : 48-pin plastic QFP (Suffix : -PF)

■ PIN ASSIGNMENT



■ PIN DESCRIPTION

| Symbol | Pin No. | Type | Name & Function |
|---|--|------|--|
| Power Supply | | | |
| VCCD | 34 | — | +5V DC power supply pins for digital block. |
| D. GND | 48 | — | Ground pin for digital block. |
| VCCA | 41, 44, 47 | — | DC power supply pins for analog block. |
| A. GND | 39, 42, 45 | — | Ground pins for analog block. |
| Clock | | | |
| CLKR | 1 | I | Clock input pin for R channel. |
| CLKG | 2 | I | Clock input pin for G channel. |
| CLKB | 3 | I | Clock input pin for B channel. |
| Digital Input | | | |
| R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 | 4 5 6 7 8 9 10 11 12 13 | I | Digital data input pins for R channel. 10-bit data is input to the pins. The R ₁ pin is the MSB and the R ₁₀ pin is the LSB. |
| G1 G2 G3 G4 G5 G6 G7 G8 G9 G10 | 14 15 16 17 18 19 20 21 22 23 | I | Digital data input pins for G channel. 10-bit data is input to the pins. The G ₁ pin is the MSB and the G ₁₀ pin is the LSB. |
| B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 | 24 25 26 27 28 29 30 31 32 33 | I | Digital data input pins for B channel. 10-bit data is input to the pins. The B ₁ pin is the MSB and the B ₁₀ pin is the LSB. |

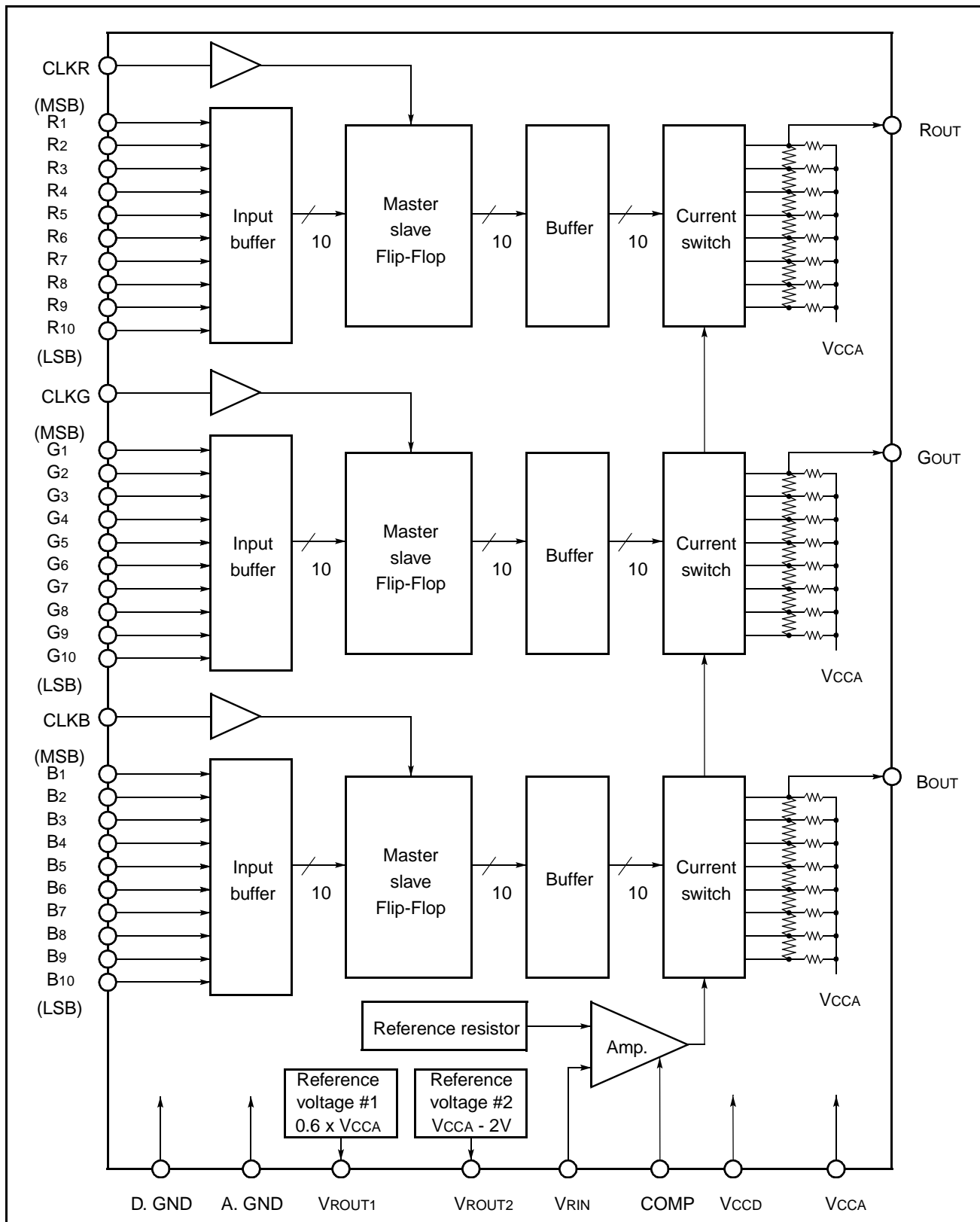
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| Symbol | Pin No. | Type | Name & Function |
|-------------------------------|---------|------|---|
| Analog Output | | | |
| ROUT | 46 | O | Analog signal output pin for R channel. |
| GOUT | 43 | O | Analog signal output pin for G channel. |
| BOUT | 40 | O | Analog signal output pin for B channel. |
| Reference Voltage | | | |
| VRIN | 37 | I | Reference voltage input pin. This pin is used to set the analog output dynamic range. When the internal reference voltage is used, this pin is connected with VROUT1 pin (36 pin) or VROUT2 pin (38 pin). When the reference voltage is supplied from the external generator, 2.65V to 4.3V or $V_{CCA} - V_{RIN} = 0.7V$ to 2.2V is input to this pin. |
| VROUT1 | 36 | O | Reference voltage output #1 pin. The output voltage is set to $0.6 \times V_{CCA}$ by the resistor divided method. When this pin is connected with VRIN pin (37 pin), an analog voltage is output from this pin in a range of $0.6 \times V_{CCA}$ to V_{CCA} . |
| VROUT2 | 38 | O | Reference voltage output #2 pin. The output voltage is set to $V_{CCA} - 2V$ by the band-gap reference method. When this pin is connected with VRIN pin (37 pin), an analog voltage is output from this pin in a range of $V_{CCA} - 2V$ to V_{CCA} . |
| Compensation Capacitor | | | |
| COMP | 35 | - | Phase compensation capacitor pin. A phase compensation capacitor of $0.1\mu F$ or greater is connected between this pin and A. GND pin. |

■ BLOCK DIAGRAM



MB40950

■ ABSOLUTE MAXIMUM RATINGS

(A. GND = D. GND = 0V)

| Parameter | Symbol | Rating | Unit |
|---------------------------------|---------------------|-------------------------|------|
| Power supply voltage | V_{CCA}, V_{CCD} | -0.5 to +7.0 | V |
| Power supply voltage difference | $V_{CCD} - V_{CCA}$ | 1.5 | V |
| Analog reference voltage | V_{RIN} | -0.5 to $V_{CCA} + 7.0$ | V |
| Digital input voltage | V_{ID} | -0.5 to +7.0 | V |
| Storage temperature | Tstg | -55 to +125 | °C |

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

(A. GND = D. GND = 0V)

| Parameter | Symbol | Value | | | Unit |
|-------------------------------------|---------------------|-------|------|------|------|
| | | Min. | Typ. | Max. | |
| Power supply voltage | V_{CCA}, V_{CCD} | 4.75 | 5.00 | 5.25 | V |
| Power supply voltage difference | $V_{CCA} - V_{CCD}$ | -0.2 | — | 0.2 | V |
| Analog reference voltage | $V_{CCA} - V_{RIN}$ | 0.70 | 2.00 | 2.20 | V |
| | V_{RIN} | 2.65 | 3.00 | 4.30 | V |
| Digital "H" level input voltage | V_{IHD} | 2.0 | — | — | V |
| Digital "L" level input voltage | V_{ILD} | — | — | 0.8 | V |
| Clock frequency | f_{CLK} | — | — | 60 | MHz |
| Setup time | t_{SU} | 8.0 | — | — | ns |
| Hold time | t_{H} | 2.0 | — | — | ns |
| Minimum clock "H" level pulse width | t_{WH} | 6.5 | — | — | ns |
| Minimum clock "L" level pulse width | t_{WL} | 6.5 | — | — | ns |
| Phase compensation capacitance | C_{COMP} | 0.1 | — | — | μF |
| Operating ambient temperature | T_{OP} | -20 | — | 70 | °C |

■ ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions Otherwise Noted)

1. DC Characteristics

| Parameter | Symbol | Value | | | Unit | Remark |
|--------------------------------------|-----------------------------|----------------------------|----------------------------|----------------------------|--------|---|
| | | Min. | Typ. | Max. | | |
| Resolution | — | — | — | 10 | bit | — |
| Linearity error | LE | — | — | ±0.07 | % | DC Accuracy |
| Differential linearity error | DLE | — | — | ±0.07 | % | DC Accuracy |
| Digital "H" level input current | I _{IHD} | — | — | 20 | μA | V _{IHD} = 2.7 (V) |
| Digital "L" level input current | I _{I_{LD}} | -100 | — | — | μA | V _{I_{LD}} = 0.4 (V) |
| Reference input current | I _{RIN} | — | — | 10 | μA | V _{RIN} = 3.000 (V) |
| Reference voltage (Resister divided) | V _{ROUT1} | 2.900 | 3.000 | 3.100 | V | V _{CCA} = V _{CCD} = 5.00 (V) |
| Reference voltage (BGR) | V _{ROUT2} | V _{CCA} -2.100 | V _{CCA} -2.000 | V _{CCA} -1.900 | V | — |
| Reference voltage (BGR) | — | — | 100 | — | ppm/°C | — |
| RGB output voltage ratio | FSR | 0 | — | 6 | % | V _{CCA} = V _{CCD} = 5.00 (V) |
| Full-scale output voltage | V _{OFS} | V _{CCA} -20 | V _{CCA} | — | mV | — |
| Zero-scale output voltage | V _{OZS} | 2.932 | 3.002 | 3.072 | V | V _{CCA} = V _{CCD} = 5.00 (V) V _{RIN} = 3.000 (V) |
| Output resistance | R _O | 192 | 240 | 288 | Ω | T _a = 25°C |
| Supply current | I _{CC} | — | 92* | 152 | mA | V _{CCA} = V _{CCD} = 5.25 (V) V _{RIN} = V _{ROUT1} |

* : V_{CCA} = V_{CCD} = 5.00V

2. AC Characteristics

| Parameter | Symbol | Value | | | Unit | Remark |
|-------------------------------|------------------|-------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Maximum conversion rate | F _S | 60 | — | — | MSPS | Terminated A. OUT pin with 240Ω, C _L = 15pF |
| Output propagation delay time | t _{pd} | — | 7 | — | ns | |
| Output rising time | t _r | — | 5 | — | ns | |
| Output falling time | t _f | — | 5 | — | ns | |
| Setting time | t _{set} | — | 17.5 | — | ns | |

■ CALCULATION OF DAC OUTPUT VOLTAGE AT IDEAL CONVERSION

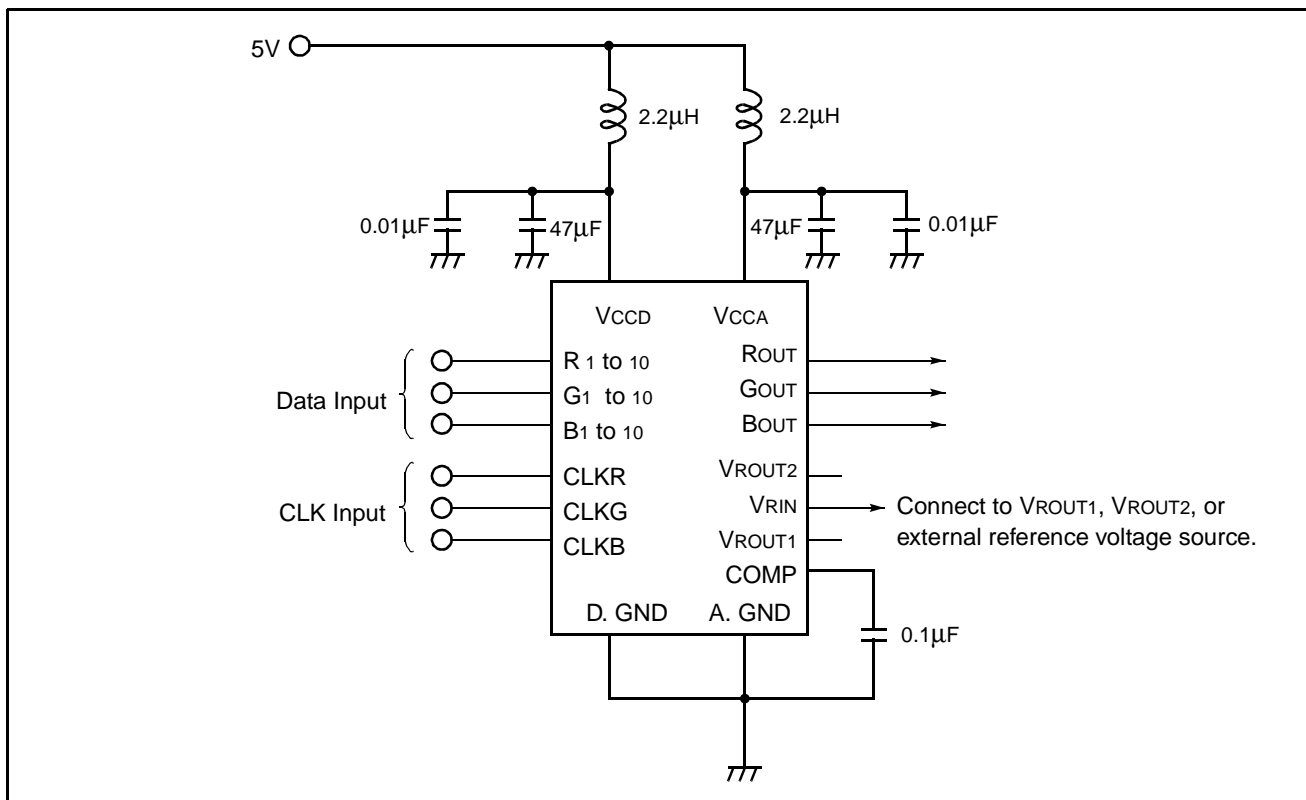
$$R_{OUT} \text{ (GOUT, BOUT)} = V_{CCA} - \frac{1023 - N}{1024} \times (V_{CCA} - V_{RIN})$$

[N : Digital Input Code (0 to 1023)]

$$V_{OFS} = V_{CCA}$$

$$V_{OZS} = V_{CCA} - \frac{1023}{1024} \times (V_{CCA} - V_{RIN})$$

■ TYPICAL CONNECTION EXAMPLE



■ NOTES ON USE

1. Power Supply Patterns of the PCB

The power supply wire patterns (Vcc and GND patterns) of the PCB should be designed as wide as possible in order to reduce parasitic impedance.

2. Switching Noise

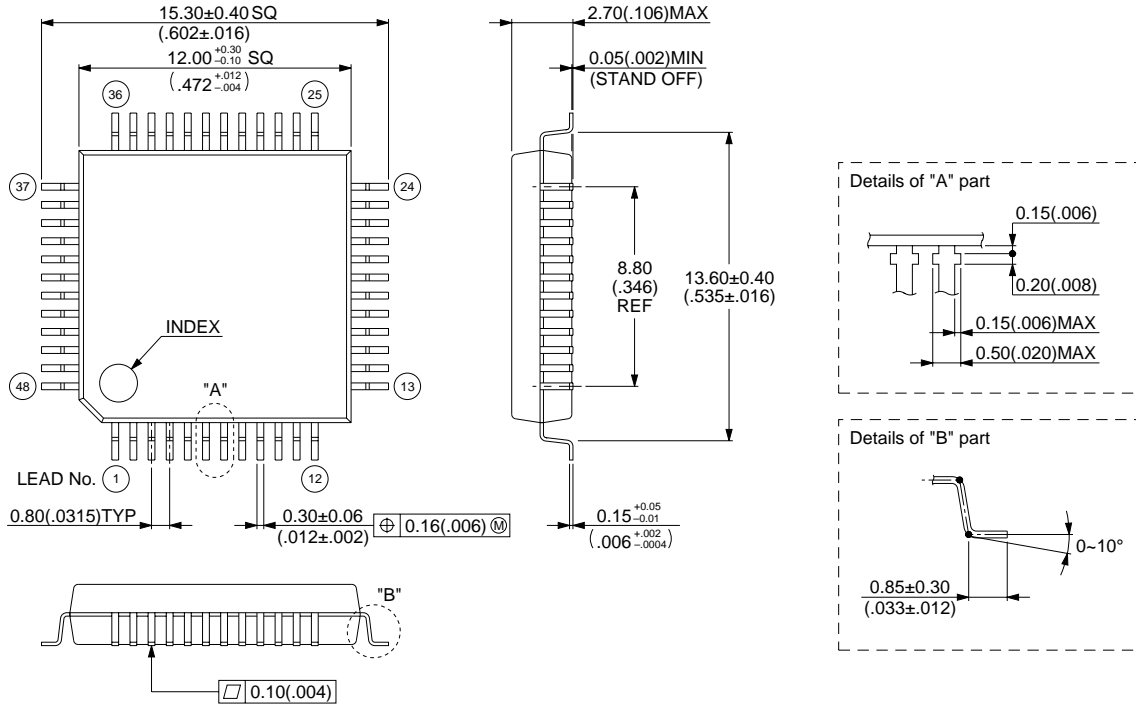
In order to reduce switching noise as much as possible, noise limit capacitor must be connected between Vccp and D. GND pins and VCCA and A. GND pins.

In this case, the capacitor should be connected to the GND pins side as near as possible.

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■ PACKAGE DIMENSION

48 pin, Plastic QFP
(FPT-48P-M15)



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Dimensions in mm (inches).

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