MAS1017

AM Receiver IC

- **High Sensitivity**
- **Very Low Power Consumption**
- **Wide Supply Voltage Range**
- **Power Down and Power Up Control**
- **High Selectivity by Crystal Filter**

DESCRIPTION

The MAS1017 AM-Receiver chip is a highly sensitive, simple to use AM receiver specially intended to receive time signals in the frequency range from 40 kHz to 100 kHz. There are only a few external components needed. The circuit has a preamplifier, wide range automatic gain control, demodulator and output comparator built in. The output signal can be processed directly with an additional digital circuitry to extract the data from the received signal.

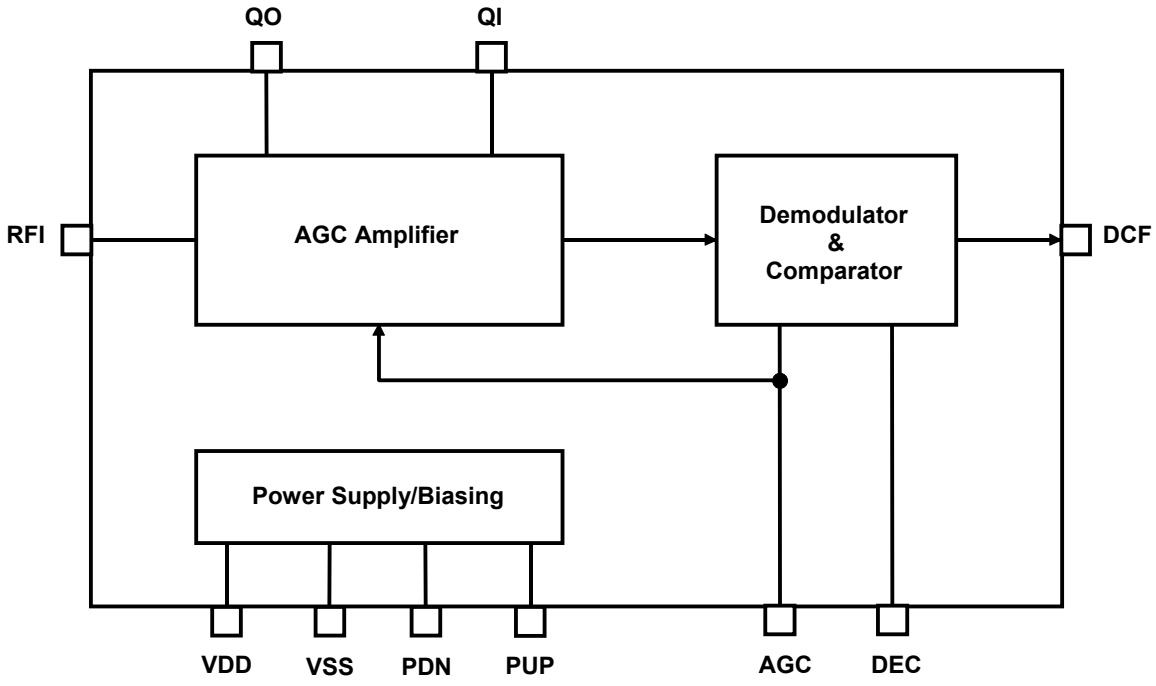
FEATURES

- Highly Sensitive AM Receiver
- Wide Supply Voltage Range
- Very Low Power Consumption
- Power Down and Power Up Control
- Only a Few External Components Needed
- Wide Frequency Range from 40 kHz to 100 kHz
- High Selectivity by Quartz Crystal Filter

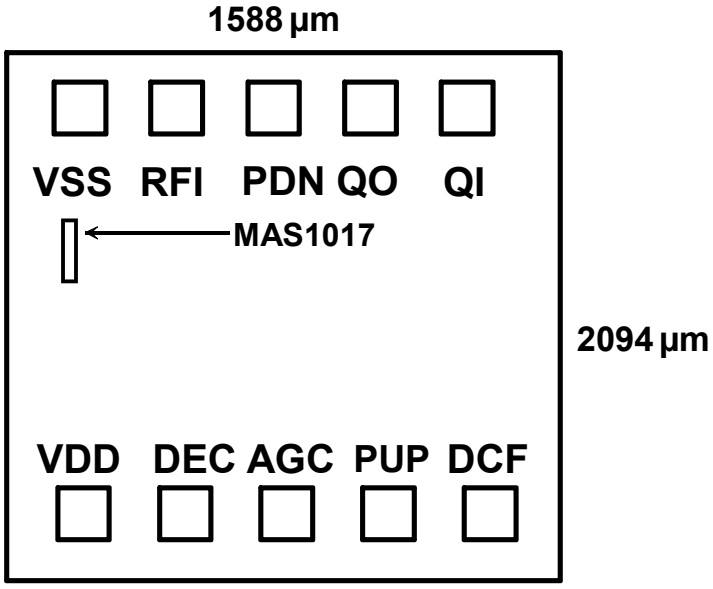
APPLICATIONS

- Time Signal Receiver for DCF77 (Germany)

BLOCK DIAGRAM



PAD LAYOUT



DIE size = 2.09 x 1.59 mm; PAD size = 100 x 100 µm
Substrate is connected to VDD. Please make sure that VDD is bonded first.
Note: Coordinates are calculated using VDD as a centre point.

Pad Identification	Name	X-coordinate	Y-coordinate	Note
Power Supply Voltage	VDD	0 µm	0 µm	
Demodulator Capacitor	DEC	244 µm	8 µm	
AGC Capacitor	AGC	520 µm	8 µm	
Power Up Input	PUP	759 µm	8 µm	1
DCF Signal Output	DCF	1075 µm	8 µm	2
Quarz Filter Input	QI	1038 µm	1625 µm	
Quarz Filter Output	QO	760 µm	1625 µm	
Power Down Input	PDN	483 µm	1625 µm	3
Receiver Input	RFI	243 µm	1625 µm	
Power Supply Ground	VSS	-15 µm	1605 µm	

Notes:
1) See power down control table below.
   - Internal pull-down resistor > 1 MΩ to VSS
2) DCF = VSS when carrier amplitude at maximum; DCF = VDD when carrier amplitude is reduced (25% modulated)
   - the output is a current source/sink with $|I_{OUT}| > 5$ µA
   - at power down the output is high impedance
3) See power down control logic table below.
   - Internal pull-up resistor > 1MΩ to VDD

PDN	PUP	Power Down
VSS	VSS	NO
VSS	VDD	NO
VDD	VSS	YES (In power down if both PDN and PUP are left unconnected)
VDD	VDD	NO

ABSOLUTE MAXIMUM RATINGS

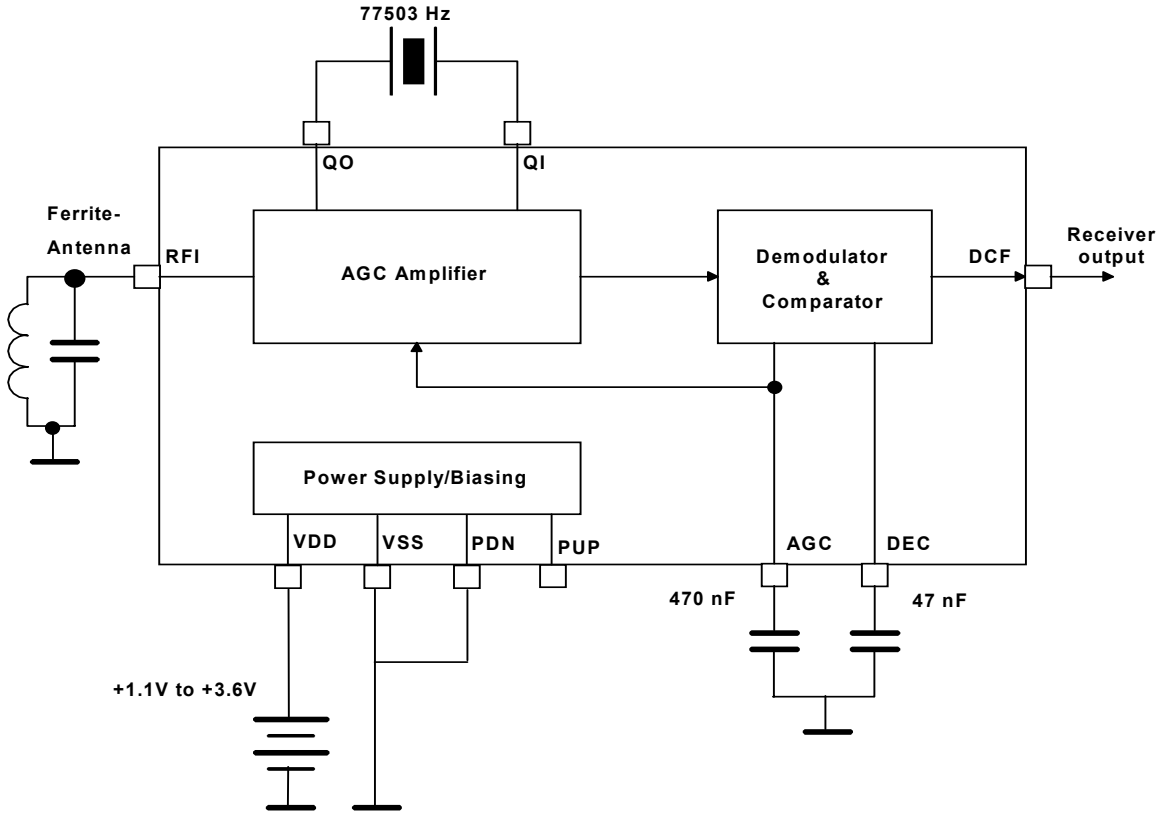
Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}-V_{SS}		-0.3	5.0	V
Input Voltage	V_{IN}		V_{SS}-0.3	V_{DD}+0.3	V
Power Dissipation	P_{MAX}			100	mW
Operating Temperature	T_{OP}		-20	70	°C
Storage Temperature	T_{ST}		-40	120	°C

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 1.4V, Temperature = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}		1.10		3.60	V
Current Consumption	I_{DD}			40	100	µA
Stand-By Current	I_{DDoff}				0.1	µA
Input Range	f_{IN}		40		100	kHz
Sensitivity	V_{IN}		0.001		20	mVrms
Input Levels $\|I_{IN}\|$<0.5 µA	V_{IL} V_{IH}		 V_{DD} – 0.3		0.3	V
Output Current V_{OL}<0.2 V_{DD};V_{OH} >0.8 V_{DD}	$\|I_{OUT}\|$		5			µA
Output Pulse	T_0		50		140	ms
	T_1		150		230	ms
Startup Time	T_{Start}			8		s
Output Delay Time	T_{Delay}			50		ms

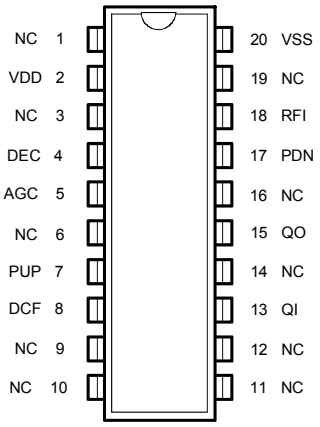
TYPICAL APPLICATION



Note 1: Ferrite Antenna and Crystal
The crystal as well as ferrite antenna frequencies are chosen according to the time signal system frequency. DCF-77 transmitter frequency is 77.5 kHz. The ferrite antenna center frequency has to be tuned to 77.5 kHz. The optimal crystal frequency is 77503 Hz but also 77500 Hz crystal can be used. The shunt capacitance of the crystal should be as close as possible to internal shunt capacitance compensation capacitor of 0.75 pF for optimal noise filtering.

Note 2: AGC and DEC Capacitors
The AGC and DEC capacitors should have low leakage currents due to very small 40 nA signal currents through the capacitors. The insulation resistance of these capacitors should be higher than 70 MΩ. Also probes with at least 100 MΩ impedance should be used for voltage probing of AGC and DEC pins.

SAMPLES IN SBDIL 20 PACKAGE



PIN DESCRIPTION

Pin Name	Pin	Type	Function	Note
NC	1			
VDD	2	P	Positive power supply	
NC	3			
DEC	4	AO	Demodulator capacitor	
AGC	5	AO	AGC capacitor	
NC	6			
PUP	7	AI	Power up input	1
DCF	8	DO	Demodulator output	2
NC	9			
NC	10			
NC	11			
NC	12			
QI	13	AI	Quartz filter input	
NC	14			3
QO	15	AO	Quartz filter output	
NC	16			
PDN	17	AI	Power down input	4
RFI	18	AI	Receiver input	
NC	19			
VSS	20	G	Power supply ground	

Notes:

1) See power down control table on page 2.
   - Internal pull-down resistor > 1 MΩ to VSS
2) DCF = VSS when carrier amplitude at maximum; DCF = VDD when carrier amplitude is reduced (25% modulated)
   - the output is a current source/sink with $|I_{OUT}| > 5\ \mu A$
   - at power down the output is high impedance
3) Pin 14 between quartz crystal filter pins must be connected to VSS to eliminate package leadframe parasitic capacitances disturbing the crystal filter performance. All other NC (Not Connected) pins are also recommended to be connected to VSS to minimize noise coupling.
4) See power down control logic table on page 2.
   - Internal pull-up resistor > 1MΩ to VDD

ORDERING INFORMATION

Product Code	Product	Package	Comments
MAS1017ATC1	AM-Receiver IC	Wafer, EWS-tested	wafer thickness 400 µm
MAS1017ATC1-1	AM-Receiver IC	Dice on sticky tape	wafer thickness 400 µm, sawn wafer, tape ring 6”, non UV tape, tape not expanded

Please contact Micro Analog Systems Oy for other wafer thickness, sawn wafer delivery as well as SMD package options.

LOCAL DISTRIBUTOR

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