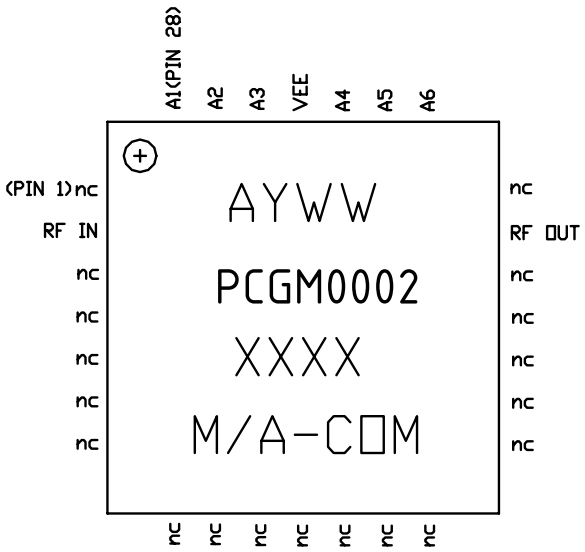
Phase Shifter
3.5-6.0 GHz

MAPCGM0002
903214 —
Preliminary Information

Features

- 6 Bit Phase Shifter
- 360° Coverage, LSB = 5.6°
- TTL Control Inputs
- MSAG™ Process
- 6mm, 28 Lead, PQFN Package



Description

The MAPCGM0002 is a 6-bit Phase Shifter with Parallel TTL Input Control and is packaged in a micro lead package (MLP). This product is fully matched to 50 ohms on both the input and output. This part has 360° of phase coverage in 5.6° increments.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate (MSAG™) Process, each device is 100% RF tested on wafer to ensure performance compliance.

M/A-COM's MSAG™ process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.

Primary Applications

- Satellite Communication
- Phased Array Radar

Absolute Maximum Conditions [1]

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	30	dBm
Digital Supply Voltage	V_{EE}	-6.0	V
Junction Temperature	T_J	180	°C
Storage Temperature	T_{STG}	-55 to +150	°C

1. Operation outside of these ranges may reduce product reliability. Operation at other than the typical values may result in performance outside the guaranteed limits.

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Control Voltage	A1 thru A6				
Logic High		2.8	5	5	V
Logic Low		0	0	0.8	V
Junction Temperature	T_J			150	°C
Digital Supply Voltage	V_{EE}	-5.2	-5.0	-4.8	V

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Electrical Characteristics: T_B = 25°C[2], Z_0 = 50Ω, V_{EE} = -5V

Parameter	Symbol	Typical	Units
Bandwidth	f	3.5-6.0	GHz
Insertion Loss	IL	6.5	dB
Input VSWR (At Reference)	VSWR	1.6:1	
Output VSWR (At Reference)	VSWR	1.7:1	
RMS Phase Error	RMS	9	º
RMS Phase Error — Calibrated	RMS	3	º
Phase Range	ΔΦ	360	º
Gain Variation over all Phase Shifter settings	ΔG	< 3	dB
Digital Supply Current	I_{EE}	< 10	mA
Input Third Order Intercept	ITOI	32	dBm
Input 1-dB Compression Point	P_{1dB}	26	dBm

2. T_B = Package Base Temperature

Truth Table[3]

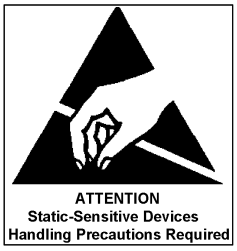
Pin	Designation	Description	Level	State
22	A6	180° Phase Bit : MSB	Logic High	Phase Shift ≈ -180°
23	A5	90° Phase Bit	Logic High	Phase Shift ≈ -90°
24	A4	45° Phase Bit	Logic High	Phase Shift ≈ -45°
25	V_{EE}	DC Supply Voltage	-5V	ON
26	A3	22.5° Phase Bit	Logic High	Phase Shift ≈ -22.5°
27	A2	11.2° Phase Bit	Logic High	Phase Shift ≈ -11.2°
28	A1	5.6° Phase Bit : LSB	Logic High	Phase Shift ≈ -5.6°

3. All Phase Bits at Logic Low = Reference State.

Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply V_{EE} = -5 V.
2. Apply Logic Voltages to control circuit as listed in Recommended Operating Conditions Table.
3. Power Down. Set V_{EE} = 0.



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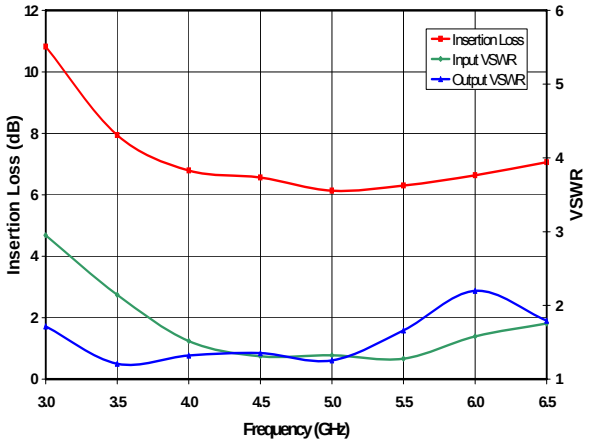

Figure 1. Reference State Insertion Loss, Input and Output VSWR vs. Frequency

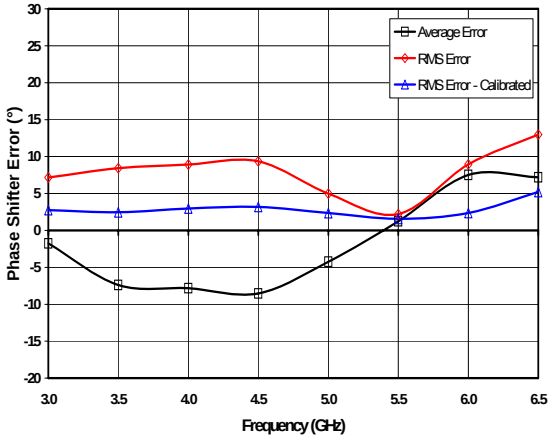

Figure 2. Phase Shifter Figures of Merit: Average Error vs. Reference State, RMS Error and Calibrated RMS Error Over All States

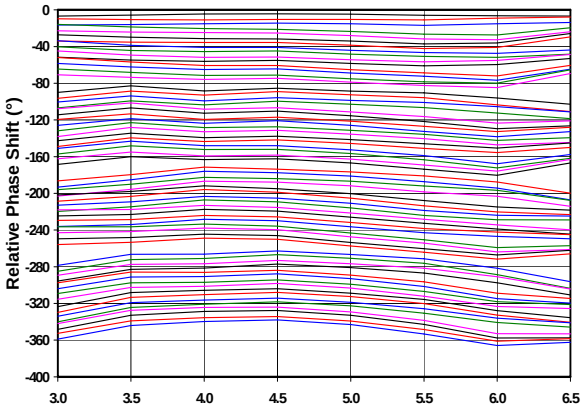

Figure 3. Relative Phase Shift vs. Phase Shifter State

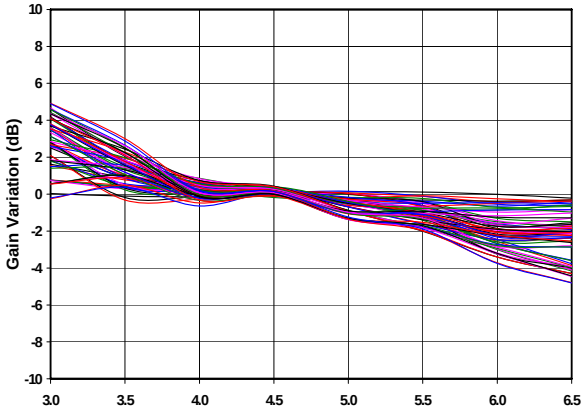

Figure 4. Relative Gain Change vs. Phase Shifter State

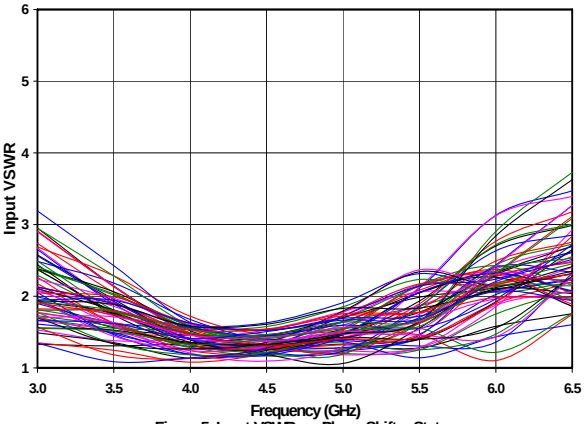

Figure 5. Input VSWR vs. Phase Shifter State

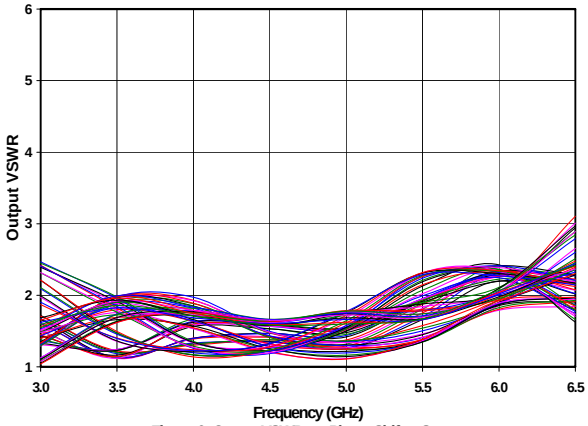

Figure 6. Output VSWR vs. Phase Shifter State

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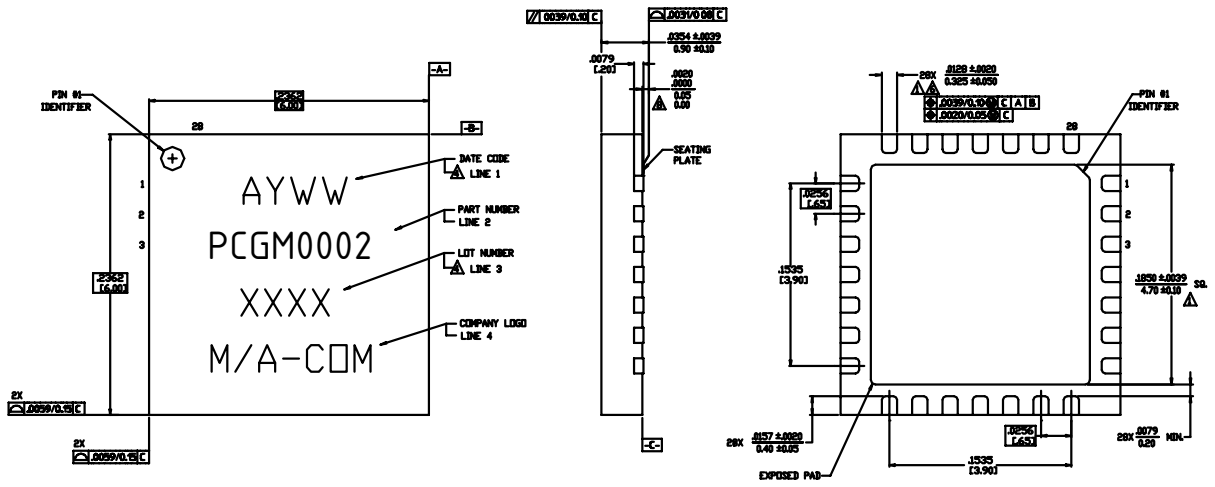

Figure 7. 6mm FQFP-N 28 Lead Package Drawing

Reference JEDEC M0-220 (see http://www.jedec.org), VAR. VJJC-3 (Issue E) for additional dimensional and tolerance information.

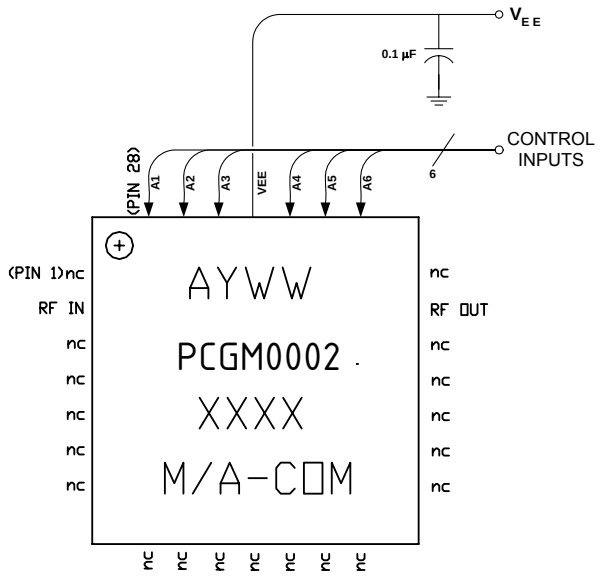

Figure 8. Recommended Bias Configuration

Refer to M/A-COM Application Note ***Surface Mounting Instructions for FQFP-N Packages*** **#S2083*** for assembly guidelines.

Application Notes can be found by going to the Site Search Page on M/A-COM's web page (http://www.macom.com/search/search.jsp) and searching for the required Application Note.

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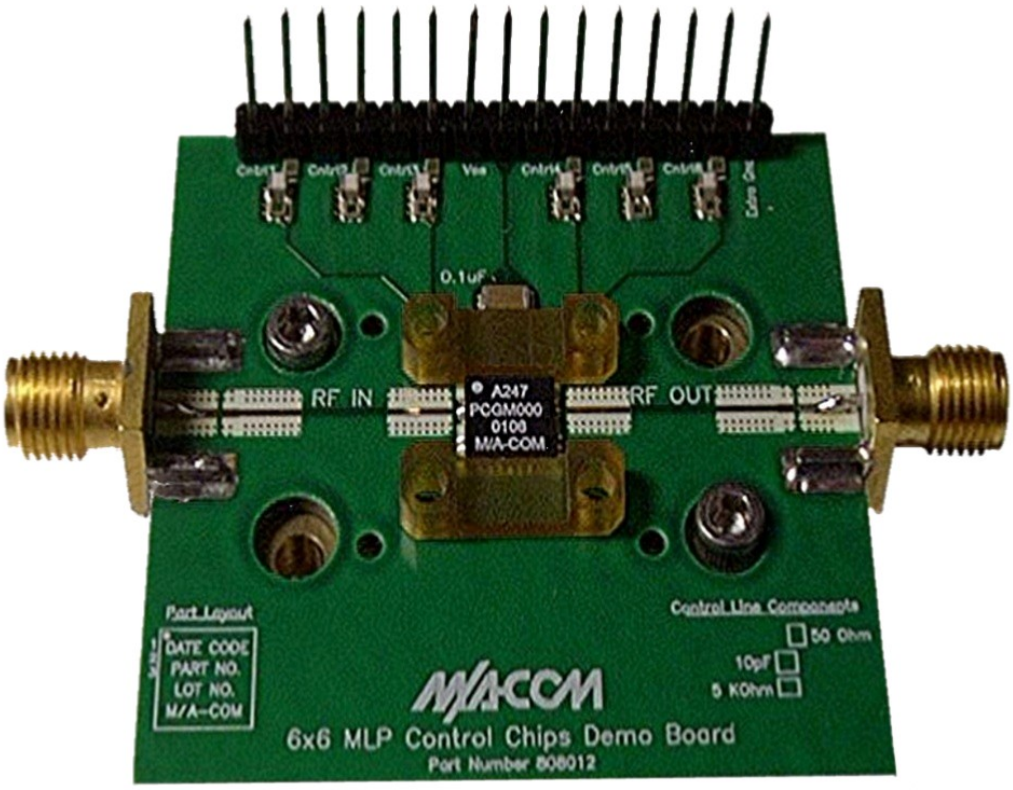

Figure 9. Demonstration Board (available upon request).

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