

Amplifier, Power, 1.9W  
10.0-13.25 GHz

MAAPGM0070-DIE  
Rev B  
Preliminary Datasheet

## Features

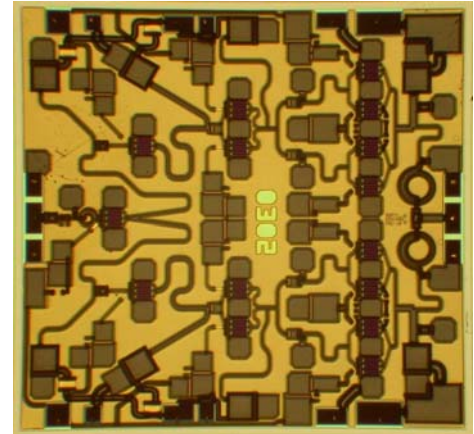
- ◆ 1.9 Watt Saturated Output Power Level
- ◆ Variable Drain Voltage (4-10V) Operation
- ◆ MSAG<sup>®</sup> Process

## Description

The MAAPGM0070-DIE is a 4-stage 1.9 W power amplifier with on-chip bias networks. This product is fully matched to 50 ohms on both the input and output. It can be used as a power amplifier stage or as a driver stage in high power applications.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate (MSAG<sup>™</sup>) Process, each device is 100% RF tested on wafer to ensure performance compliance.

M/A-COM's MSAG<sup>™</sup> process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.



## Primary Applications

- ◆ Point-to-Point Radio
  - ◆ 10, 11 and 13 GHz Bands

## Also Available in:

Description	Ceramic Package	Plastic Package	SAMPLES	
			Sample Board (Die)	Mechanical Sample (Die)
Part Number	MAAPGM0070	MAAP-000070-PKG003	MAAP-000070-SMB003	MAAP-000070-MCH000

**Electrical Characteristics:**  $T_B = 30^\circ\text{C}^1$ ,  $Z_0 = 50 \Omega$ ,  $V_{DD} = 8\text{V}$ ,  $I_{DQ} = 900\text{mA}^2$ ,  $P_{in} = 8 \text{ dBm}$ ,  $R_G = 100 \Omega$

Parameter	Symbol	Typical	Units
Bandwidth	f	10-13.25	GHz
Output Power	$P_{OUT}$	32.8	dBm
1-dB Compression Point	$P_{1dB}$	32.6	dBm
Power Added Efficiency	PAE	25	%
Small Signal Gain	G	34	dB
Input VSWR	VSWR	1.8:1	
Output VSWR	VSWR	2.1:1	
Output Third Order Intercept	TOI	39	dBm
Output Third Order Intermod, $P_{out} = 26 \text{ dBm}$ (DCL)	IMD3	30	dBc
Gate Current	$I_{GG}$	10	mA
Drain Current	$I_{DD}$	900	mA

1.  $T_B = \text{MMIC Base Temperature}$
2. Adjust  $V_{GG}$  between  $-2.6$  and  $-1.2\text{V}$  to achieve specified  $I_{DQ}$ .

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- **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

Visit [www.macom.com](http://www.macom.com) for additional data sheets and product information.

### Maximum Ratings<sup>3</sup>

Parameter	Symbol	Absolute Maximum	Units
Input Power	$P_{IN}$	13.0	dBm
Drain Supply Voltage	$V_{DD}$	+12.0	V
Gate Supply Voltage	$V_{GG}$	-3.0	V
Quiescent Drain Current (No RF)	$I_{DQ}$	1.42	A
Quiescent DC Power Dissipated (No RF)	$P_{DISS}$	14.2	W
Junction Temperature	$T_J$	170	°C
Storage Temperature	$T_{STG}$	-55 to +150	°C

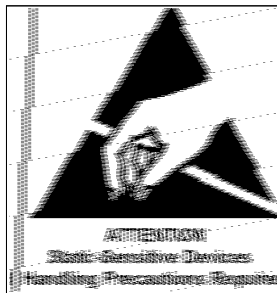
3. Operation beyond these limits may result in permanent damage to the part.

### Recommended Operating Conditions<sup>4</sup>

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Voltage	$V_{DD}$	4.0	8.0	10.0	V
Gate Voltage	$V_{GG}$	-2.6	-2.0	-1.2	V
Input Power	$P_{IN}$		8.0	11.0	dBm
Thermal Resistance	$\Theta_{JC}$		10.3		°C/W
MMIC Base Temperature	$T_B$			Note 5	°C

4. Operation outside of these ranges may reduce product reliability.

5. MMIC Base Temperature = 170°C —  $\Theta_{JC} * V_{DD} * I_{DQ}$

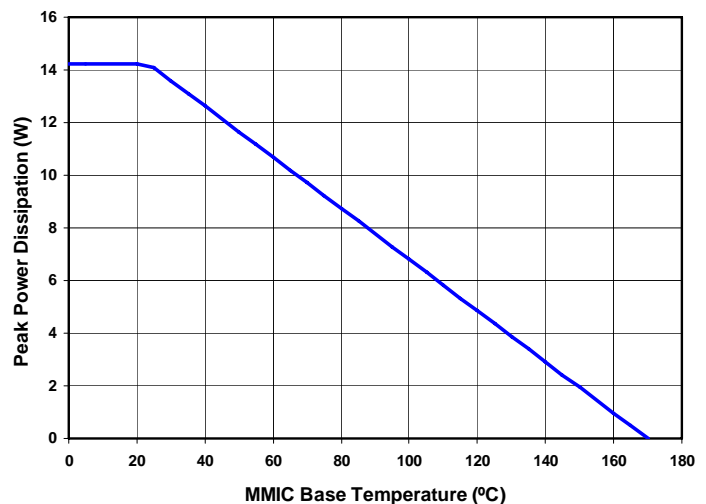


### Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply  $V_{GG} = -2.7$  V,  $V_{DD} = 0$  V.
2. Ramp  $V_{DD}$  to desired voltage, typically 8.0 V.
3. Adjust  $V_{GG}$  to set  $I_{DQ}$ , (approximately @ -2.0 V).
4. Set RF input.
5. Power down sequence in reverse. Turn  $V_{GG}$  off last.

Power Derating Curve, Quiescent (No RF)



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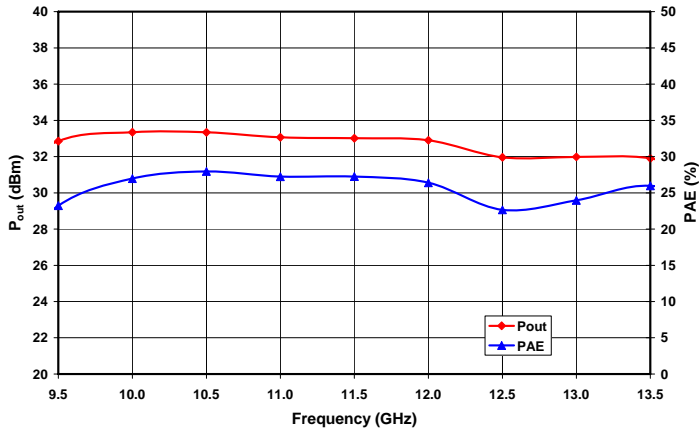


Figure 1. Output Power and Power Added Efficiency at  $V_D = 8V$ ,  $P_{in} = 8dBm$ , and 25% IDSS

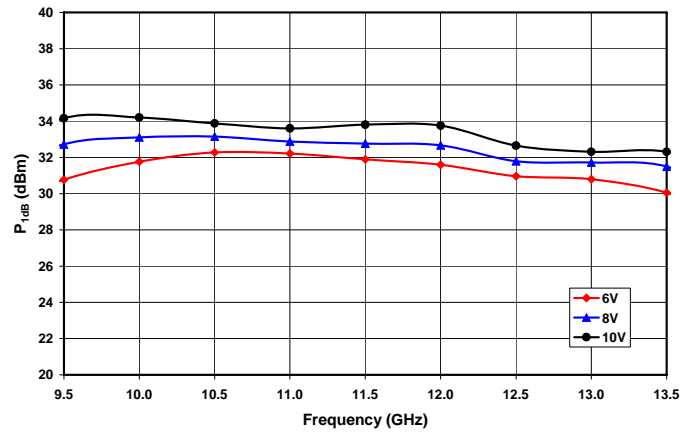


Figure 2. 1dB Compression Point and Drain Voltage at 25% IDSS

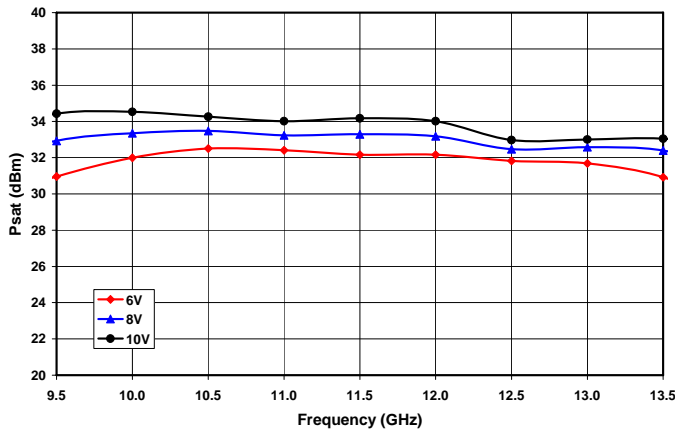


Figure 3. Saturated Output Power and Drain Voltage at 25% IDSS

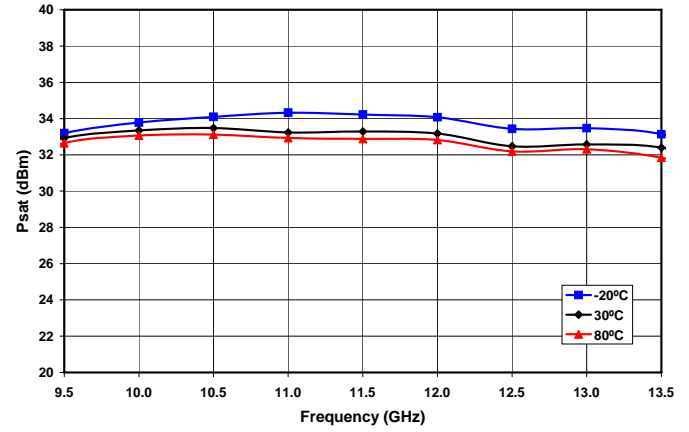


Figure 4. Saturated Output Power and Temperature at 8V and 25% IDSS

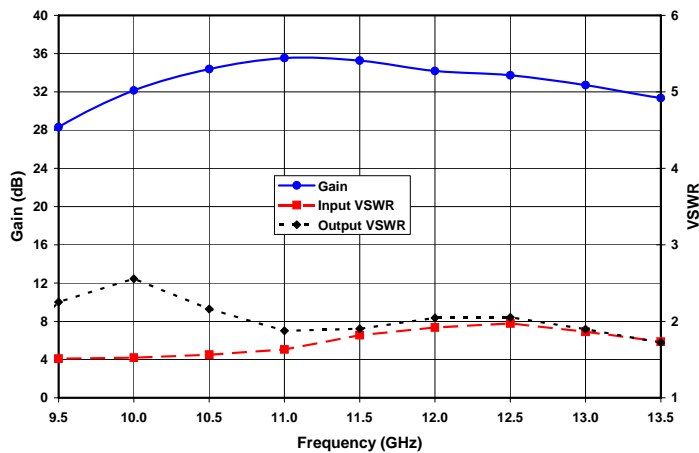


Figure 5. Small Signal Gain and Input and Output VSWR at 25% IDSS,  $V_D = 8V$

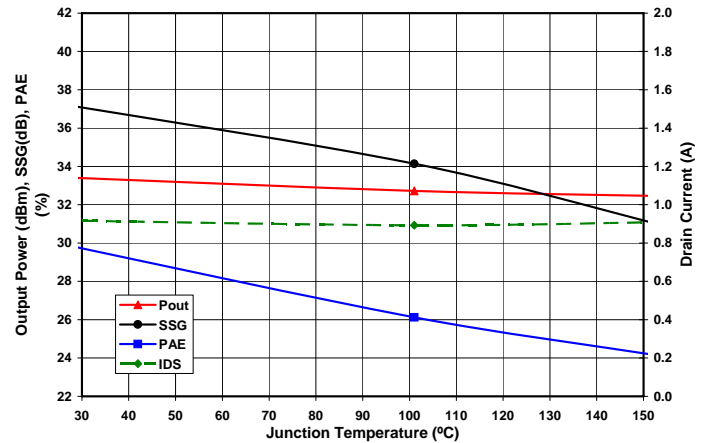


Figure 6. Output Power, Small Signal Gain, Power Added Efficiency, and Drain Current vs. Junction Temperature at 8V, 12 GHz, and 25% IDSS

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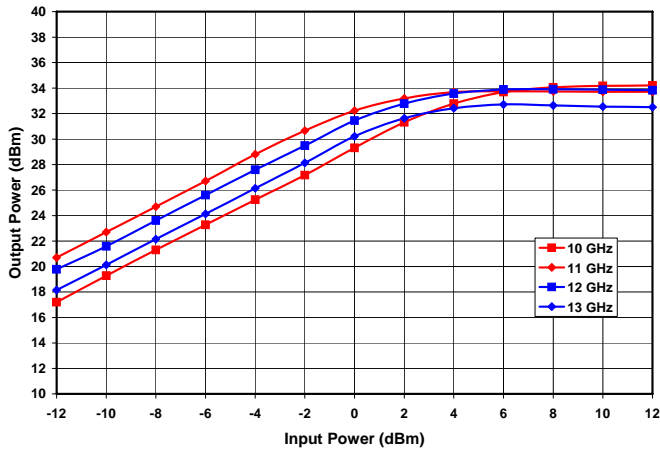


Figure 7. Output Power vs. Input Power and Frequency at 10V and 25% IDSS

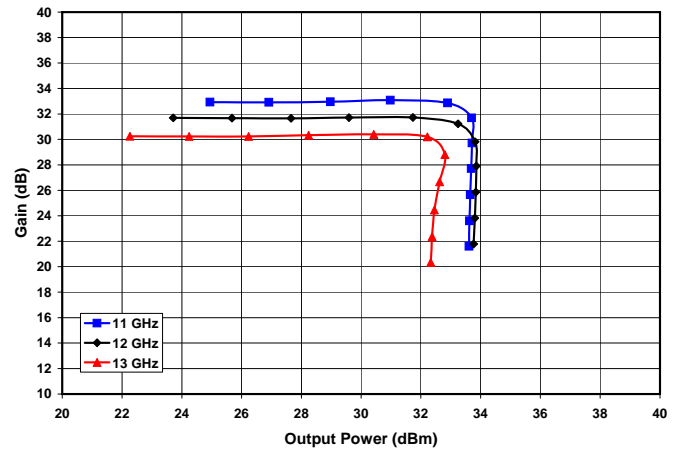


Figure 8. Gain vs. Output Power and Frequency at 10V and 25% IDSS

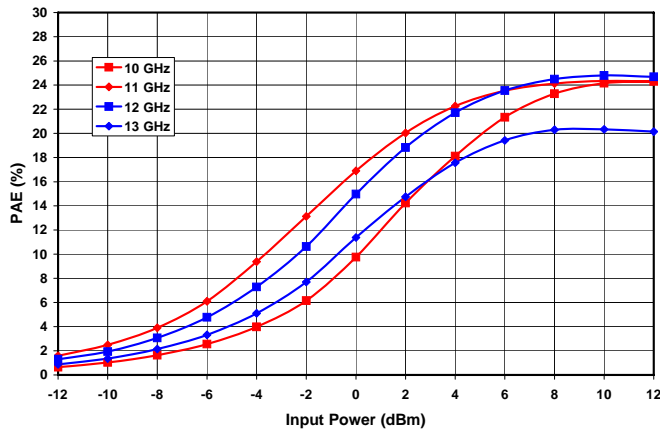


Figure 9. Power Added Efficiency vs. Input Power and Frequency at 10V and 25% IDSS

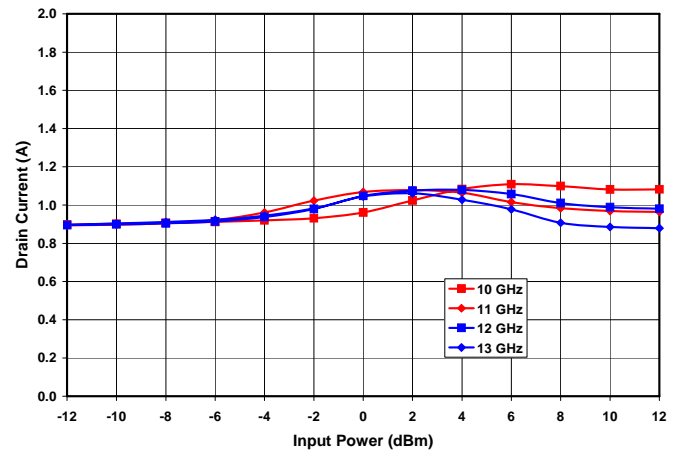


Figure 10. Drain Current vs. Input Power and Frequency at 10V and 25% IDSS

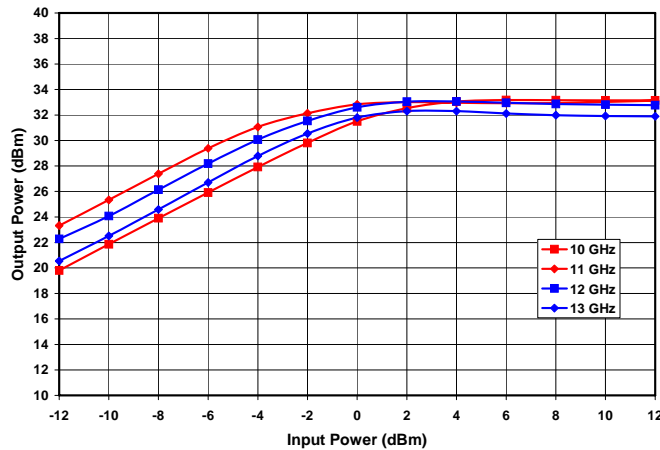


Figure 11. Output Power vs. Input Power and Frequency at 8V and 25% IDSS

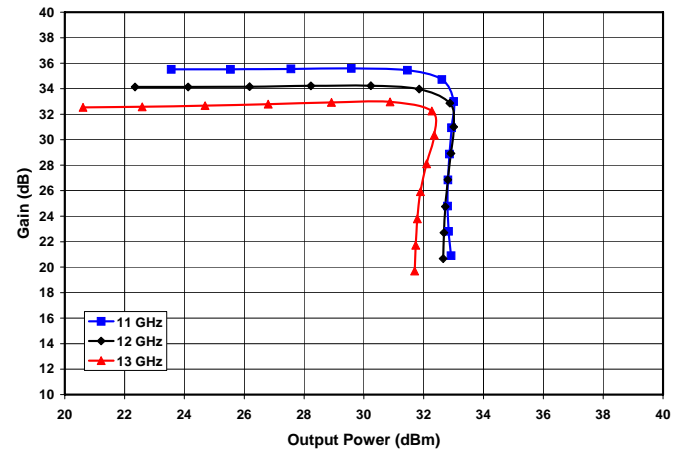


Figure 12. Gain vs. Output Power and Frequency at 8V and 25% IDSS

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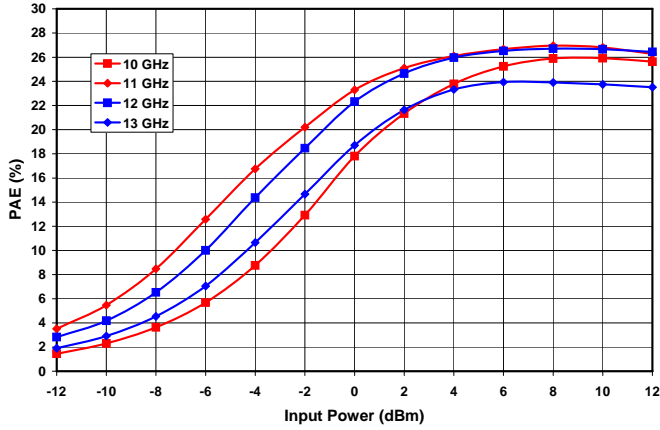


Figure 13. Power Added Efficiency vs. Input Power and Frequency at 8V and 25% IDSS

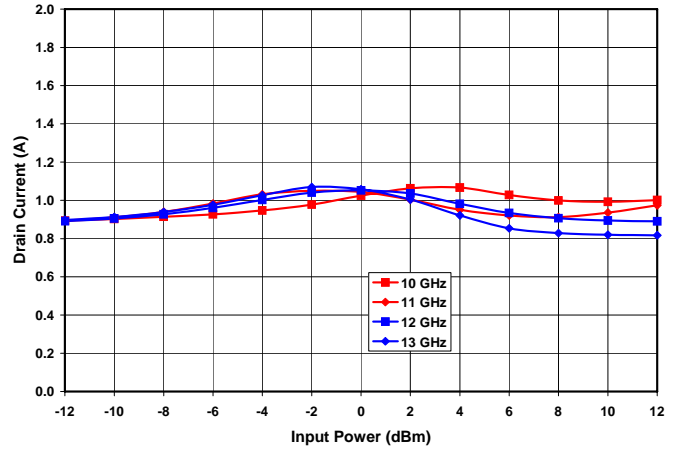


Figure 14. Drain Current vs. Input Power and Frequency at 8V and 25% IDSS

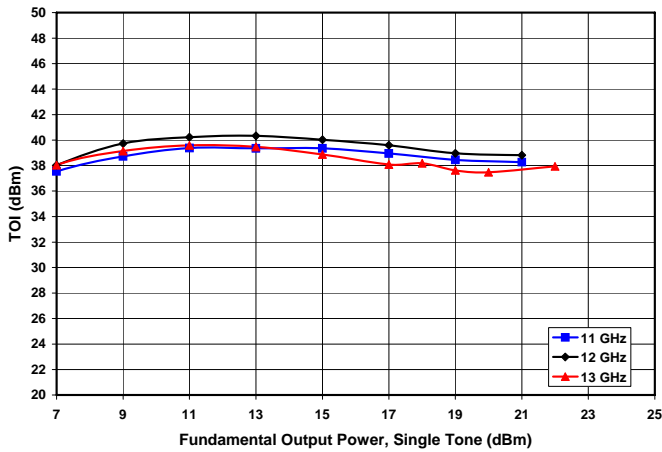


Figure 15. Third Order Intercept vs. Output Power and Frequency at 6V.

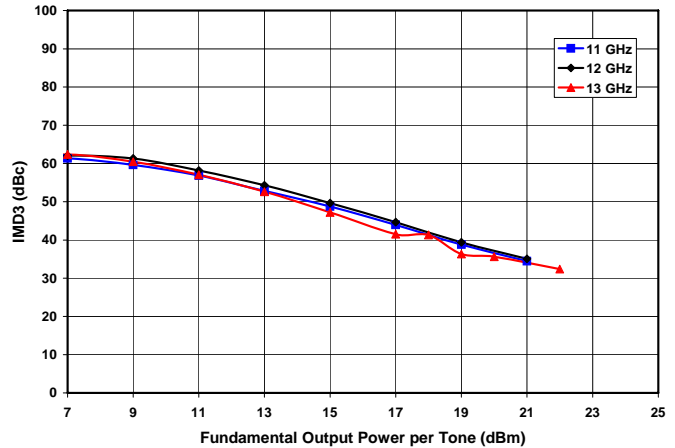


Figure 16. Third Order Intermod vs. Output Power and Frequency at 6V.

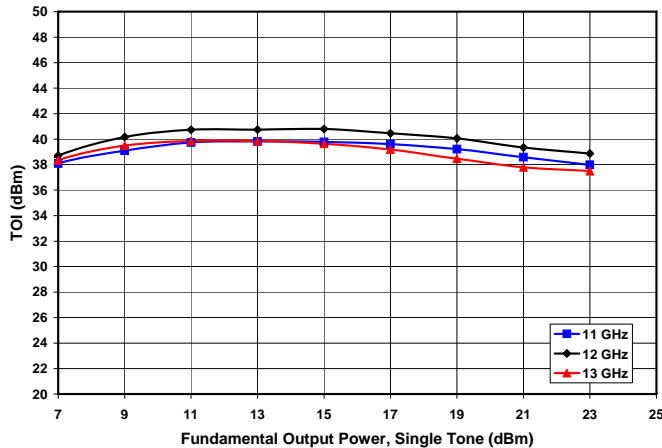


Figure 17. Third Order Intercept vs. Output Power and Frequency at 8V.

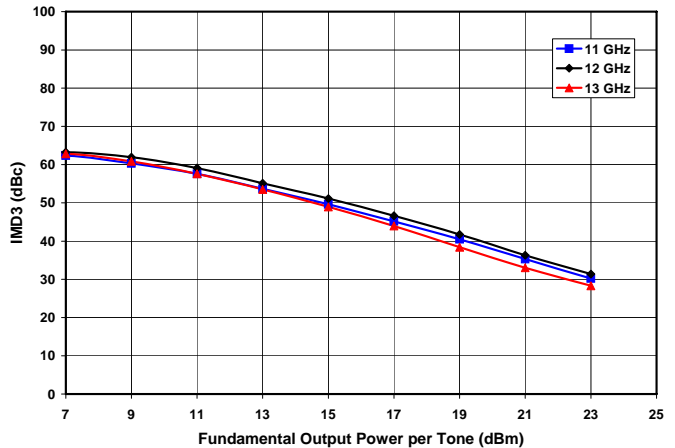


Figure 18. Third Order Intermod vs. Output Power and Frequency at 8V.

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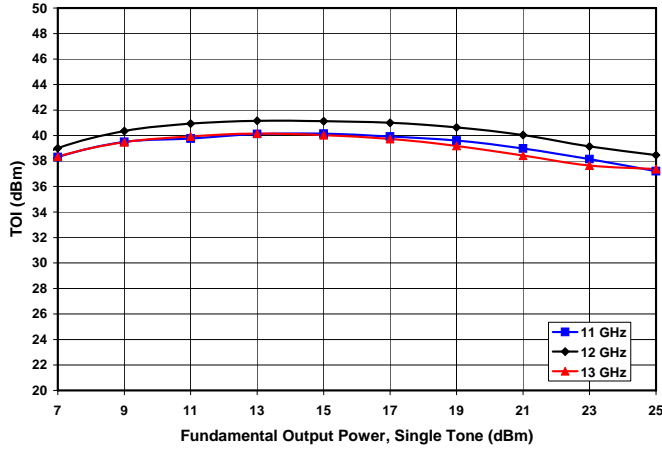


Figure 19. Third Order Intercept vs. Output Power and Frequency at 10V.

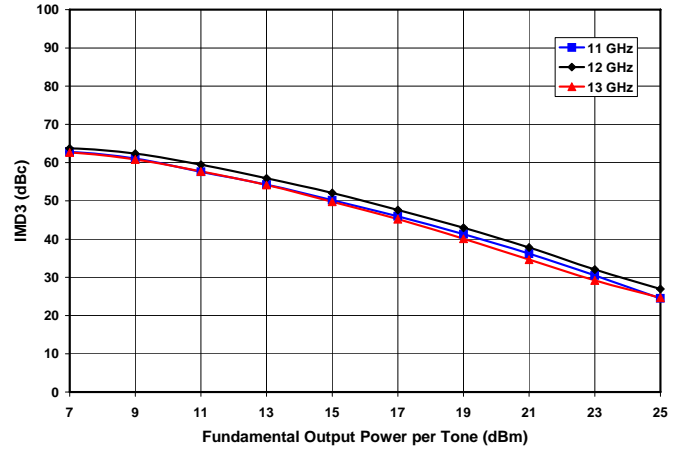


Figure 20. Third Order Intermod vs. Output Power and Frequency at 10V.

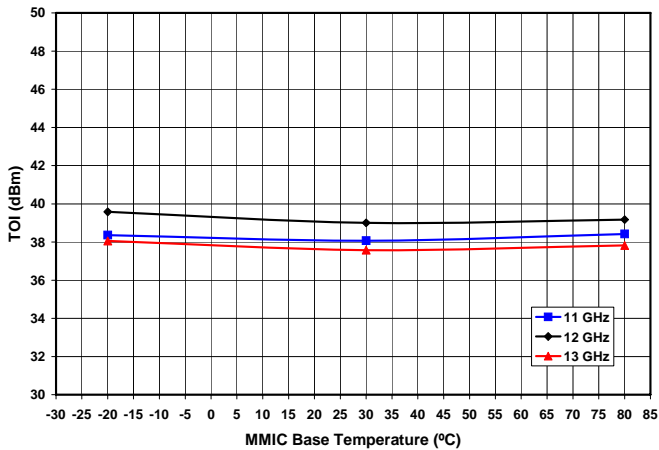


Figure 21. Third Order Intercept vs. Temperature and Frequency at 8V and  $P_{out} = 26$  dBm DCL.

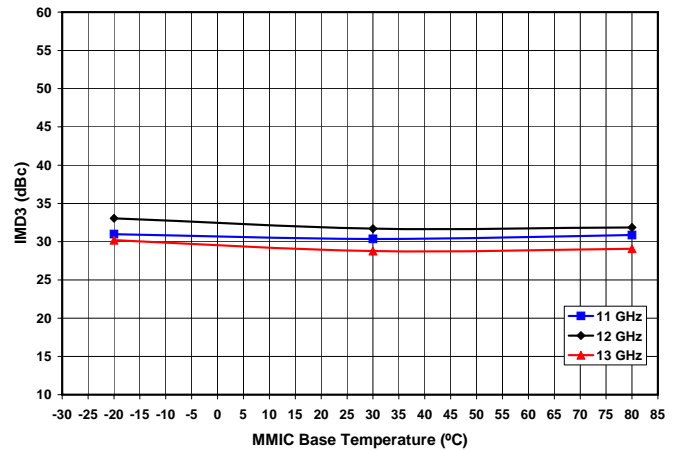
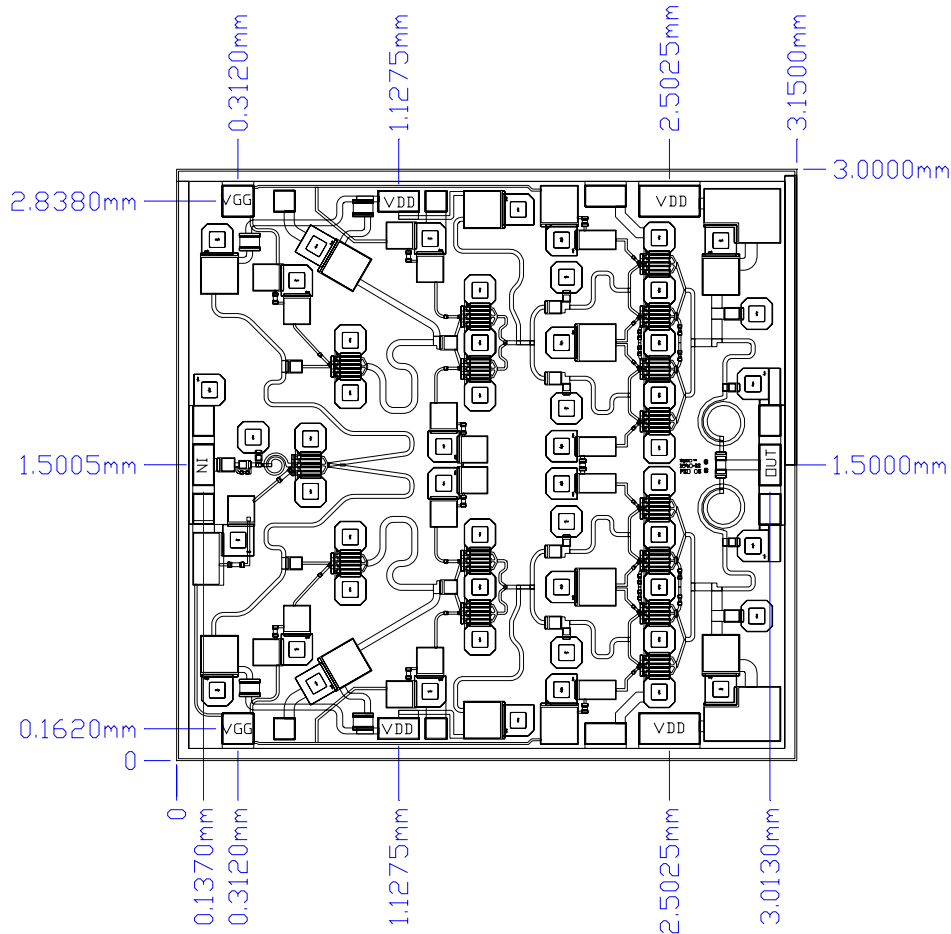


Figure 22. Third Order Intermod vs. Temperature and Frequency at 8V and  $P_{out} = 25$  dBm DCL.

**Mechanical Information**

Chip Size: 3.000 x 3.150 x 0.075 mm (118 x 124 x 3 mils)



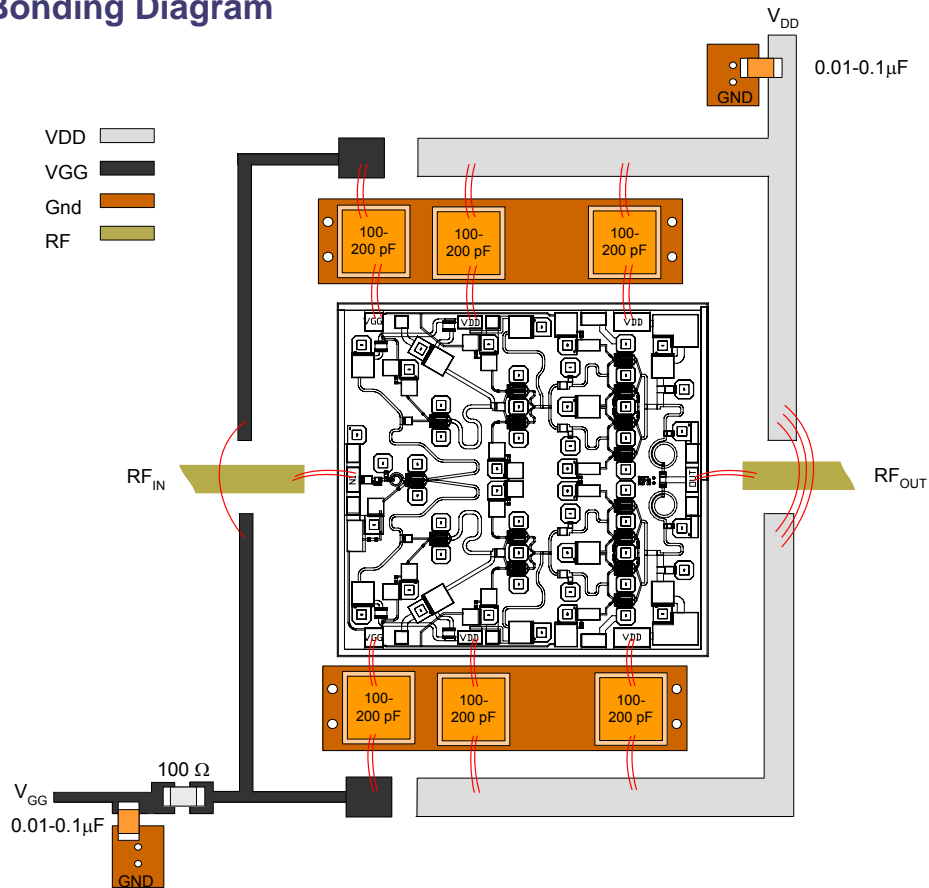
Chip edge to bond pad dimensions are shown to the center of the bond pad.

**Figure 23. Die Layout**

**Bond Pad Dimensions**

Pad	Size (µm)	Size (mils)
RF In and Out	100 x 200	4 x 8
DC Drain Supply Voltage VDD	200 x 100	8 x 4
DC Gate Supply Voltage VGG	150 x 150	6 x 6

**Assembly and Bonding Diagram**



**Figure 24. Recommended operational configuration. Wire bond as shown.**

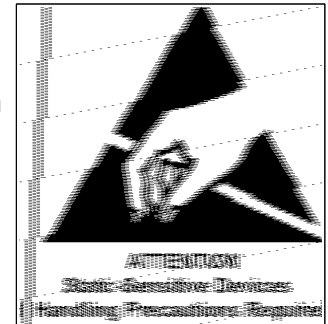
**Die Handling:**

Refer to Application Note AN3016.

**Assembly Instructions:**

**Die Attach:** Use AuSn (80/20) 1 mil. preform solder. Limit time @ 310 °C to less than 7 minutes. Refer to Application Note AN3017 for more detailed information.

**Wirebonding:** Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.



**Biasing Note: Must apply negative bias to V<sub>GG</sub> before applying positive bias to V<sub>DD</sub> to prevent damage to amplifier.**