

M66300P/FP

PARALLEL-IN SERIAL-OUT DATA BUFFER WITH FIFO

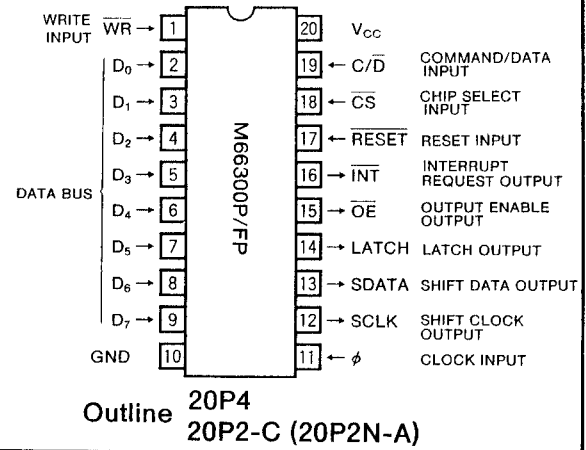
DESCRIPTION

The M66300P/FP is a CMOS-type large-scale integrated circuit with 63-byte FIFO (First-In First-Out Memory). Commands or data up to 63 bytes can be stored directly from the 8-bit bus. The data stored in the FIFO can be output as serial data on command and, when output ends, an interrupt request signal is output. Having 2-bit output (\overline{OE} , LATCH) which can be set/reset by the command, M66300 can be connected to peripheral circuits that have a serial latch structure.

FEATURES

- General-purpose 8-bit CPU bus compatible
- Built-in 63-byte FIFO
- High-speed output (10Mbps)
- Direct connection to LED array driver such as M66310 or M66311
- Low-noise, high-output circuit
 $I_{OL}=24mA, I_{OH}=-24mA$
 $(I_{OL}=4mA, I_{OH}=-4mA \text{ for } \overline{INT})$
- TTL compatible inputs
 $V_{IL}=0.8V \text{ max}, V_{IH}=2.0V \text{ min}$
- Schmitt input (\overline{RESET})
 Hysteresis 0.8V typ

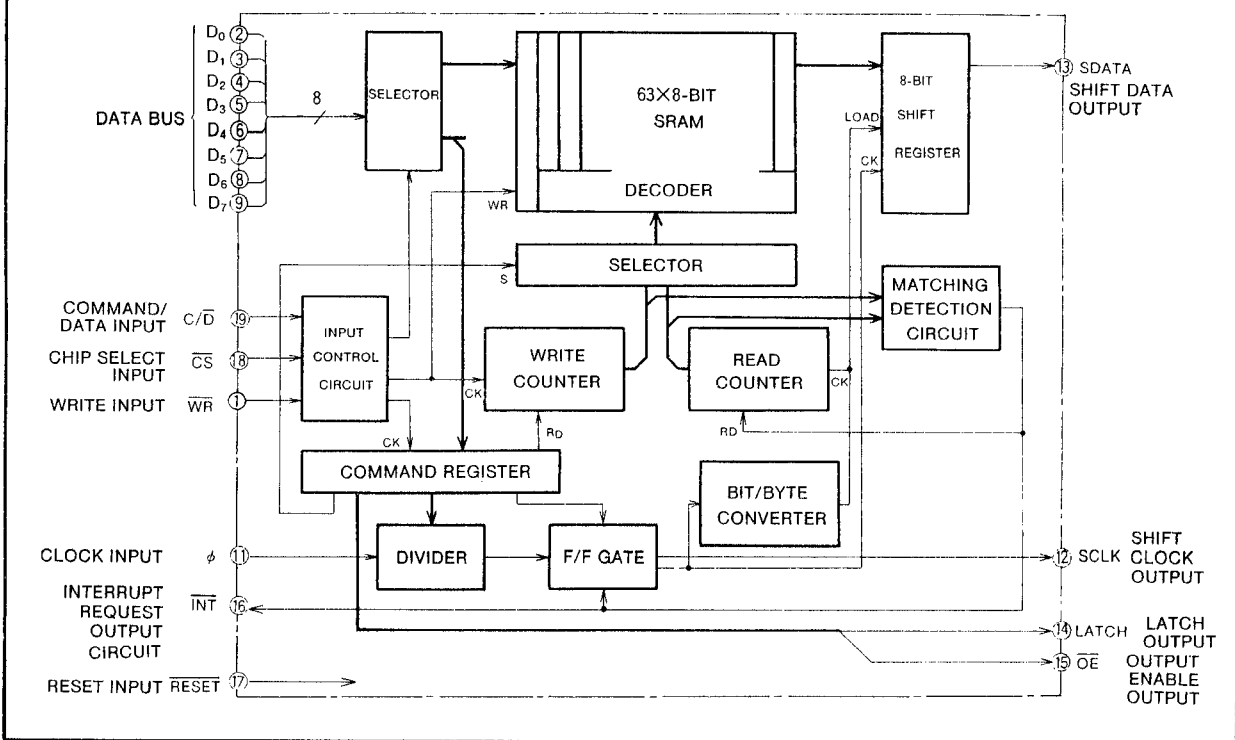
PIN CONFIGURATION (TOP VIEW)



APPLICATION

General digital equipment for industrial and home use, panel display controllers, and eraser unit controller for copying machine.

BLOCK DIAGRAM



PARALLEL-IN SERIAL-OUT DATA BUFFER WITH FIFO

FUNCTION

The information on data bus D₀~D₇ is considered as commands when C/D=1, and as data when C/D=0. There are four kinds of commands.

Command 1 sets division ratio for clock input φ and outputs as shift clock SCLK.

Command 2 sets the M66300 to write mode. The CPU is capable of writing 8-bit parallel data (C/D=0) of up to 63 bytes into the internal memory (FIFO) of the M66300.

Command 3 sets the M66300 to serial output mode. All

data written in the internal memory (FIFO) is output as serial data starting with the LSB, in sync with the clock, which is set by command 1.

When output ends, the interrupt request INT is output to the CPU.

Command 4 cancels the INT and sets/resets the two control ports (LATCH, OE).

If command 3 is executed immediately after command 4, the same data is output again.

Table 1 Function table

Command	Inputs											Outputs					Remark		
	Control inputs				Data inputs								SCLK	SDATA	INT	OE		LATCH	
	R	CS	C/D	WR	D7	D6	D5	D4	D3	D2	D1	D0							
—	0	X	X	X	X	X	X	X	X	X	X	X	0	0	1	1	0	Initialize	
—	1	1	X	X	X	X	X	X	X	X	X	X	* 1	* 1	* 1	* 2	* 2	Memory contents not changed	
1	1	0	1	φ	1	0	0	0	X	X	X	X	0	0	1	1	0	φ	Valid when D ₇ is high-level
					1	0	0	1	0	0	1	0	0	1	1	0	1/2 division of φ		
					1	0	1	0	0	1	0	0	1	1	0	0	1/4 division of φ		
					1	0	1	1	0	1	1	0	0	1	1	0	0	1/8 division of φ	
					1	1	0	0	0	0	0	1	1	0	0	0	1/16 division of φ		
2	1	φ	φ	0	X	X	X	X	0	X	X	0	0	0	1	1	0	WRITE MODE setting	WRITE MODE
					0	X	X	X	X	X	X	X	X	0	0	1	1	0	
3	* 5	X	X	X	X	X	X	X	X	X	X	X	* 3	* 4	1	1	0	SERIAL OUT MODE setting	SERI. OUT MODE
					X	X	X	X	X	X	X	X	X	X	X	* 3	* 4	1	
4	0	1	φ	0	X	X	X	X	1	D2	D1	X	0	0	1	D2	D1	set/reset the OE and LATCH, cancel INT	

- Note 1 :
- * 1 : The same operation as * 3 and * 4 in the SERIAL OUT mode. The output is not changed in other modes.
 - * 2 : The output is not chaged
 - * 3 : The φ division pulse, which is set by command 1 is output on WR rise
 - * 4 : SDATA (n) is output on SCLK fall (n-1).
 - * 5 : Indicates 1 when WR is 0. Don't care when WR is 1.
 - X : Don't care

PARALLEL-IN SERIAL-OUT DATA BUFFER WITH FIFO

BASIC OPERATION

Fig. 1 shows the basic operation flowchart. On the C/\bar{D} signal, data inputs $D_0 \sim D_7$ are switched among four commands and 8-bit parallel data. When C/\bar{D} is 1, the command is stored on the rise of \bar{WR} .

First, command 1 is stored. Command 1 sets the division ratio for clock input ϕ as 5 divisions of 1, 1/2, 1/4, 1/8 and 1/16. (The default division is 1.)

Then command 2 is stored. When command 2 is stored, 8-bit parallel data is written into the internal memory (FIFO), up to 63 bytes on the write cycle of the CPU.

When the write operation ends, command 3 is stored, and all data written in the internal memory is output as serial data (SDATA), starting with the LSB, in sync with the shift clock (SCLK output), which is set by command 1.

The SDATA changes on the fall of SCLK. If data output ends, an interrupt request is output to the CPU.

\bar{INT} is canceled by command 4 or by command 2 and 3. The command 4 sets/resets two control ports (LATCH, \bar{OE}) as well as canceling \bar{INT} .

If command 3 is executed without executing command 2 after Command 4, the same data is output again. If the repeat output is not required, return to command 2.

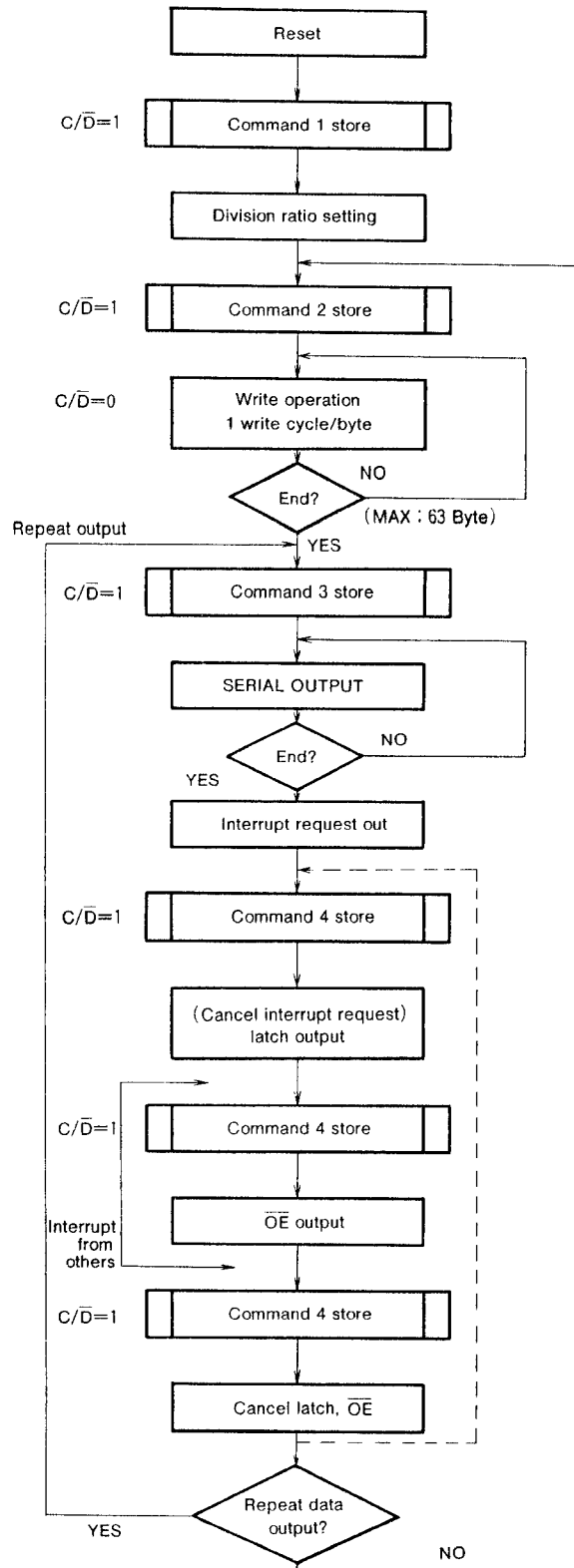


Fig. 1 Flowchart (Basic operation)

PARALLEL-IN SERIAL-OUT DATA BUFFER WITH FIFO

PIN DESCRIPTION

- RESET (Reset input)

When this is low-level, it clears the command and shift register and initializes the address of the internal memory (FIFO).

- ϕ (Clock input)

When the frequency of clock input ϕ is f_0 , the frequency f of shift clock output SCLK is given by the following equation.

$$f = (1/n) \cdot f_0 \quad (n=1, 2, 4, 8, 16)$$

- CS (chip select input)

When this is low-level, communication between the M66300 and the CPU becomes possible. When this is high-level, data from the CPU is ignored. However, data in the internal memory is maintained. In the serial output mode, data output operation continues and, as soon as it ends, an interrupt request instruction \overline{INT} is output. (\overline{INT} can be canceled only when \overline{CS} is low-level.) In other modes, output is maintained as it is.

- C/D (Command/data input)

The information on $D_0 \sim D_7$ is regarded as commands when this is high-level and is regarded as data when this is low-level.

- WR (Write input)

On WR rise, a command from the CPU is written into the command register and data is written into the internal memory. This input generates the serial data start signal, cancels \overline{INT} , and sets the 2-bit control ports (LATCH, \overline{OE}).

- SCLK (Shift clock output)

The clock frequency is determined by $D_6 \sim D_4$ when D_7 is 1, as shown in Table 2 and Fig. 2. Clock output starts on WR rise of command 3.

- SDATA (Shift data output)

All data written in the internal memory are output as serial data in sync with the SCLK.

- \overline{INT} (Interrupt request output)

When output of all data in the internal memory ends, a low-level signal is output.

- LATCH (Latch output)

- \overline{OE} (Output enable output)

These two outputs are set/reset by command 4 on WR rise. The signal was named after the IC (ex. M66310 or M66311) connected in the next stage, but it can be used freely for other applications.

INSTRUCTION SET

Four commands can be set by the 8-bit command words from the CPU.

- 1) Command 1 80₁₆~C0₁₆ (Note 2)
Division ratio setting
- 2) Command 2 00₁₆ (Note 3)
Write mode from the CPU to the internal memory is set.

- 3) Command 3 01₁₆ (Note 3)
Data output mode from the internal memory (FIFO) is set.
- 4) Command 4 08₁₆~0F₁₆ (Note 3)
Cancels the \overline{INT} and sets the two control ports (LATCH, \overline{OE}). (Note 4)

Note 2 : Lower byte can be 0~F.

3 : Upper byte can be 1~7.

4 : \overline{INT} can also be canceled by command 2 or 3.

Fig. 2 shows the method for determining the command word for the instruction set. When D_7 is 1, $D_3 \sim D_0$ are masked and when D_3 is 1, D_0 is masked.

Table 2 Division ratio setting

$D_7 \sim D_4$	Division
8 ₁₆	ϕ
9 ₁₆	1/2 of ϕ
A ₁₆	1/4 of ϕ
B ₁₆	1/8 of ϕ
C ₁₆	1/16 of ϕ

Table 3 OE, LATCH setting

$D_3 \sim D_0$	\overline{OE}	LATCH	\overline{INT} cancellation
8 ₁₆ , 9 ₁₆	0	0	canceled ↓
A ₁₆ , B ₁₆	0	1	
C ₁₆ , D ₁₆	1	0	
E ₁₆ , F ₁₆	1	1	

PARALLEL-IN SERIAL-OUT DATA BUFFER WITH FIFO

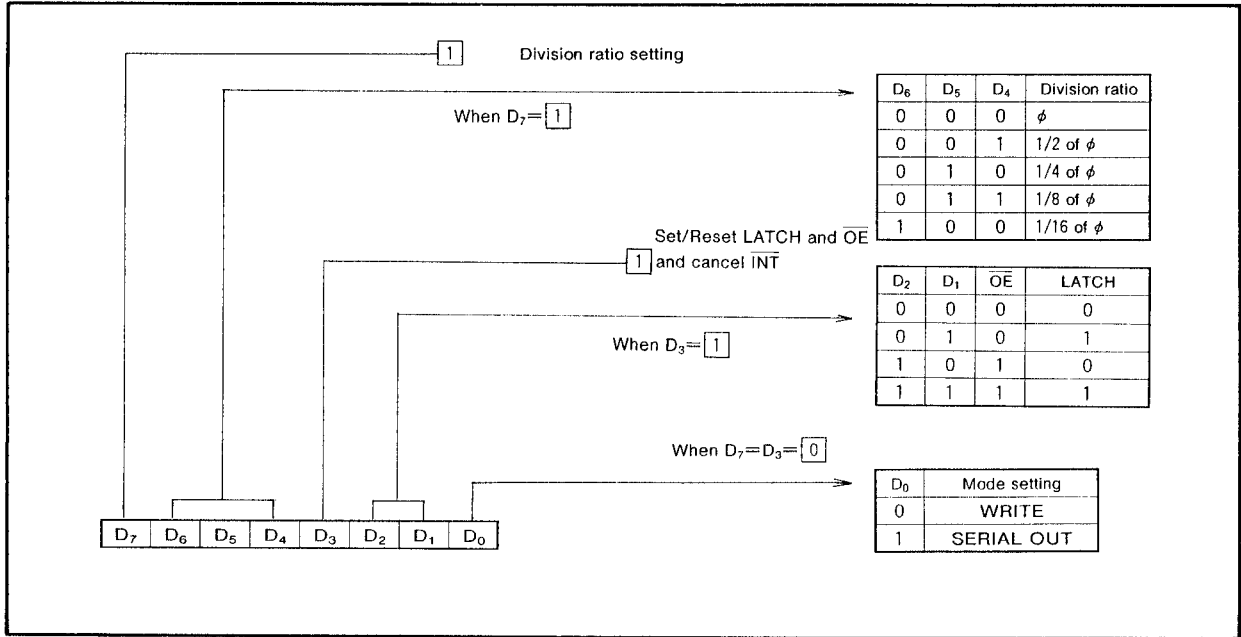
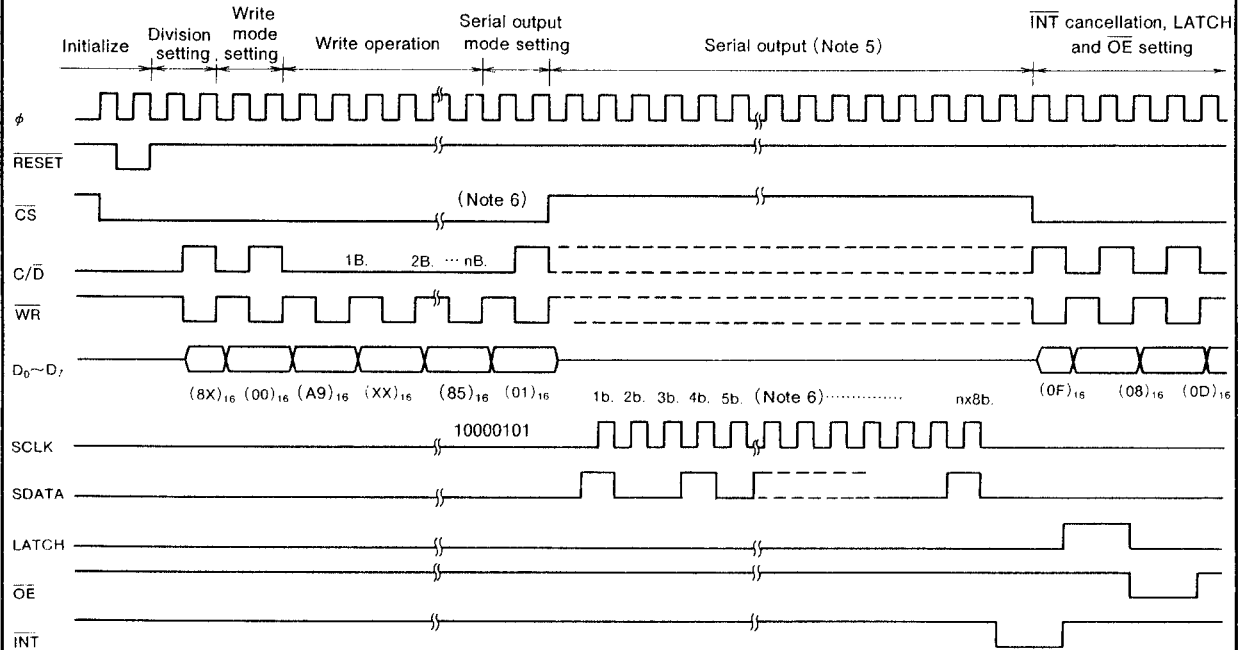


Fig. 2 Instruction set

EXAMPLE OF TIME CHART



Note 5 : Always maintain \overline{WR} at high-level when \overline{CS} is low-level.

6 : B.=Byte, b.=bit

7 : ϕ need not be the CPU signal. (ϕ and \overline{WR} need not be synchronous.)

8 : ϕ indicates the value when division ratio is set 1. If the division ratio is other than 1, a similar time chart is obtained if ϕ is regarded as the waveform divided.

PARALLEL-IN SERIAL-OUT DATA BUFFER WITH FIFO

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-0.5~+7	V
V_I	Input voltage		-0.5~+ V_{CC} +0.5	V
V_O	Output voltage		-0.5~+ V_{CC} +0.5	V
P_d	Power dissipation		500	mW
T_{stg}	Storage temperature		-65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -10 \sim +75^\circ\text{C}$)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
GND	Supply voltage			0		V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		-10		75	°C

ELECTRICAL CHARACTERISTICS ($T_a = -10 \sim +75^\circ\text{C}$, $V_{CC} = 5 \text{ V} \pm 10\%$, $GND = 0 \text{ V}$)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage	Inputs other than $\overline{\text{RESET}}$	2			V
V_{IL}	Low-level input voltage				0.8	V
V_{T+}	Positive input threshold voltage	$\overline{\text{RESET}}$			2.4	V
V_{T-}	Negative input threshold voltage		0.6			V
$V_{T+} - V_{T-}$	Hysteresis width		0.2	0.8		V
V_{OH}	High-level output voltage	INT	$V_{CC} - 0.80$	$V_{CC} - 0.30$	$V_{CC} - 0.40$	V
		Output pin other than INT				
V_{OL}	Low-level output voltage	INT				V
		Output pin other than INT				
I_{CC}	Supply current	$V_I = V_{CC}$ or GND		20	50	mA
I_{IH}	High-level input current	$V_I = V_{CC}$			+1	μA
I_{IL}	Low-level input current	$V_I = 0 \text{ V}$			-1	μA
C_I	Input capacitance			5	10	pF

Note 9 : The current flowing into the IC is positive (no sign).

PARALLEL-IN SERIAL-OUT DATA BUFFER WITH FIFO

TIMING REQUIREMENTS ($T_a = -10 \sim +75^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $\text{GND} = 0\text{V}$)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(\phi)}$	Clock pulse width		50			ns
$t_{W(\bar{W})}$	Write pulse width		100			ns
$t_{W(\bar{R})}$	Reset pulse width		100			ns
$t_{SU(D-\bar{W})}$	Data setup time before write		50			ns
$t_H(\bar{W}-D)$	Data hold time after write		0			ns
$t_{SU(A-\bar{W})}$	Address setup time before write		0			ns
$t_H(\bar{W}-A)$	Address hold time after write		0			ns
$t_{rec}(\bar{W})$	Write recovery time		100			ns
$t_{rec}(\overline{\text{INT}}-\bar{W})$	Write recovery time after INT		100			ns
$t_{rec}(\bar{R}-\bar{W})$	Write recovery time after reset		100			ns

Note 10 : Increase of the input rise time (t_r) and fall time (t_f) of clock input ϕ may cause misoperation.
 t_r, t_f : These are recommended to be 20ns or less.

SWITCHING CHARACTERISTICS ($T_a = -10 \sim +75^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_C(\phi)$	Clock Cycle		100			ns
$t_{PLH}(\bar{W}-\overline{\text{INT}})$	Propagation time between write and $\overline{\text{INT}}$	$C_L = 50\text{pF}$		30	100	ns
$t_{PHI}(\bar{R}-\overline{\text{INT}})$	Propagation time between $\overline{\text{RESET}}$ and $\overline{\text{INT}}$			20	100	ns
$t_{PLH}(\bar{W}-\overline{\text{OE}})$	Propagation time between write and $\overline{\text{OE}}$			20	100	ns
$t_{PHL}(\bar{W}-\overline{\text{OE}})$				25	100	ns
$t_{PLH}(\bar{W}-\text{LATCH})$	Propagation time between write and LATCH			20	100	ns
$t_{PHL}(\bar{W}-\text{LATCH})$				25	100	ns
$t_{PLH}(\bar{W}-\text{SCLK})$	Propagation time between write and SCLK		$1 \times T$	—	$2 \times T + 100$	ns
$t_{PLH}(\phi-\text{SCLK})$	Propagation time between ϕ and SCLK	$C_L = 150\text{pF}$		35	100	ns
$t_{PLH}(\phi-\text{SDATA})$	Propagation time between ϕ and SDATA			30	100	ns
$t_{PHL}(\phi-\text{SDATA})$				30	100	ns
$t_{PHL}(\phi-\overline{\text{INT}})$	Propagation time between ϕ and $\overline{\text{INT}}$			30	100	ns
$t_{PLH}(\bar{R}-\overline{\text{OE}})$	Propagation time between $\overline{\text{RESET}}$ and $\overline{\text{OE}}$			20	100	ns
$t_{PHL}(\bar{R}-\text{LATCH})$	Propagation time between $\overline{\text{RESET}}$ and LATCH			25	100	ns
t_{TLH}	Low-to high-level output transition time ($\overline{\text{INT}}$)	$C_L = 50\text{pF}$		10	25	ns
t_{THL}	High-to low-level output transition time ($\overline{\text{INT}}$)			6	25	ns
t_{TLH}	Low-to high-level output transition time (SCLK, SDATA, $\overline{\text{OE}}$, LATCH)			10	25	ns
t_{THL}	High-to low-level output transition time (SCLK, SDATA, $\overline{\text{OE}}$, LATCH)	$C_L = 150\text{pF}$		7	25	ns

Note 11 : $T = (1/\phi(f_0)) \times (1/\text{division ratio})\text{ns}$

12 : AC test waveform

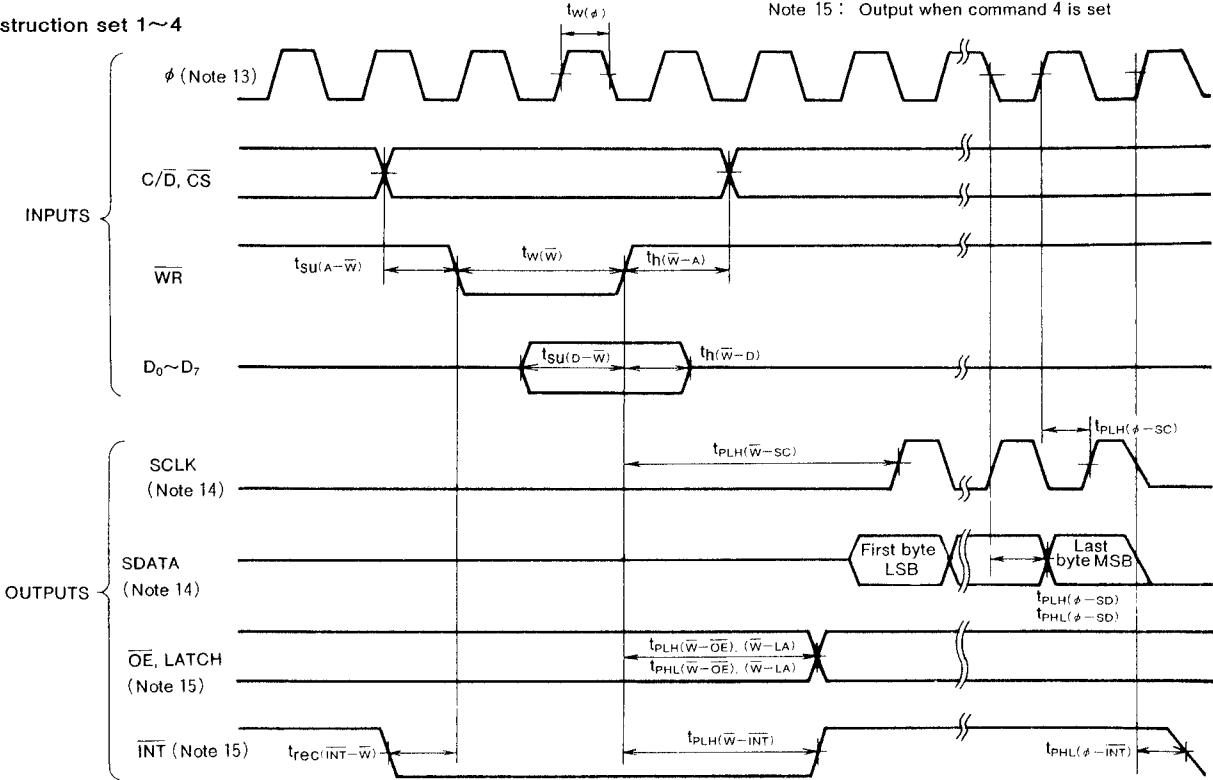
Input pulse level	0~3V
Input pulse rise time	6ns
Input pulse fall time	6ns
Reference voltage	
Input voltage	1.3V
Output voltage	1.3V

PARALLEL-IN SERIAL-OUT DATA BUFFER WITH FIFO

TIMING DIAGRAM

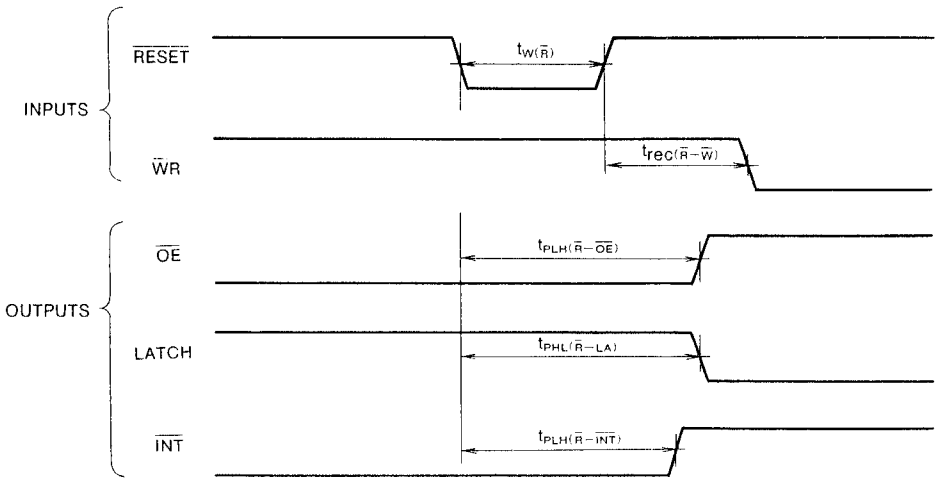
Instruction set 1~4

Note 14 : Output when command 3 is set
 Note 15 : Output when command 4 is set



Note 13 : The timing diagram when division ratio is set (1/2, 1/4, 1/8, 1/16) is regarded as the waveform as divided by ϕ . There are specific ϕ inputs for switching from each ϕ state.

Timing diagram when RESET



WR recovery time other than data reading



PARALLEL-IN SERIAL-OUT DATA BUFFER WITH FIFO

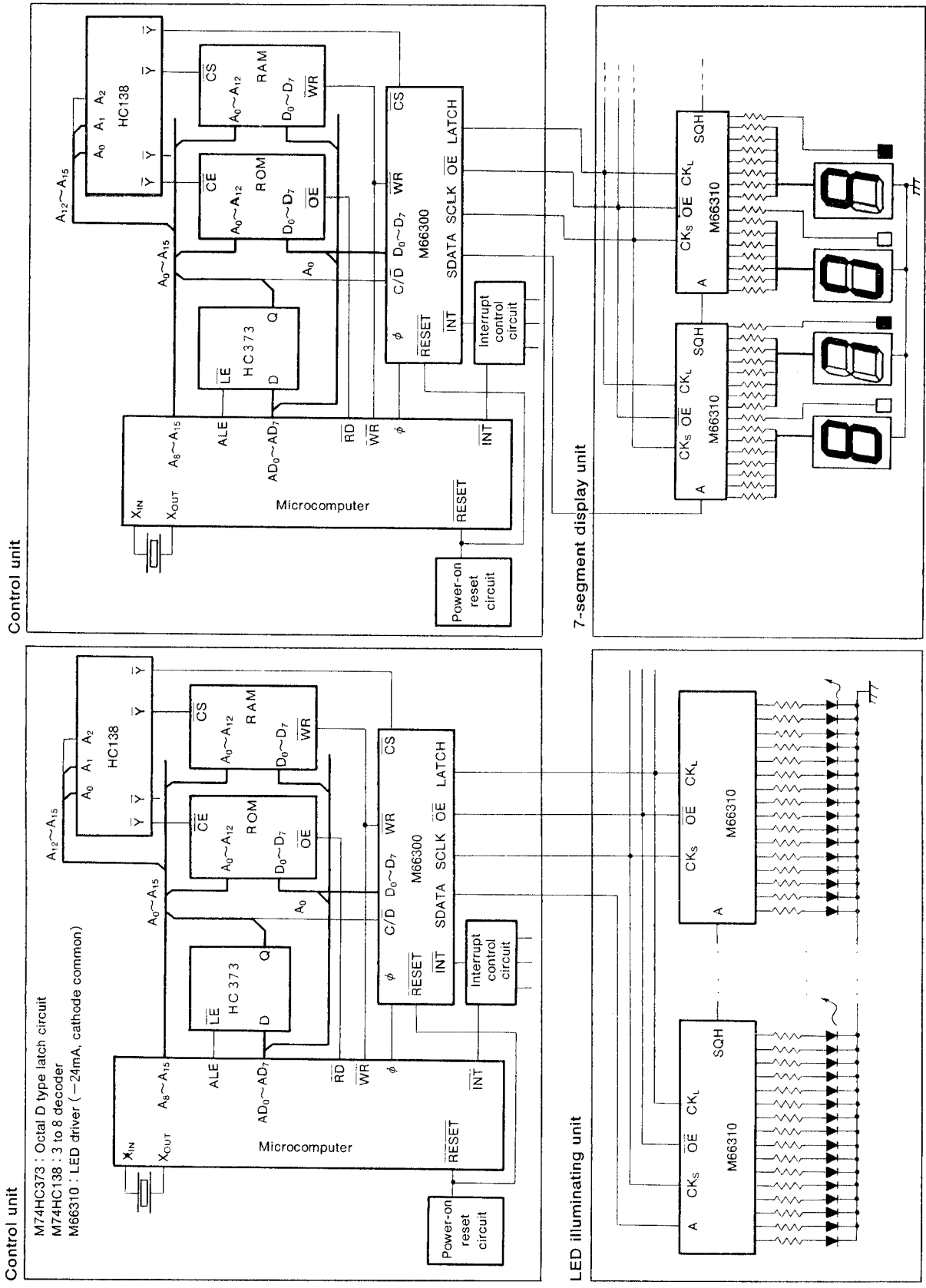


Fig. 4 Application example 2 (Panel display circuit)

Fig. 3 Application example 1 (PPC copying machine eraser circuit)

PARALLEL-IN SERIAL-OUT DATA BUFFER WITH FIFO

TYPICAL CHARACTERISTICS (24mA OUTPUT PIN)

