

# M64898GP

## PLL FREQUENCY SYNTHESIZER WITH DC-DC CONVERTER FOR PC

### DESCRIPTION

The M64898GP is a semiconductor integrated circuit consisting of PLL frequency synthesizer for TV/VCR /PC.

It contains the prescaler with operating up to 1.3GHz, 4 band drivers and DC-DC converter for Tuning voltage.

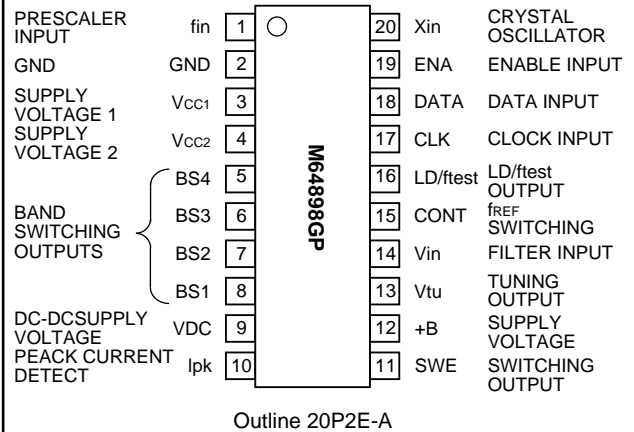
### FEATURES

- Built-in DC-DC converter for Tuning voltage
- 4 integrated PNP band drivers (I<sub>o</sub>=30mA, V<sub>sat</sub>=0.2V typ@V<sub>cc1</sub> to 10V)
- Built-in prescaler with input amplifier (max=1.3GHz)
- PLL lock/unlock status display output (Built-in pull up resistor)
- X'tal 4MHz is used to realize 3 type of tuning steps (Divider ratio 1/512, 1/640, 1/1024)
- Software compatible with M64892/M64893
- Automatic switching of tuning step according to the number of data bits (62.5kHz at 18bits, 32.25kHz at 19bits)
- Built-in Power on reset system
- Small Package(SSOP)

### APPLICATION

PC, TV, VCR tuners

### PIN CONFIGURATION (TOP VIEW)



### RECOMMENDED OPERATING CONDITION

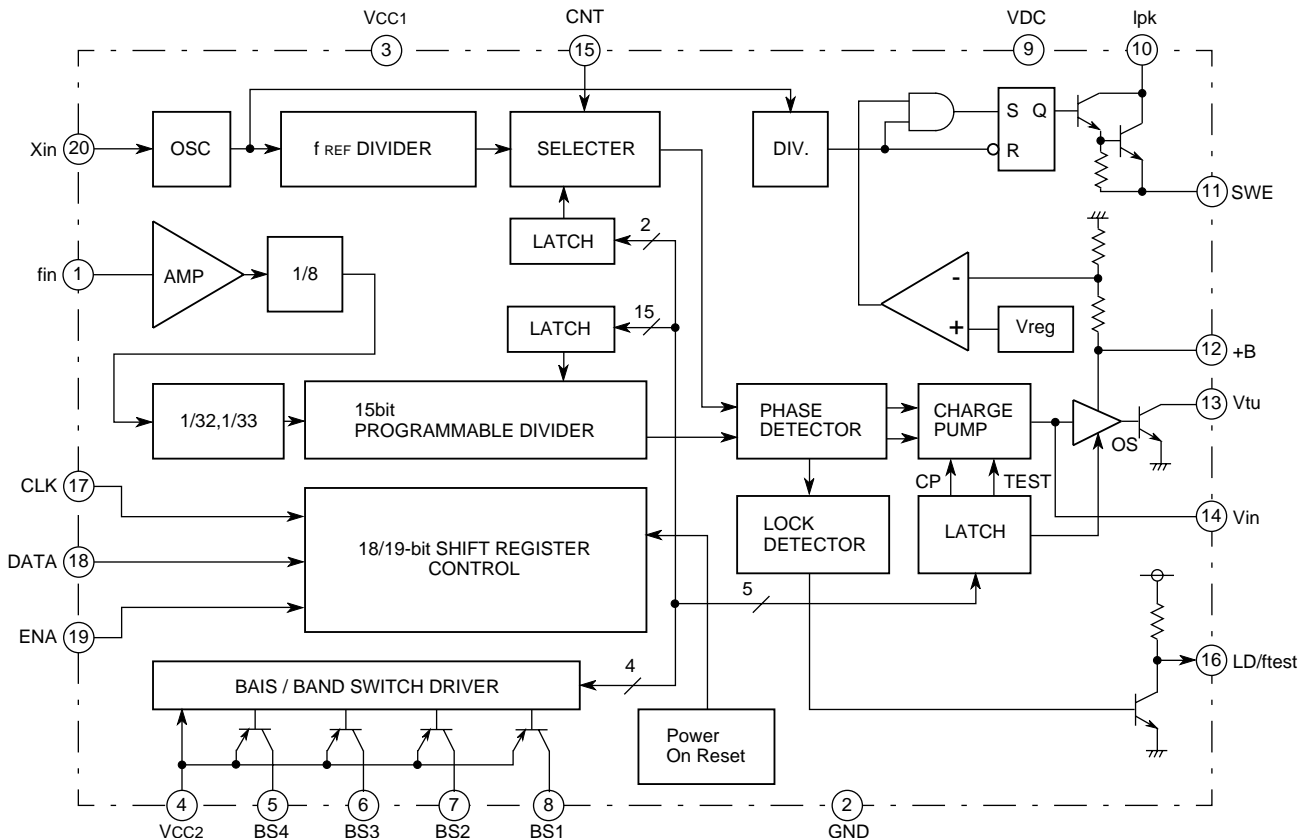
Supply voltage range.....V<sub>cc1</sub>=4.5 to 5.5V

V<sub>cc2</sub>=V<sub>cc1</sub> to 10V

Rated supply voltage.....V<sub>cc1</sub>=5V

V<sub>cc2</sub>=V<sub>cc1</sub>

### BLOCK DIAGRAM



**PLL FREQUENCY SYNTHESIZER WITH DC-DC CONVERTER FOR PC****DESCRIPTION OF PIN**

Pin No.	Symbol	Pin name	Function
1	f in	Prescaler input	Input for the VCO frequency.
2	GND	GND	Ground to 0V.
3	Vcc1	Power supply voltage 1	Power supply voltage terminal. 5.0V±0.5V
4	Vcc2	Power supply voltage 2	Power supply for band switching, Vcc1 to 10V
5	BS4	Band switching outputs	PNP open collector method is used. When the band switching data is "H", the output is ON. When it is "L", the output is OFF.
6	BS3		
7	BS2		
8	BS1		
9	VDC	DC-DC power supply voltage	DC-DC power supply voltage terminal. 5.0V±0.5V
10	l <sub>pk</sub>	Peack current detect	When potential difference with VDC terminal becomes more than 0.33V by current limiting detector of DC-DC converter, the listing rises with off.
11	SWE	Switching output	DC-DC converter oscillator output.
12	+B	Power supply voltage	Power supply voltage for turning voltage.
13	V <sub>tu</sub>	Tuning output	This supplies the tuning voltage.
14	V <sub>in</sub>	Filter input (Charge pump output)	This is the output terminal for the LPF input and charge pump output. When the phase of the programmable divider output (f 1/N) is ahead compared to the reference frequency (f <sub>REF</sub> ), the "source" current state becomes active. If it is behind, the "sink" current becomes active. If the phases are the same, the high impedance state becomes active.
15	LD/test	Lock detect /Test port	Lock detector output. When loop of phase locked loop locked it, it rises with "H" level in "L" level or unlock. In control byte data input, the programmable freq. divider output and reference freq. output is selected by the test mode.
16	CONT	f <sub>REF</sub> Switchi	Set up reference frequency divider ratio. In "L" level, set it up in 1/640(19Bit) in setting "opening" in 1/1024(19Bit) or 1/512 (18Bit).
17	CLOCK	Clock input	Data is read into the shift register when the clock signal falls.
18	DATA	Data input	Input for band SW and programmable freq. divider set up.
19	ENABLE	Enable input	This is normally at a "L". When this is at "H", data and clock signals are received. Data is read into the latch when the enable signal after the 18th signal of the clock signal falls or when the 19th pulse of the clock signal falls.
20	X in	This is connected to the crystal oscillator.	4.0MHz crystal oscillator is connected.

**ABSOLUTE MAXIMUM RATINGS** (T<sub>a</sub>=-20°C to +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC1</sub>	Supply voltage 1	Pin3	6.0	V
V <sub>CC2</sub>	Supply voltage 2	Pin4	10.8	V
V <sub>I</sub>	Input voltage	Not to exceed V <sub>CC1</sub>	6.0	V
V <sub>O</sub>	Output voltage	f <sub>REF</sub> output	6.0	V
V <sub>BSOFF</sub>	Voltage applied when the band output is OFF		10.8	V
I <sub>BSON</sub>	Band output current	per 1 band output circuit	40.0	mA
t <sub>BSON</sub>	ON the time when the band output is ON	40mA per 1 band output circuit 3circuits are pn at same time,	10	sec
P <sub>d</sub>	Power dissipation	T <sub>a</sub> =75°C	255	mW
T <sub>opr</sub>	Operating temperature		-20 to +75	°C
T <sub>stg</sub>	Storage temperature		-40 to +125	°C

## PLL FREQUENCY SYNTHESIZER WITH DC-DC CONVERTER FOR PC

## RECOMMENDED OPERATING CONDITIONS (Ta=-20°C to +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
VCC1	Supply voltage 1	Pin3	4.5 to 5.5	V
VCC2	Supply voltage 2	Pin4	VCC1 to 10.0	V
fopr1	Operating frequency (1)	Crystal oscillation circuit	4.0	V
fopr2	Operating frequency (2)		80 to 1300	MHz
IBDL	Band output current 5 to 8	Normally 1 circuit is on. 2 circuits on at the same time is max. It is prohibited to have 3 or more circuits turned on at the same time.	0 to 30	mA

## ELECTRICAL CHARACTERISTICS (Ta=-20°C to +75°C, unless otherwise noted, VCC1=5.0V, VCC2=9.0V)

Symbol	Parameter	Test pin	Test conditions	Limits			Unit	
				Min.	Typ.	Max.		
V <sub>IH</sub>	Input terminals	"H" input voltage	17 to 19	3.0	-	V <sub>CC1</sub> +0.3	V	
V <sub>IL1</sub>		"L" input voltage	15	-	-	0.4	V	
V <sub>IL2</sub>		"L" input voltage	17 to 19	-	-	1.5	V	
I <sub>IH</sub>		"H" input current	17 to 19	V <sub>CC1</sub> =5.5V, V <sub>i</sub> =4.0V	-	-	10	μA
I <sub>IL1</sub>		"L" input current	15	V <sub>CC1</sub> =5.5V, V <sub>i</sub> =0V	-	-50	-80	μA
I <sub>IL2</sub>		"L" input current	17, 19	V <sub>CC1</sub> =5.5V, V <sub>i</sub> =0.5V	-	-6	-10	μA
I <sub>IL3</sub>		"L" input current	18	V <sub>CC1</sub> =5.5V, V <sub>i</sub> =0.5V	-	-18	-30	μA
V <sub>OH</sub>	Lock output	"H" output voltage	16	V <sub>CC1</sub> =5.5V	5.0	-	-	V
V <sub>OL</sub>		"L" output voltage	16	V <sub>CC1</sub> =5.5V	-	0.3	0.5	V
V <sub>BS</sub>	Band SW	Output voltage	5 to 8	V <sub>CC2</sub> =9V, I <sub>o</sub> =-30mA	11.6	11.8	-	V
I <sub>olk1</sub>		Leak current	5 to 8	V <sub>CC2</sub> =9V, Band SW is OFF V <sub>o</sub> =0V	-	-	-10	μA
V <sub>toH</sub>	Tuning output	Output voltage "H"	13	+B=31V	30.5	-	-	V
V <sub>toL</sub>		Output voltage "L"	13	+B=31V	-	0.2	0.4	V
I <sub>cpo</sub>	Charge pump	"H" output current	14	V <sub>CC1</sub> =5.0V, V <sub>o</sub> =2.5V	-	±270	±370	μA
I <sub>cpLK</sub>		Leak current	14	V <sub>CC1</sub> =5.0V, V <sub>o</sub> =2.5V	-	-	±50	nA
I <sub>CC1</sub>	Supply current 1	3	V <sub>CC1</sub> =5.5V	-	20	30	mA	
I <sub>CC2A</sub>	Supply current 2	4 circuits OFF	4	V <sub>CC2</sub> =9V	-	-	0.3	mA
I <sub>CC2B</sub>		1 circuit ON, Output open	4	V <sub>CC2</sub> =9V	-	4.0	6.0	mA
I <sub>CC2C</sub>		Output current 30mA	4	V <sub>CC2</sub> =9V, I <sub>o</sub> =-30mA	-	34.0	36.0	mA
DC-DC Converter								
I <sub>CCdc</sub>	Supply current (action)	9	V <sub>CC1</sub> =5.5V	-	1.3	3.0	mA	
V <sub>do</sub>	Output voltage	12	V <sub>CC1</sub> =5.5V	28	31	35	V	
f <sub>osc</sub>	OSC frequency	11	V <sub>CC1</sub> =5.5V	-	571	-	kHz	
V <sub>ipk</sub>	Current limit detect voltage	10	V <sub>CC1</sub> =5.5V	-	330	-	mV	

The typical values are at V<sub>CC1</sub>=5.0V, V<sub>CC2</sub>=9.0V, Ta=+25°C.

**PLL FREQUENCY SYNTHESIZER WITH DC-DC CONVERTER FOR PC****SWITCHING CHARACTERISTICS** ( $T_a = -20^\circ\text{C}$  to  $+75^\circ\text{C}$ , unless otherwise noted,  $V_{CC1} = 5.0\text{V}$ ,  $V_{CC2} = 9.0\text{V}$ )

Symbol	Parameter	Test pin	Test conditions	Limits			Unit	
				Min.	Typ.	Max.		
f <sub>opr</sub>	Prescaler operating frequency	1	$V_{CC1} = 4.5$ to $5.5\text{V}$ $V_{in} = V_{inmin}$ to $V_{inmax}$	80	–	1300	MHz	
V <sub>in</sub>	Operating input voltage	1	$V_{CC1} = 4.5$ to $5.5\text{V}$	80 to 100MHz	-24	–	4	dBm
				100 to 950MHz	-27	–	4	
				950 to 1300MHz	-15	–	4	
t <sub>PWC</sub>	Clock pulse width	17	$V_{CC1} = 4.5$ to $5.5\text{V}$	1	–	–	$\mu\text{s}$	
t <sub>SU (D)</sub>	Data setup time	18	$V_{CC1} = 4.5$ to $5.5\text{V}$	2	–	–	$\mu\text{s}$	
t <sub>H (D)</sub>	Data hold time	18	$V_{CC1} = 4.5$ to $5.5\text{V}$	1	–	–	$\mu\text{s}$	
t <sub>SU (E)</sub>	Enable setup time	18	$V_{CC1} = 4.5$ to $5.5\text{V}$	3	–	–	$\mu\text{s}$	
t <sub>H (E)</sub>	Enable hold time	18	$V_{CC1} = 4.5$ to $5.5\text{V}$	3	–	–	$\mu\text{s}$	
t <sub>INT</sub>	Enable data interval time	19, 18	$V_{CC1} = 4.5$ to $5.5\text{V}$	1	–	–	$\mu\text{s}$	
t <sub>r</sub>	Rise time	17, 18, 19	$V_{CC1} = 4.5$ to $5.5\text{V}$	–	–	1	$\mu\text{s}$	
t <sub>f</sub>	Fall time	17, 18, 19	$V_{CC1} = 4.5$ to $5.5\text{V}$	–	–	1	$\mu\text{s}$	
t <sub>BT</sub>	Next enable prohibit time	19	$V_{CC1} = 4.5$ to $5.5\text{V}$	5	–	–	$\mu\text{s}$	
t <sub>BCL</sub>	Next clock prohibit time	17, 19	$V_{CC1} = 4.5$ to $5.5\text{V}$	5	–	–	$\mu\text{s}$	

**PLL FREQUENCY SYNTHESIZER WITH DC-DC CONVERTER FOR PC**

**METHOD OF SETTING DATA**

The programmable divider ratio uses 15bits. Setting up the band switching output uses 4bits.

The test mode data uses 8bits. The total bits used is 27bits. Data is read in when the enable signal is "H" and the clock signal falls.

The band switching data is read in at the 4th pulse of the clock signal. The programmable counter data is read into the latch by the fall of the enable signal after the 18th pulse of the clock signal or the fall of the 19th pulse of the clock signal. When the enable signal goes to "L" before the 18th pulse of the enable signal, only the band SW data is updated and other data is ignored.

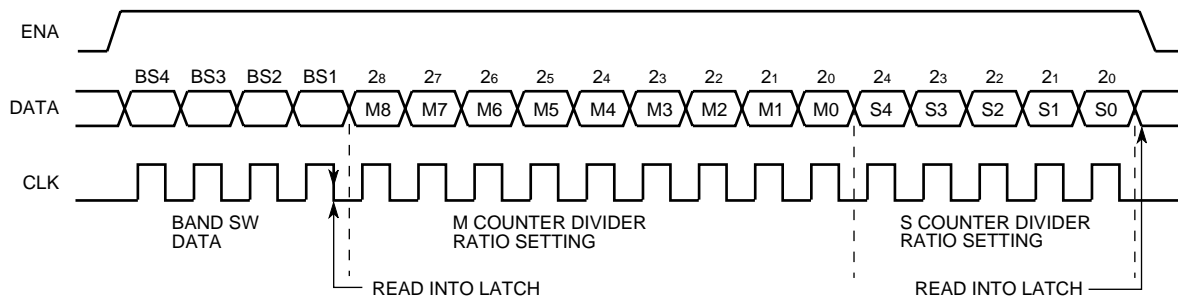
Automatic judgment facility comes being it, and, as for Shift resistor, CONT terminal rises by 18/19 bits at the time of "L". At the time of data of 18 bits, M9 bit of Programmable divider is done reset of, and it is established in reference frequency divider ratio 1/512.

At the time of 19 bits,reference frequency divider ratio is established in 1/1024.

When reference frequency divider ratio was established in 1/640 by 19 bits at the time of "opening" CONT terminal, and it became "L" before 19 pulse enable signal, only band SW data are renewed, and other data are ignored.

(1) Transfer of the 18th bit data (CONT terminal is "L" )

Data is latched by the fall of the enable signal after the 18th clock signal. At this time, the divider of the 1/512 of the reference frequency is used.

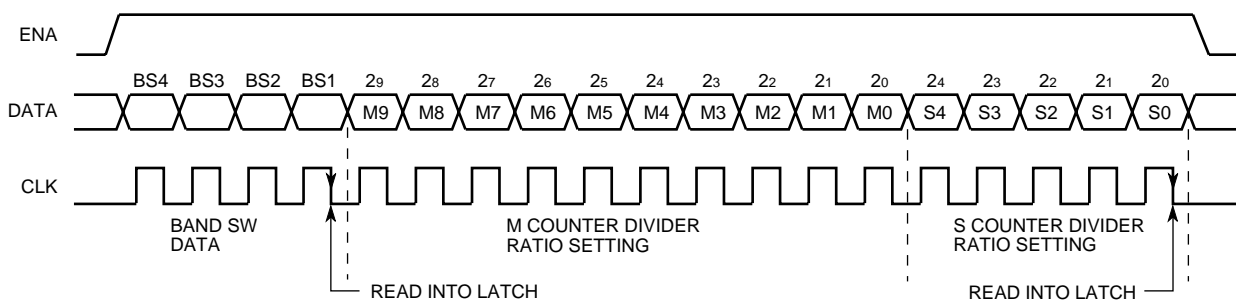


(2) Transfer of the 19th bit data (CONT terminal is "L" or "open")

The data is latched at the 19th pulse of the clock signal. Reference frequency divider ratio is established in 1/1024 in case of "L" CONT terminal at this time. Reference frequency divider ratio is established in 1/640 in case of "opening" CONT terminal.

Invalid the clock signal after 19th pulse.

Notice) When CONT terminal is "L", to change reference frequency, set up as ENA in "L" after 19th pulse of clock signal by all means.



**PLL FREQUENCY SYNTHESIZER WITH DC-DC CONVERTER FOR PC**

**HOW TO SET THE DIVIDING RATIO OF THE PROGRAMMABLE DIVIDER**

(1) Transfer of the 18th bit data (CONT terminal is "L" )

Total divider N is given by the following formulas in addition to the prescaler used in the previous stage.

$$N = 8 \cdot (32M + S)$$

M : 9 bit main counter divider  
S : 5 bit swallow counter divider

The M and S counters are binary the possible ranges of divider are as follows.

$$32 \leq M \leq 511$$

$$0 \leq S \leq 31$$

Therefore, the range of divider N is 8,192 to 131,064.

The tuning frequency  $f_{VCO}$  is given in the following equations.

$$f_{VCO} = f_{REF} \times N$$

$$= 7.8125 \times 8 \times (32M + S)$$

$$= 62.5 \times (32M + S) \text{ [kHz]}$$

Therefore, the tuning frequency range is 64MHz to 1023.9375MHz.

(2) Transfer of the 19th bit data (CONT terminal is "L" )

Total divider N is given by the following formulas in addition to the prescaler used in the previous stage.

$$N = 8 \cdot (32M + S)$$

M : 10 bit main counter divider  
S : 5 bit swallow counter divider

The M and S counters are binary the possible ranges of divider are as follows.

$$32 \leq M \leq 1023$$

$$0 \leq S \leq 31$$

Therefore, the range of divider N is 8,192 to 262,136.

The tuning frequency  $f_{VCO}$  is given in the following equations.

$$f_{VCO} = f_{REF} \times N$$

$$= 3.90625 \times 8 \times (32M + S)$$

$$= 31.25 \times (32M + S) \text{ [kHz]}$$

Therefore, the tuning frequency range is 32MHz to 1023.96875 MHz.

(3) Transfer of the 19th bit data (CONT terminal is "open")

Total divider N is given by the following formulas in addition to the prescaler used in the previous stage.

$$N = 8 \cdot (32M + S)$$

M : 10 bit main counter divider  
S : 5 bit swallow counter divider

The M and S counters are binary the possible ranges of divider are as follows.

$$32 \leq M \leq 1023$$

$$0 \leq S \leq 31$$

Therefore, the range of divider N is 8,192 to 262,136.

The tuning frequency  $f_{VCO}$  is given in the following equations.

$$f_{VCO} = f_{REF} \times N$$

$$= 6.25 \times 8 \times (32M + S)$$

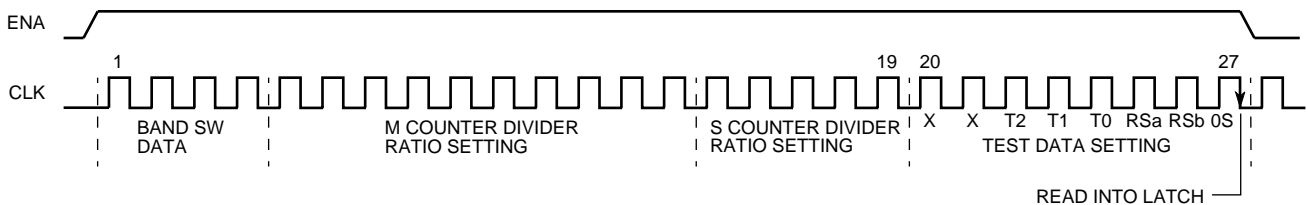
$$= 50.0 \times (32M + S) \text{ [kHz]}$$

But, the tuning frequency range is 51.2MHz to 1300MHz from the maximum prescaler operating frequency.

**TEST MODE DATA SET UP METHOD**

The data for the test mode uses 20 to 27bits. Data is latched when the 27th clock signal falls.

(1) When transferring 3-wire 27 bit data



(2) Test Mode Bit Set Up

- X : Random, 0 or 1. normal "0"
- T0, T1, & T2 : Set up test modes
- RSa, RSa : Set the frequency divider of the reference frequency
- OS : Set up the tuning amplifier

**PLL FREQUENCY SYNTHESIZER WITH DC-DC CONVERTER FOR PC**

**Setting up for the test mode**

T2	T1	T0	Charge pump	12 pin output	Mode
0	0	X	Normal operation	LD	Normal operation
0	1	X	High impedance	LD	Test mode
1	1	0	Sink	LD	Test mode
1	1	1	Source	LD	Test mode
1	0	0	High impedance	fREF	Test mode
1	0	1	High impedance	f1/N	Test mode

**Set up for the reference Frequency divider ratio**

RSa	RSb	Divider ratio
1	1	1/512
0	1	1/1024
X	0	1/640

**Set up the tuning amplifier**

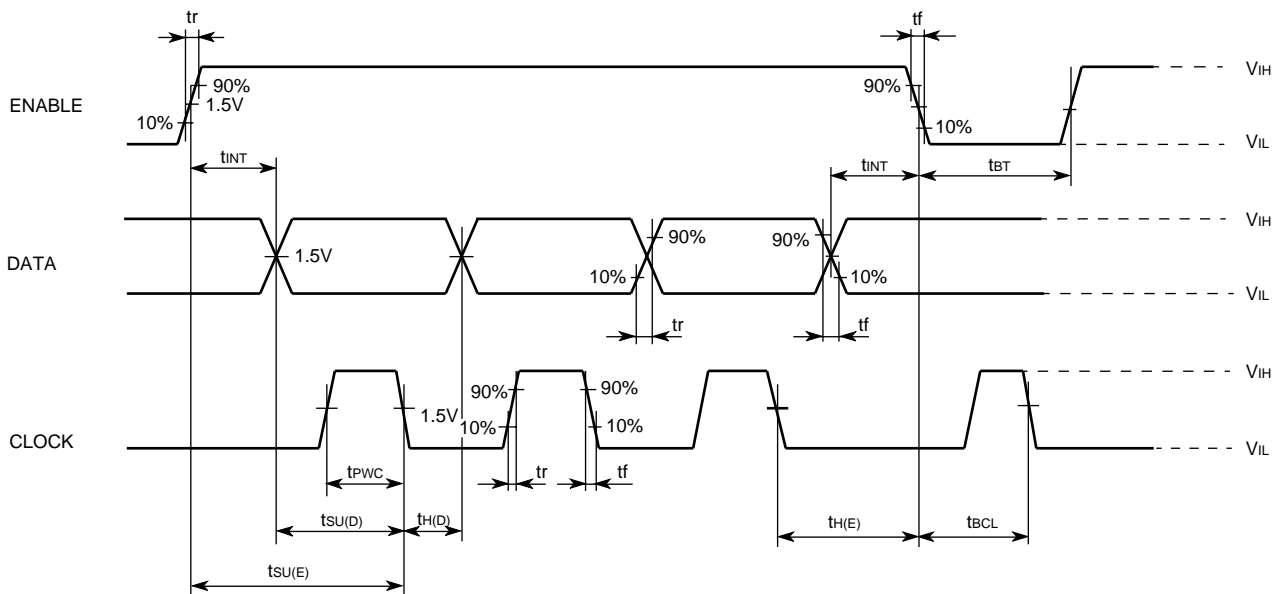
OS	Tuning voltage output	Mode
0	ON	Normal
1	OFF	Test

**Power on reset operation  
(Initial state the power is turned ON)**

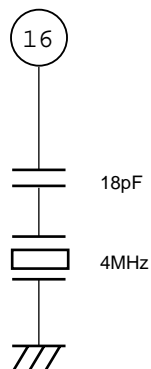
- BS4 to BS1 : OFF
- Charge pump : High impedance
- Tuning amplifier : OFF
- Charge pump current : 270μA \*
- Frequency divider ratio : 1/1024
- Lock detect : H

\* Charge pump current is replaced by 70μA when locks it by automatic change facility.

**TIMING DIAGRAM**



**CRYSTAL OSCILLATOR CONNECTION DIAGRAM**



Crystal oscillator characteristics  
Actual resistance : less than 300Ω  
Load capacitance : 20pF

PLL FREQUENCY SYNTHESIZER WITH DC-DC CONVERTER FOR PC

APPLICATION EXAMPLE

