

M62371GP

3V TYPE 8-BIT 36CH SELECTOR SW BUILT-IN D-A CONVERTER WITH BUFFER AMPLIFIERS

DESCRIPTION

The M62371GP is a CMOS semiconductor IC, containing 36 channels of 8-bit D-A converters. It is operable with a low supply voltage between 2.7 ~ 3.6V, and is easy to use due to serial data input, and 3-pin(DI, CLK, LD)connection with microcomputer. The IC also contains Do pin terminal, enabling cascade connection, and therefore is suitable for automatic control in combination with a microcomputer. (M62371GP is an advanced product of M62370GP on its buffer amp. drivability.)

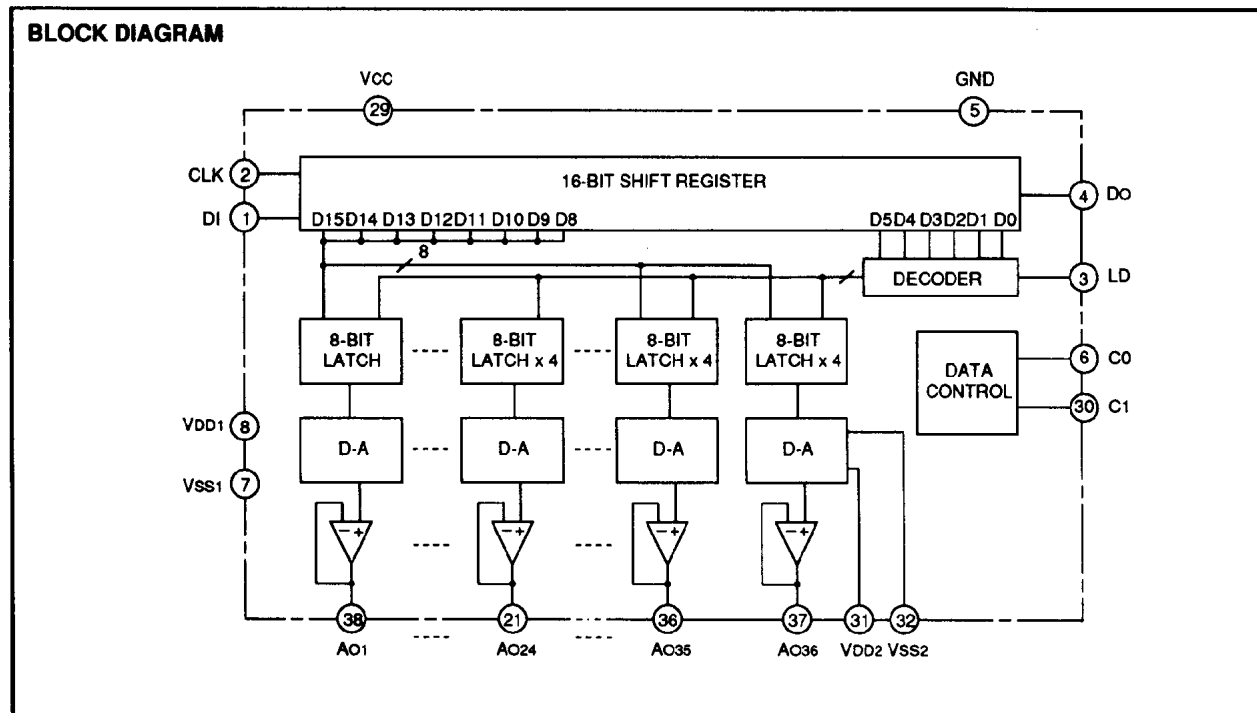
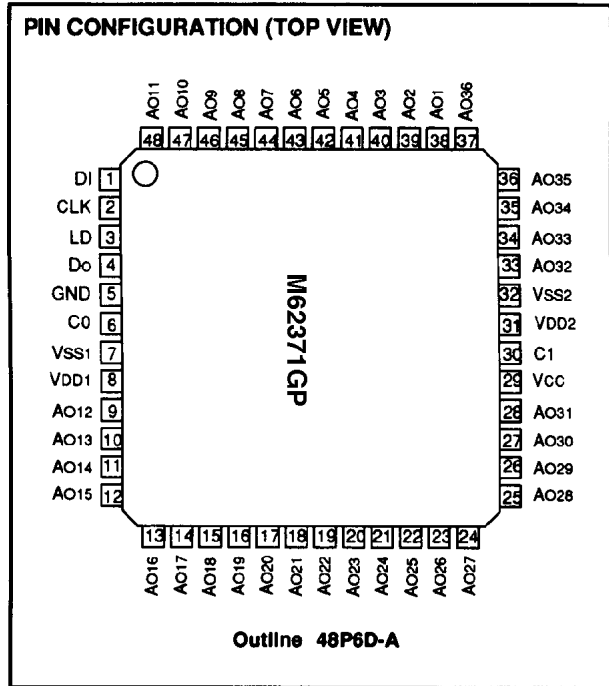
FEATURES

- Operable with a low voltage between 2.7 ~ 3.6V
- 16-bit serial data input(connected via 3 pins:DI, CLK, LD)
- 36 channels built-in of 8-bit D-A converter
- 6 channels of D-A converters capable of selecting and outputting 4 data stored in each converter, through 2 control terminals

APPLICATION

Digital-analog conversion in industrial or home-use electronic equipment

Automatic control in combination with EEPROM and microcomputer (Substitute for conventional semi-fixed resistor)



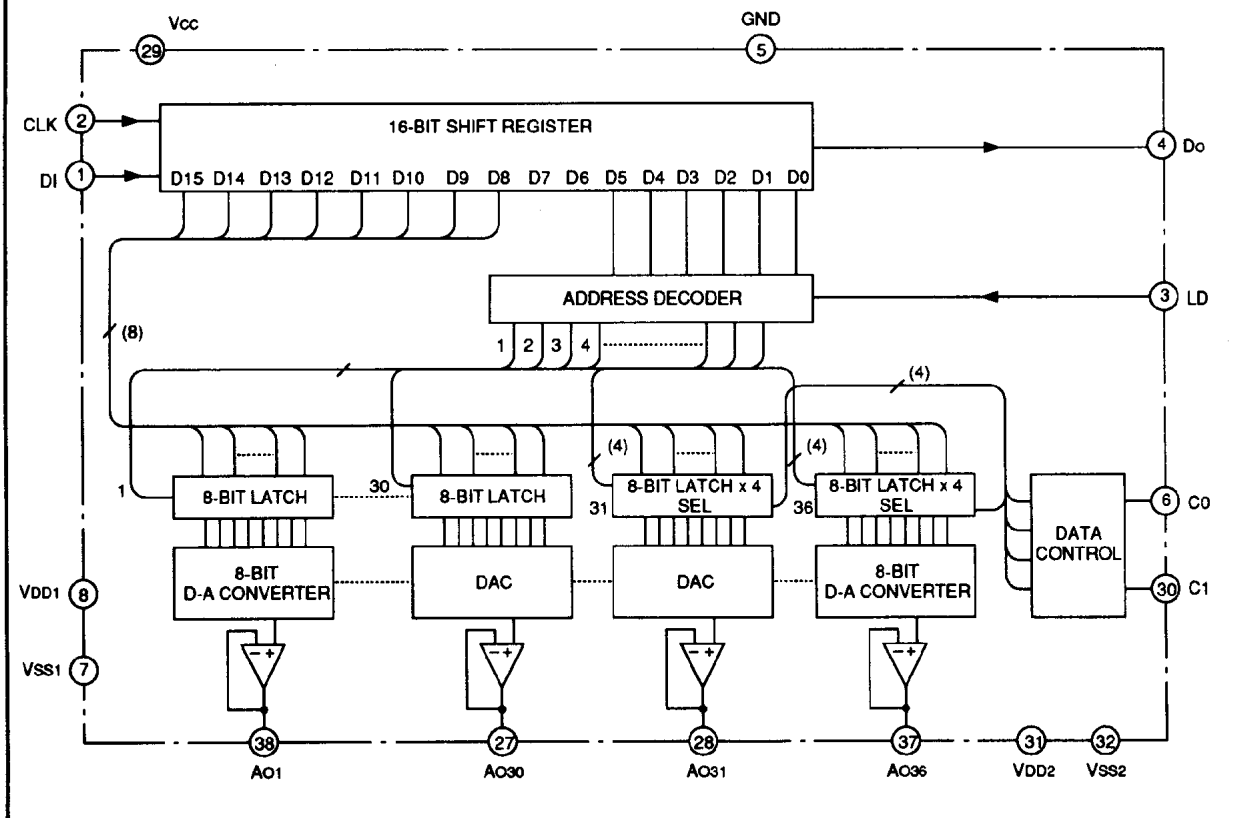
M62371GP

3V TYPE 8-BIT 36CH SELECTOR SW BUILT-IN D-A CONVERTER WITH BUFFER AMPLIFIERS

EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
①	DI	Serial data input terminal to input 16-bit long serial data
④	Do	Terminal to output MSB data of 16-bit shift register
②	CLK	Shift clock input terminal. Input signal at DI pin is input to 16-bit shift register at rise of shift clock pulse
③	LD	When H-level signal is input to this terminal, the value stored in 16-bit shift register is loaded in decoder and D-A converter output register
⊗ } ⊗ ⑨ } ⊗ ⊗ } ⊗	Ao1 } Ao11 Ao12 } Ao31 Ao32 } Ao36	8-bit D-A converter output terminal
⊗	Vcc	Power supply terminal
⑤	GND	GND terminal
⑥	C0	Data select signal input terminal 1 for channel No. 31 through 36
⊗	C1	Data select signal input terminal 2 for channel No. 31 through 36
⑧	VDD1	Upper reference voltage input terminal and power supply to operational amplifier for channel No. 1 through 24
⑦	VSS1	Lower reference voltage input terminal for channel No. 1 through 24
⊗	VDD2	Upper reference voltage input terminal and power supply to operational amplifier for channel No. 25 through 36
⊗	VSS2	Lower reference voltage input terminal for channel No. 25 through 36

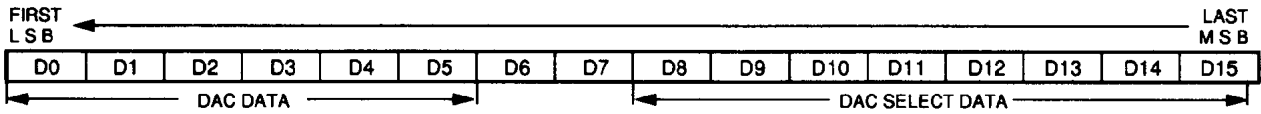
BLOCK DIAGRAM FOR EXPLANATION OF TERMINALS



M62371GP

3V TYPE 8-BIT 36CH SELECTOR SW BUILT-IN D-A CONVERTER WITH BUFFER AMPLIFIERS

DIGITAL DATA FORMAT



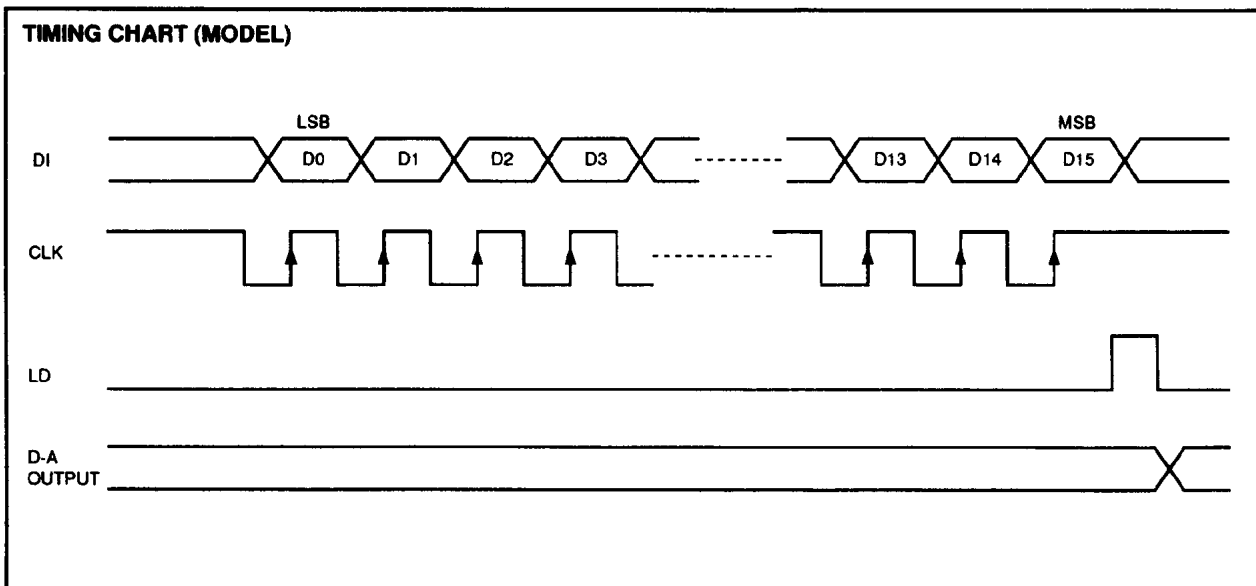
D8	D9	D10	D11	D12	D13	D14	D15	D-A output
0	0	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 1 + V_{refL}$
1	0	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 2 + V_{refL}$
0	1	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 3 + V_{refL}$
1	1	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 4 + V_{refL}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	$(V_{refU} - V_{refL}) / 256 \times 255 + V_{refL}$
1	1	1	1	1	1	1	1	V_{refU}

D5	D4	D3	D2	D1	D0	DAC selection
0	0	0	0	0	0	Don't care
0	0	0	0	0	1	AO1 selection
0	0	0	0	1	0	AO2 selection
?	?	?	?	?	?	}
0	1	1	1	1	0	AO30 selection
0	1	1	1	1	1	AO31(0)selection
1	0	0	0	0	0	AO32(0)selection
?	?	?	?	?	?	}
1	0	0	1	0	0	AO36(0)selection
1	0	0	1	0	1	AO31(1)selection
?	?	?	?	?	?	}
1	0	1	0	1	0	AO36(1)selection
1	0	1	0	1	1	AO31(2)selection
?	?	?	?	?	?	}
1	1	0	0	0	0	AO36(2)selection
1	1	0	0	0	1	AO31(3)selection
?	?	?	?	?	?	}
1	1	0	1	1	0	AO36(3)selection
1	1	0	1	1	1	Don't care
?	?	?	?	?	?	}
1	1	1	1	1	1	Don't care

C0	C1	AO31 through AO36 data selected
0	0	Address 0 selected
0	1	Address 1 selected
1	0	Address 2 selected
1	1	Address 3 selected

* $V_{refU} = V_{DD1}, V_{DD2}$
 $V_{refL} = V_{SS1}, V_{SS2}$

TIMING CHART (MODEL)



M62371GP**3V TYPE 8-BIT 36CH SELECTOR SW BUILT-IN D-A CONVERTER WITH BUFFER AMPLIFIERS****ABSOLUTE MAXIMUM RATINGS** (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.3~7.0	V
Vo	Output voltage		-0.3~Vcc+0.3	V
Pd	Power dissipation		400	mW
K θ	Thermal derating	Ta \leq 25°C	4	mW/°C
Topr	Operating temperature		-20~+85	°C
Tstg	Storage temperature		-40~+125	°C

ELECTRICAL CHARACTERISTICS**Digital part** (Vcc=+3V \pm 10%, Vcc=VDD, Ta=-20 ~+85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Vcc	Supply voltage		2.7	3.0	5.5	V
Icc	Circuit current	CLK=1MHz operation, Vcc=3V, IAO=0 μ A		1.0		mA
IILK	Input leak current		-10		10	μ A
VIL	Input low voltage				0.6	V
VIH	Input high voltage		2.4			V
VOL	Output low voltage	IOL=2.5mA			0.4	V
VOH	Output high voltage	IOH=-400 μ A	Vcc-0.4			V

Note. Standard value is at Ta=25°C.

Analog part (Vcc=+3V \pm 10%, Vcc=VDD, Ta=-20 ~+85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
IDD	Current dissipation			8.0	12.0	mA
VDD	D-A converter upper reference voltage range		2.7	3.0	5.5	V
VSS	D-A converter lower reference voltage range		GND		VDD-2	V
VAO	Buffer amplifier output voltage range	IAO=±0.5mA	0.1		VDD-0.1	V
		IAO=±1.0mA	0.2		VDD-0.2	
IAO	Buffer amplifier output driving range	Upper saturation voltage=0.4V Lower saturation voltage=0.4V	-1.5		1.5	mA
SDL	Differential nonlinearity error	Vcc=2.700V	-1.0		1.0	LSB
SL	Nonlinearity error	VDD=2.700V	-1.5		1.5	LSB
SZERO	Zero code error	VSS=0.050V	-2		2	LSB
SFULL	Full scale error	No load (IAO=±0)	-2		2	LSB
Co	Output capacitive load				0.1	μ F
RO	Buffer amplifier output impedance			50		Ω

M62371GP

3V TYPE 8-BIT 36CH SELECTOR SW BUILT-IN D-A CONVERTER WITH BUFFER AMPLIFIERS

AC CHARACTERISTICS (V_{CC}=V_{DD}, T_a=-20 ~ +85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
tCKL	Clock "L" pulse width		200			ns
tCKH	Clock "H" pulse width		200			ns
tCR	Clock rise time				200	ns
tCF	Clock fall time				200	ns
tDCH	Data setup time		30			ns
tCHD	Data hold time		60			ns
tCHL	LDsetup time		200			ns
tLDC	LD hold time		100			ns
tLDH	LD "H" pulse duration		100			ns
tDO	Data output delay time	CL=100pF	70		350	ns
tLDD	D-A converter output settling time	CL≤100pF, V _{AO} :0.3V±2.7V The time until the output becomes the final value of ±2 LSB			100	μs

TIMING CHART

