

# M62368GP

## 3V TYPE 8-BIT 6CH D-A CONVERTER WITH BUFFER AMPLIFIERS

### DESCRIPTION

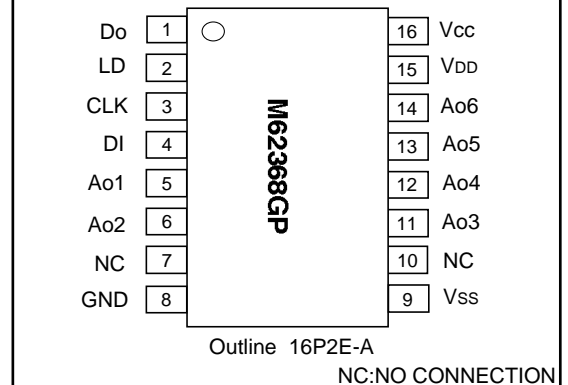
The M62368GP is a CMOS semiconductor IC, containing 6 channels of 8-bit D-A converters. It is operable with a low supply voltage between 2.7~3.6V, and is easy to use due to serial data input, and 3-pin(DI,CLK,LD)connection with microcomputer.

The IC also contains Do pin terminal, enabling cascade connection, and therefore is suitable for automatic control in combination with a microcomputer.

### FEATURES

- Operable with a low voltage between 2.7~3.6V
- 12-bit serial data input(connected via 3 pins:DI,CLK,LD)
- 6 channels of R-2R and segment type high-performance 8-bit D-A converters
- 6 buffer operational amplifiers with full swing of output voltage between Vcc and GND.
- High oscillation stability against the capacitive load of buffer operational amplifiers.

### PIN CONFIGURATION (TOP VIEW)

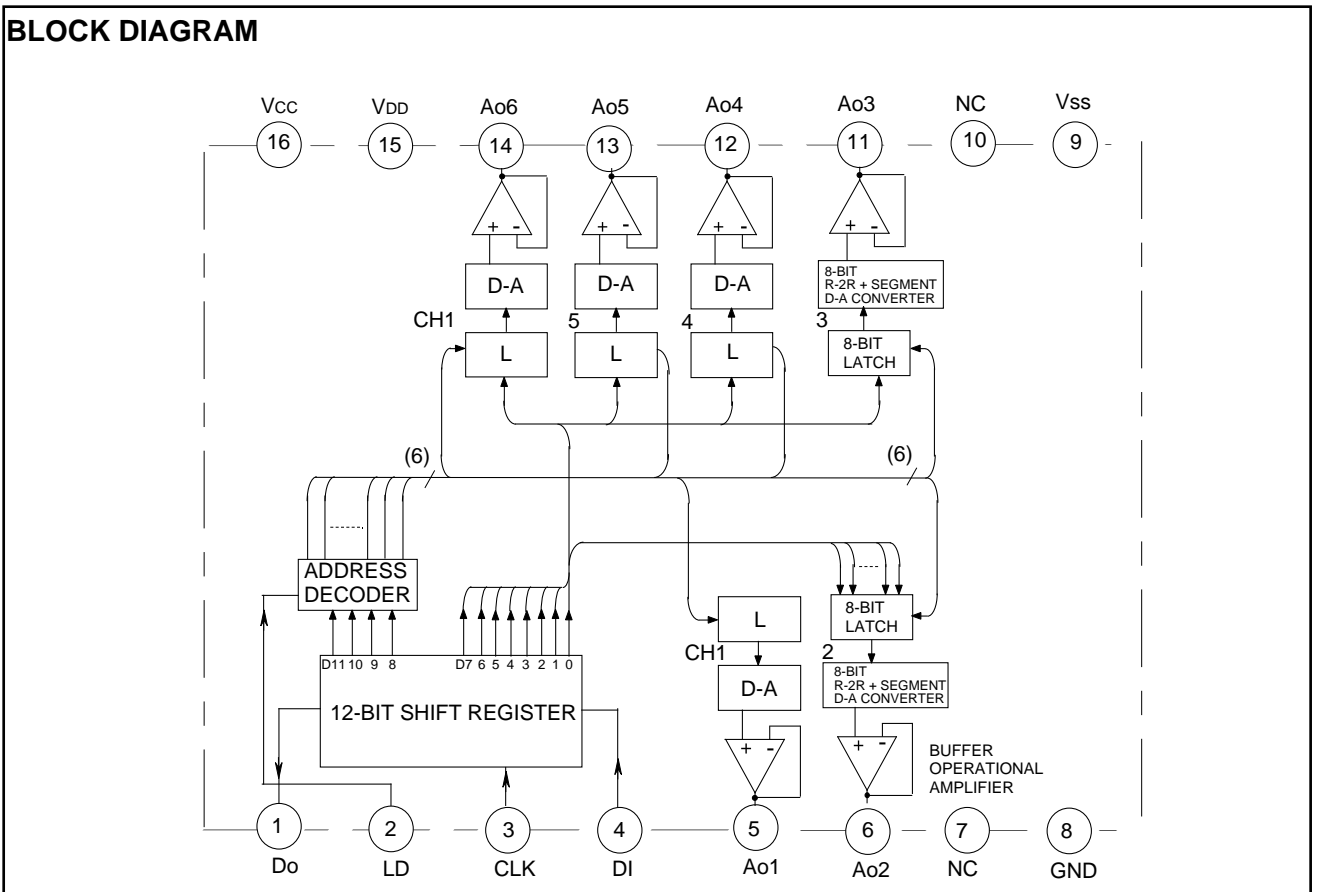


### APPLICATION

Digital-analog conversion in industrial or home-use electronic equipment.

Automatic control in combination with EEPROM and microcomputer(Substitute for conventional semi-fixed resistor)

### BLOCK DIAGRAM



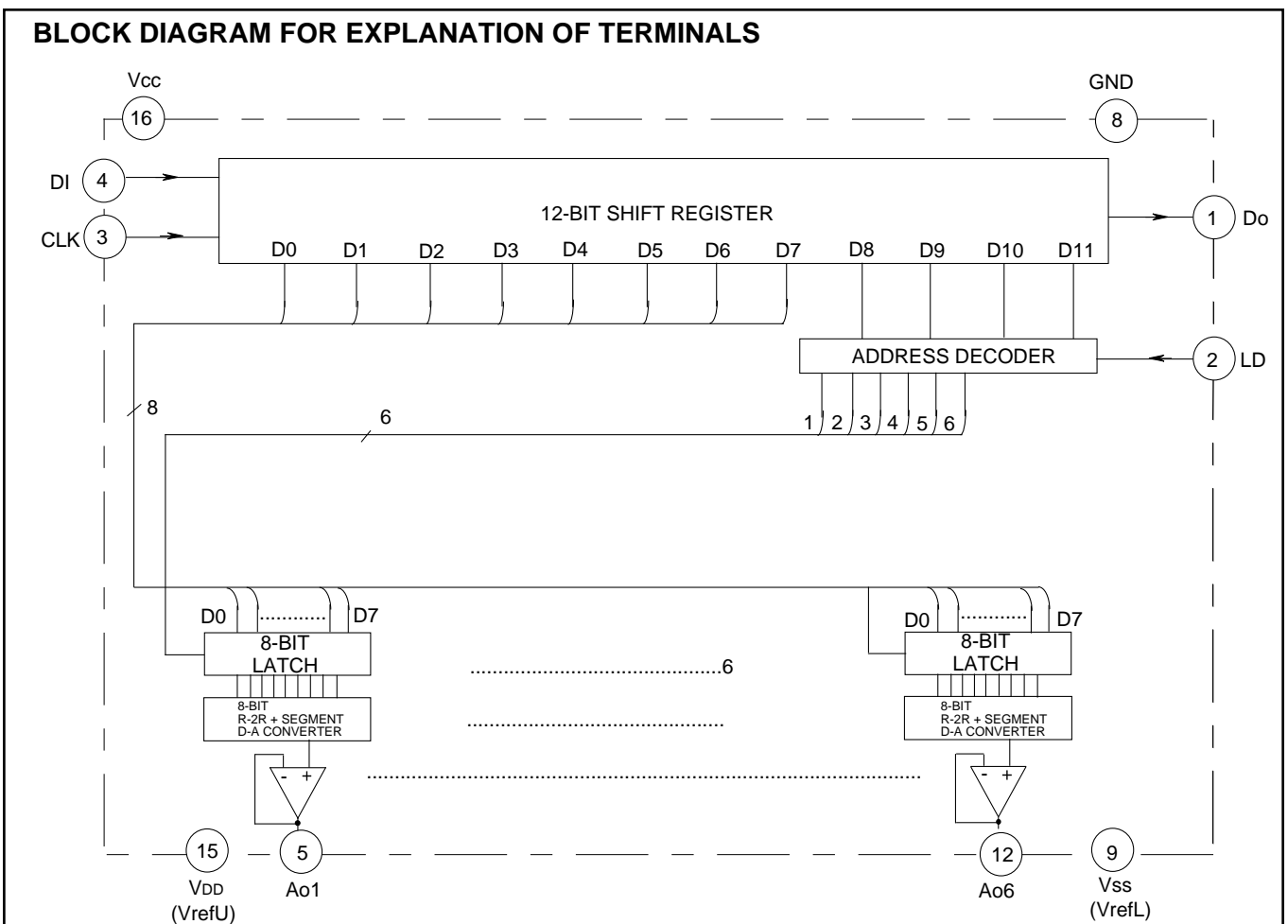
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### EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
④	DI	Serial data input terminal to input 12-bit long serial data
①	Do	Terminal to output MSB data of 12-bit shift register
③	CLK	Shift clock input terminal. Input signal at DI pin is input to 12-bit shift register at rise of shift clock pulse
②	LD	When H-level signal is input to this terminal, the value stored in 12-bit shift register is loaded in decoder and D-A converter output register
⑤	Ao1	8-bit D-A converter output terminal
⑥	Ao2	
⑪	Ao3	
⑫	Ao4	
⑬	Ao5	
⑭	Ao6	
⑯	Vcc	Power supply terminal
⑧	GND	GND terminal
⑮	VDD	D-A converter upper reference voltage input terminal
⑨	VSS	D-A converter lower reference voltage input terminal

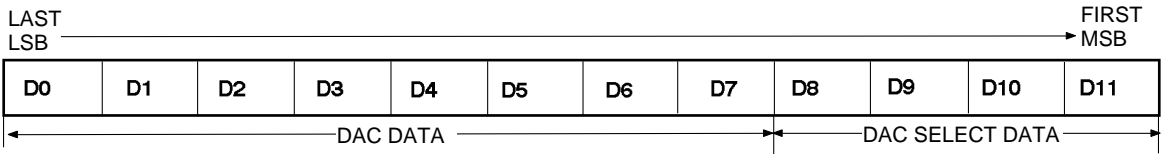
### BLOCK DIAGRAM FOR EXPLANATION OF TERMINALS



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### DIGITAL DATA FORMAT

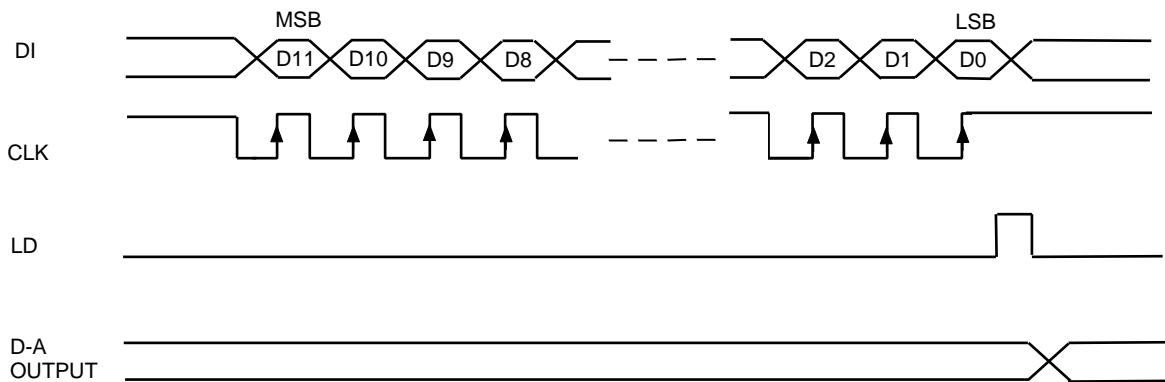


D0	D1	D2	D3	D4	D5	D6	D7	D-A output
0	0	0	0	0	0	0	0	$(V_{refU}-V_{refL}) / 256 \times 1 + V_{refL}$
1	0	0	0	0	0	0	0	$(V_{refU}-V_{refL}) / 256 \times 2 + V_{refL}$
0	1	0	0	0	0	0	0	$(V_{refU}-V_{refL}) / 256 \times 3 + V_{refL}$
1	1	0	0	0	0	0	0	$(V_{refU}-V_{refL}) / 256 \times 4 + V_{refL}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	$(V_{refU}-V_{refL}) / 256 \times 255 + V_{refL}$
1	1	1	1	1	1	1	1	$V_{refU}$

D8	D9	D10	D11	DAC selection
0	0	0	0	Don't care
0	0	0	1	Ao1 selection
0	0	1	0	Ao2
0	0	1	1	Ao3
0	1	0	0	Ao4
0	1	0	1	Ao5
0	1	1	0	Ao6
0	1	1	1	Don't care
1	0	0	0	Don't care
1	0	0	1	Don't care
1	0	1	0	Don't care
1	0	1	1	Don't care
1	1	0	0	Don't care
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care

\*  $V_{refU}=V_{DD}$   
 $V_{refL}=V_{SS}$

### TIMING CHART (MODEL)



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## 3V TYPE 8-BIT 6CH D-A CONVERTER WITH BUFFER AMPLIFIERS

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Supply voltage		-0.3~+7.0	V
V <sub>DD</sub>	Upper reference voltage of D-A converter		-0.3~+7.0	V
V <sub>IN</sub>	Input voltage		-0.3~V <sub>CC</sub> +0.3	V
V <sub>O</sub>	Output voltage		-0.3~V <sub>CC</sub> +0.3	V
P <sub>d</sub>	Power dissipation		150	mW
T <sub>opr</sub>	Operating temperature		-20~+85	°C
T <sub>stg</sub>	Storage temperature		-40~+125	°C

### ELECTRICAL CHARACTERISTICS

**Digital part**(V<sub>CC</sub>,V<sub>refU</sub>=+3V±10%, V<sub>CC</sub> V<sub>refU</sub>,GND,V<sub>refL</sub>=0V,T<sub>a</sub>=-20 ~ +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V <sub>CC</sub>	Supply voltage		2.7	3.0	3.6	V
I <sub>CC</sub>	Circuit current	CLK=1MHz operation,V <sub>CC</sub> =3V,I <sub>AO</sub> =0μA			3.5	mA
I <sub>ILK</sub>	Input leak current	V <sub>IN</sub> =0~V <sub>CC</sub>	-10		10	μA
V <sub>IL</sub>	Input low voltage				0.2V <sub>CC</sub>	V
V <sub>IH</sub>	Input high voltage		0.8V <sub>CC</sub>			V
V <sub>OL</sub>	Output low voltage	I <sub>OL</sub> =2.5mA			0.4	V
V <sub>OH</sub>	Output high voltage	I <sub>OH</sub> =-400μA	V <sub>CC</sub> -0.4			V

**Analog part**(V<sub>CC</sub>,V<sub>refU</sub>=+3V±10%, V<sub>CC</sub> V<sub>refU</sub>,T<sub>a</sub>=-20 ~ +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I <sub>refU</sub>	Current dissipation	V <sub>refU</sub> =3V,V <sub>refL</sub> =0V Data condition:maximum current		1.4	2.5	mA
V <sub>refU</sub>	D-A converter upper reference voltage range	Reference voltage can not always be set to any value in this range,because it is restricted to the buffer amplifier output voltage range	0.7V <sub>CC</sub>		V <sub>CC</sub>	V
V <sub>refL</sub>	D-A converter lower reference voltage range		GND		0.3V <sub>CC</sub>	V
V <sub>AO</sub>	Buffer amplifier output voltage range	I <sub>AO</sub> =±500μA I <sub>AO</sub> =+500μA -200μA	0.1		V <sub>CC</sub> -0.1	V
			0.2		V <sub>CC</sub> -0.2	
I <sub>AO</sub>	Buffer amplifier output driving range	Upper saturation voltage=0.4V Lower saturation voltage=0.4V	-0.3		1	mA
SDL	Differential nonlinearity error	V <sub>CC</sub> =2.760V	-1.0		1.0	LSB
SL	Nonlinearity error	V <sub>refU</sub> =2.610V	-1.5		1.5	LSB
SZERO	Zero code error	V <sub>refL</sub> =0.050V(10mV/LSB)	-2		2	LSB
SFULL	Full scale error	Without load(I <sub>AO</sub> =±0)	-2		2	LSB
C <sub>O</sub>	Output capacitive load				0.1	μF
R <sub>O</sub>	Buffer amplifier output impedance			5		

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**AC CHARACTERISTICS**( $V_{CC}, V_{refU}=+3V\pm 10\%$ ,  $V_{CC} \ V_{refU}, GND, V_{refL}=0V, T_a=-20 \sim +85^\circ C$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
tCKL	Clock "L" pulse width		200			ns
tCKH	Clock "H" pulse width		200			ns
tCR	Clock rise time				200	ns
tCF	Clock fall time				200	ns
tDCH	Data set up time		30			ns
tCHD	Data hold time		60			ns
tCHL	LD set up time		200			ns
tLDC	LD hold time		100			ns
tLDH	LD "H" pulse duration		100			ns
tDo	Data output delay time	$C_L=100pF$	70		350	ns
tLDD	D-A output setting time	$C_L \ 100pF, V_{AO}:0.1\rightarrow 2.6V$ The time until the output becomes the final value of 1/2 LSB			300	$\mu s$

### TIMING CHART

