

# M62009L/P/FP

## Low Power 2 Output System Reset IC with External Input

REJ03D0782-0100

Rev.1.00

Sep 14, 2005

### Description

As applications for microcomputers are increasing, a desire has arisen for a RAM backup function. Let us introduce Renesas new low power dissipation, high-performance system reset IC, which is suitable for such RAM backup.

The M62009, which is a low power dissipation 2-output microcomputer system reset IC, is a 2-output system reset IC which provides for RAM backup in microcomputers, and reduces power dissipation by using the Bi-CMOS process. The M62009 considerably reduces the number of components in the reset circuit.

The M62009 performs two-step detection of normal supply voltage and backup supply voltage required for backup mode. When the supply voltage is switched from normal supply voltage to backup supply voltage the interruption output, which is one of the two outputs, gives the interruption signal to a microcomputer, in this way, the microcomputer reduces power dissipation and enters in the backup mode. If the backup supply voltage goes lower than the voltage required for backup, the reset output ( $\overline{\text{RESET}}$  output) which is different from the  $\overline{\text{INT}}$  output gives the reset signal (forced reset) to the microcomputer. The interruption signal from the  $\overline{\text{INT}}$  output recovers the microcomputer from the backup mode. To recover from reset,  $\overline{\text{RESET}}$  output is canceled when the specified interval of time (delay time) elapses after the signal is given from the  $\overline{\text{INT}}$  output.

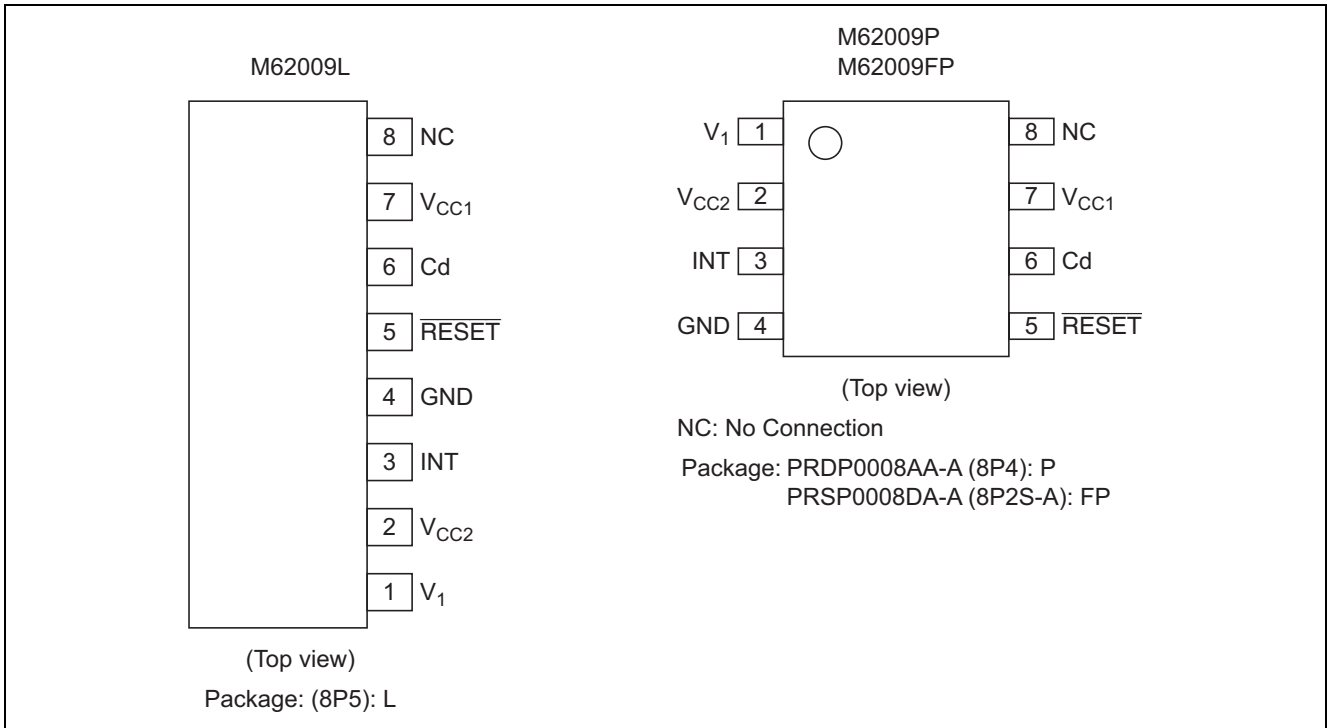
### Features

- Bi-CMOS process realizes a configuration of low current dissipating circuits.
  - $I_{CC} = 7 \mu\text{A}$  (Typ, normal mode,  $V_{CC1} = V_{CC2} = 5.0 \text{ V}$ )
  - $I_{CC} = 5 \mu\text{A}$  (Typ, backup mode,  $V_{CC1} = 5.0 \text{ V}$ )
  - $I_{CC} = 1 \mu\text{A}$  (Typ, backup mode,  $V_{CC1} = 2.5 \text{ V}$ )
- Two-step detection of supply voltage
  - $V_{CC1}$  ( $\overline{\text{RESET}}$ ):
    - $V_{SI-1} = 4.0 \text{ V}$  (Typ, increase of  $V_{CC1}$ )
    - $V_{SI-2} = 2.0 \text{ V}$  (Typ, decrease of  $V_{CC1}$ )
  - $V_{CC2}$  ( $\overline{\text{INT}}$ ):
    - Free setup
- Two outputs (open drain type)
  - Reset output ( $\overline{\text{RESET}}$ ): Forced reset signal output
  - Interruption output ( $\overline{\text{INT}}$ ): Output of the signal for interruption processing (output of the switching signal for backup mode)
- Three types of outline packages
  - 8-pin plastic SIP (single in-line package)
  - 8-pin plastic DIP (dual in-line package)
  - 8-pin plastic SOP (mini flat package)
- Output based on RAM backup mode (see the timing chart)

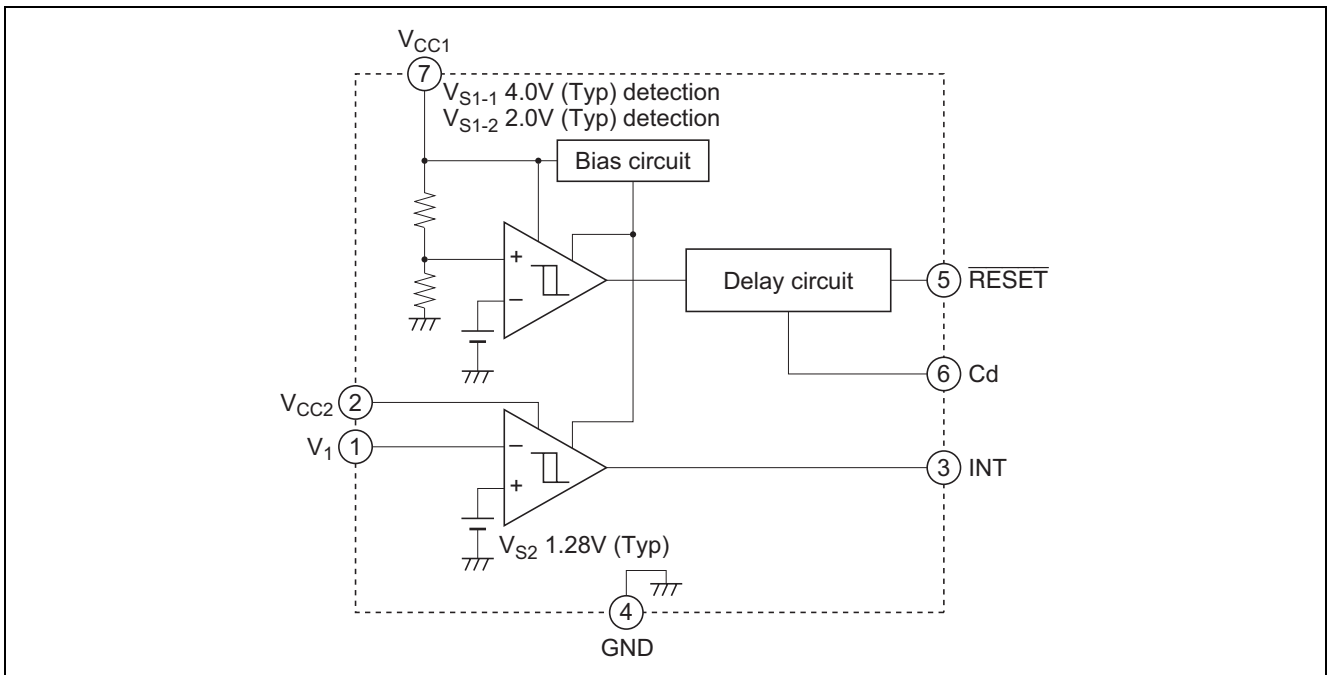
### Application

- Prevention of errors in microcomputer system in electronic equipment that requires RAM backup, such as office, industrial, and home-use equipment.

## Pin Arrangement



## Block Diagram



## Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V <sub>CC</sub>	8	V	
Output sink current	I <sub>sink</sub>	5	mA	
Power dissipation	P <sub>d</sub>	800	mW	8-pin SIP
		625		8-pin DIP
		440		8-pin SOP
Thermal derating	K <sub>θ</sub>	4.4	mW/°C	Ta ≥ 25°C
Operating temperature	T <sub>opr</sub>	-20 to +75	°C	
Storage temperature	T <sub>stg</sub>	-40 to +125	°C	

## Electrical Characteristics

(Ta = 25°C, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Detection voltage	V <sub>S1-1</sub>	3.8	4.0	4.2	V	Increase of V <sub>CC1</sub>
	V <sub>S1-2</sub>	1.85	2.00	2.15		Decrease of V <sub>CC1</sub>
Reference voltage	V <sub>S2</sub>	1.23	1.28	1.33	V	Decrease of V <sub>1</sub>
Hysteresis voltage	ΔV <sub>S</sub>	—	87	—	mV	V <sub>CC2</sub> = Detection voltage of hysteresis voltage (Detection voltage = 4V setup)
Circuit current	I <sub>CC1</sub>	—	7	15	μA	V <sub>CC1</sub> = V <sub>CC2</sub> = 5V
	I <sub>CC2-1</sub>	—	5	10		V <sub>CC1</sub> = 5V, V <sub>CC2</sub> = 0V
	I <sub>CC2-2</sub>	—	1	3		V <sub>CC1</sub> = 2.5V, V <sub>CC2</sub> = 0V
Delay time	t <sub>d</sub>	—	50	—	ms	C <sub>d</sub> = 0.33μF
Output saturation voltage	V <sub>sat</sub>	—	0.2	0.4	V	V <sub>IN</sub> = 5V, I <sub>O</sub> = 4mA (NMOS)
Reset output response time	t <sub>RESET</sub>	—	30	—	μs	Time between V <sub>CC1</sub> (when falling) = V <sub>S1-2</sub> and output of RESET signal
Interruption output reset time	t <sub>INT</sub>	—	100	—	μs	Time between V <sub>CC2</sub> (when falling) = V <sub>S2</sub> and output of INT signal

### Operating Description

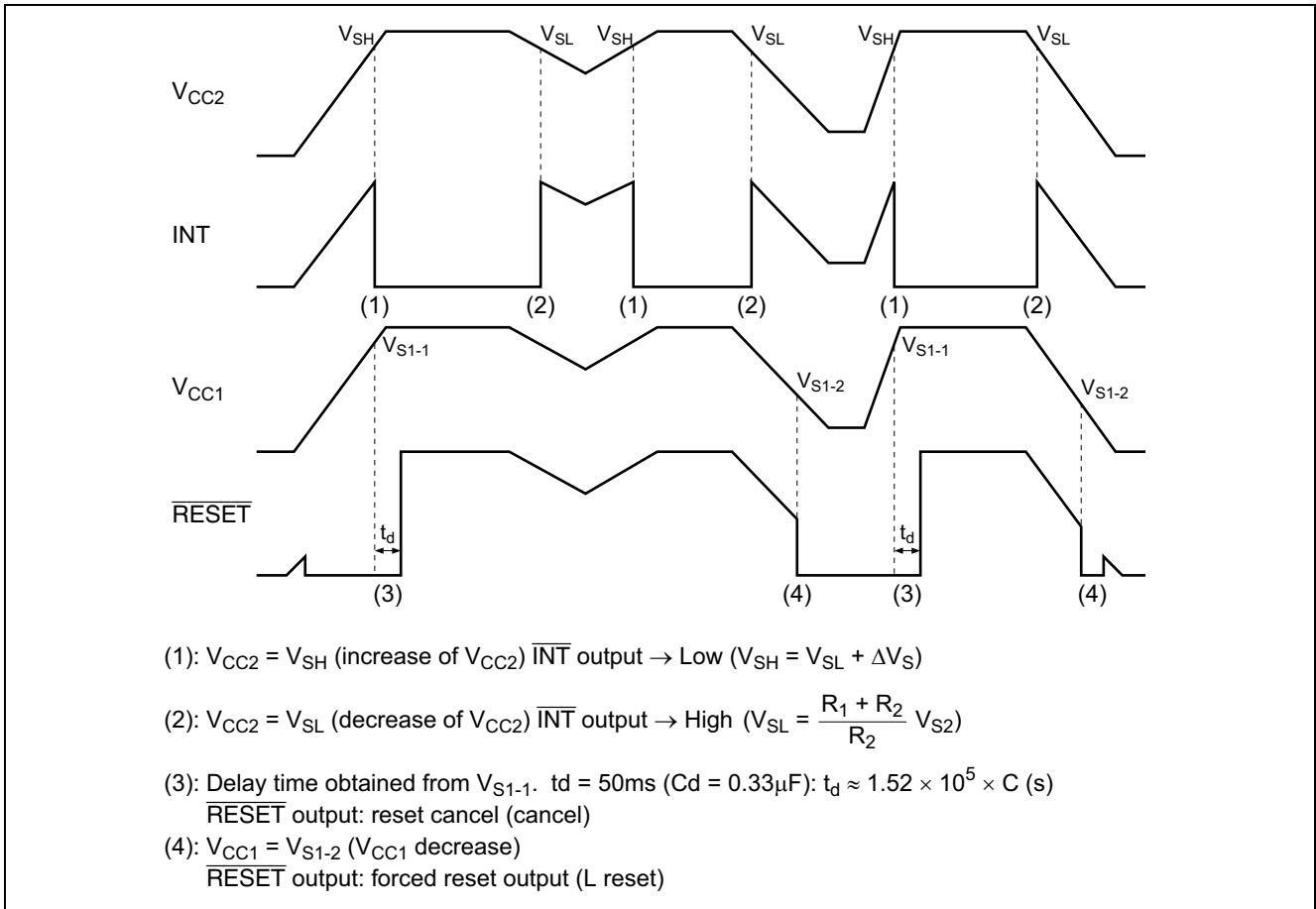


Figure 1 Operating Waveform

### Application Example

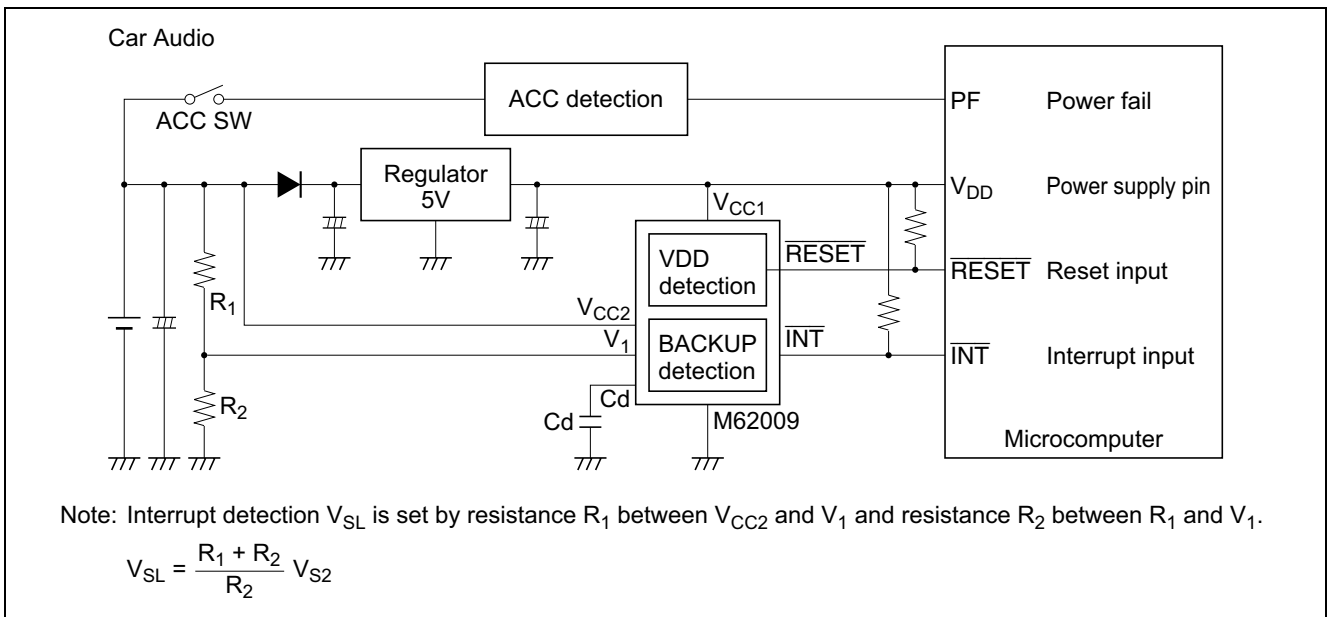
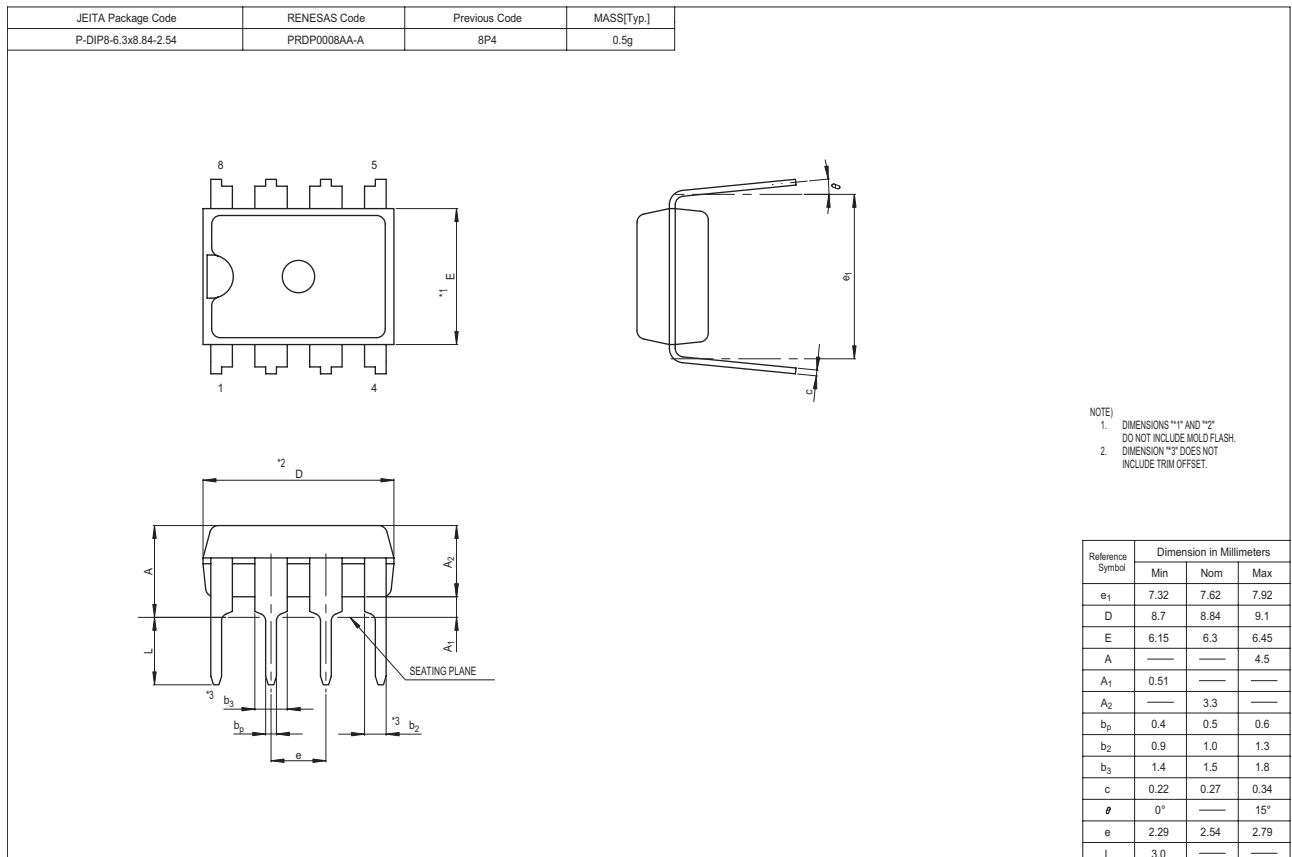
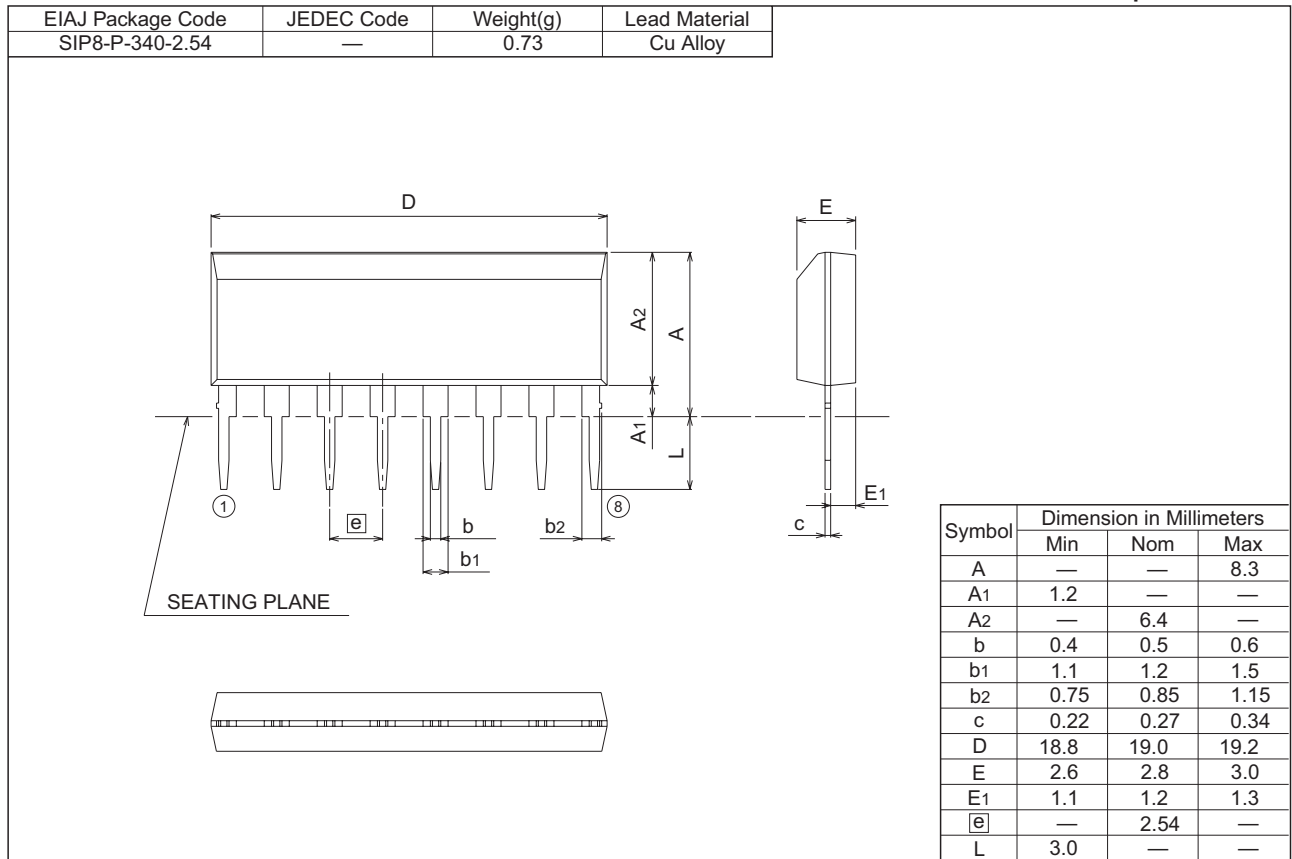


Figure 2 Application Example

# Package Dimensions

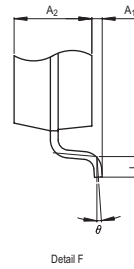
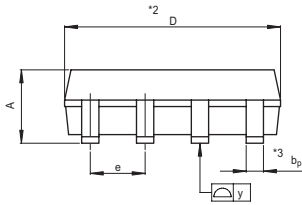
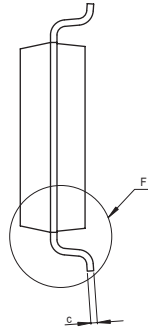
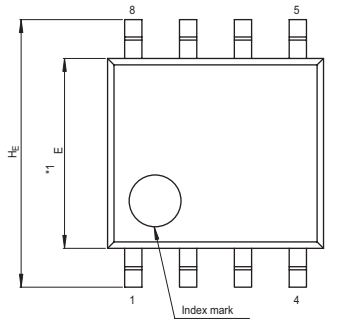
## 8P5

Plastic 8pin 340mil SIP



# M62009L/P/FP

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-4.4x5-1.27	PRSP0008DA-A	8P2S-A	0.07g



NOTE)  
 1. DIMENSIONS  $*1$  AND  $*2$   
 DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION  $*3$  DOES NOT  
 INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.8	5.0	5.2
E	4.2	4.4	4.6
$A_2$	—	1.5	—
$A_1$	0.05	—	—
A	—	—	1.9
$b_p$	0.35	0.4	0.5
c	0.13	0.15	0.2
$\theta$	0°	—	10°
$H_E$	5.9	6.2	6.5
e	1.12	1.27	1.42
y	—	—	0.1
L	0.2	0.4	0.6

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450 Holger Way, San Jose, CA 95134-1368, U.S.A  
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

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#### **Renesas Technology (Shanghai) Co., Ltd.**

Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China  
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#### **Renesas Technology Singapore Pte. Ltd.**

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
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Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea  
Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

#### **Renesas Technology Malaysia Sdn. Bhd.**

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: <603> 7955-9390, Fax: <603> 7955-9510