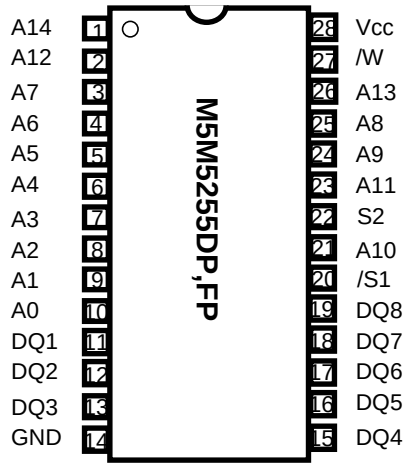
M5M5255DP,FP -45LL,-55LL,-70LL, -45XL,-55XL,-70XL

262,144-BIT (32,768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5255DP,FP is 262,144-bit CMOS static RAMs organized as 32,768-words by 8-bits which is fabricated using high-performance 3 polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery results in a high density and low power static RAM. Stand-by current is small enough for battery back-up application. It is ideal for the memory systems which require simple interface.

PIN CONFIGURATION (TOP VIEW)



Outline 28P4 (DP)
28P2W-C (DFP)

FEATURE

Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5255DP, FP-45LL	45ns	55mA (Vcc=5.5V)	20µA (Vcc=5.5V)
M5M5255DP, FP-55LL	55ns		
M5M5255DP, FP-70LL	70ns		
M5M5255DP, FP-45XL	45ns		5µA (Vcc=5.5V)
M5M5255DP, FP-55XL	55ns		0.05µA (Vcc=3.0V, Typical)
M5M5255DP, FP-70XL	70ns		

- •Single +5V power supply
- •No clocks, no refresh
- •Data-Hold on +2.0V power supply
- •Directly TTL compatible : all inputs and outputs
- •Three-state outputs : OR-tie capability
- •Simple memory expantion by /S1, S2
- •Common Data I/O
- •Battery backup capability
- •Low stand-by current·····0.05µA(typ.)

PACKAGE

M5M255DP : 28 pin 600 mil DIP
M5M5255DFP : 28 pin 450 mil SOP

APPLICATION

Small capacity memory units

FUNCTION

The operation mode of the M5M5255DP,FP is determined by a combination of the device control inputs /S1, S2 and /W. Each mode is summarized in the function table.

A write cycle is executed whenever the low level /W overlaps with the low level /S1 and the high level S2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of /W, /S1 or S2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained.

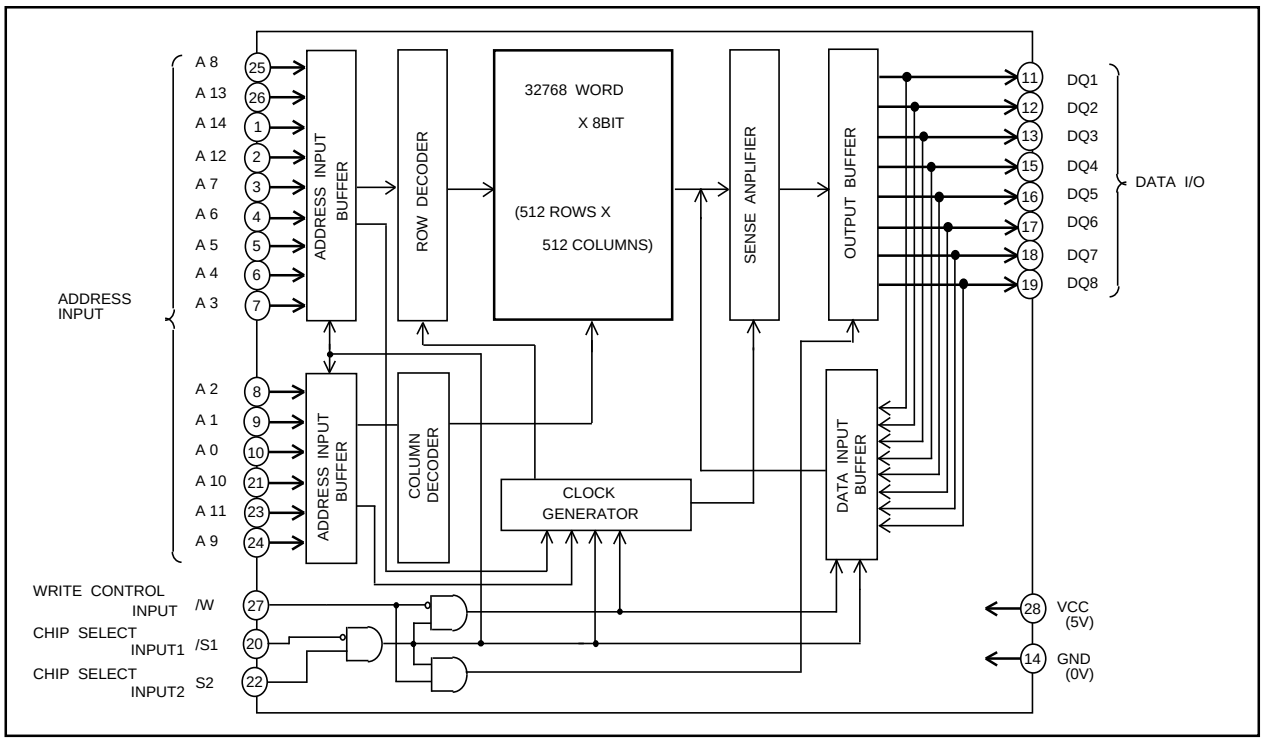
A read cycle is executed by setting /W at a high level while /S1 and S2 are in an active state(/S1="L", S2="H").

When setting /S1 at a high level or S2 at a low level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by /S1 and S2. The power supply current is reduced as low as the stand-by current which is specified as Icc3 or Icc4, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

/S1	S2	/W	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Non selection	High-impedance	Stand-by
L	H	L	Write	D_{IN}	Active
L	H	H	Read	D_{OUT}	Active

FUNCTION TABLE



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to GND	-0.3*~7.0	V
V_I	Input voltage		-0.3*~Vcc+0.3 (Max 7.0)	V
V_O	Output voltage		0~Vcc	V
P_d	Power dissipation	Ta=25°C	700	mW
T_{opr}	Operating temperature		0~70	°C
T_{stg}	Storage temperature		-65~150	°C

* -3.0V in case of AC (Pulse width ≤ 30ns)

DC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.2		Vcc +0.3	V
V_{IL}	Low-level input voltage			-0.3		0.8	V
V_{OH1}	High-level output voltage 1	I_{OH}=-1mA		2.4			V
V_{OH2}	High-level output voltage 2	I_{OH}=-0.1mA		Vcc -0.5			V
V_{OL}	Low-level output voltage	I_{OL}=2mA				0.4	V
I_I	Input current	V_I=0~Vcc				±1	uA
I_O	Output current in off-state	/S_1=V_{IH} or S_2=V_{IL} or /OE=V_{IH} $V_{I/O}$=0~Vcc				±1	uA
Icc1	Active supply current (AC, MOS level)	/S_1≤0.2V, S_2>Vcc-0.2V Other inputs<0.2V or >Vcc-0.2V Output-open(duty 100%)	45ns		35	50	mA
			55ns		30	45	
			70ns		25	40	
Icc2	Active supply current (AC, TTL level)	/S_1=V_{IL},S_2=V_{IH} other inputs=V_{IH} or V_{IL} Output-open(duty 100%)	45ns		35	55	mA
			55ns		30	50	
			70ns		25	45	
Icc3	Stand-by current	S_2≤0.2V or /S_1≥Vcc-0.2V, S_2≥Vcc-0.2V other inputs=0~Vcc	-LL			20	uA
			-XL			5	
Icc4	Stand-by current	/S_1=V_{IH} or S_2=V_{IL}, other inputs=0~Vcc				3	mA

* -3.0V in case of AC (Pulse width ≤ 30ns)

CAPACITANCE (Ta=0~70°C, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			6	pF
C_O	Output capacitance	V_O=GND,V_O=25mVrms, f=1MHz			8	pF

Note 0: Direction for current flowing into an IC is positive (no mark).
1: Typical value is one at Ta = 25°C.
2: C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, Vcc=5V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level·····V_{IH}=2.4V,V_{IL}=0.6V

Input rise and fall time·····5ns

Reference level·····V_{OH}=V_{OL}=1.5V

Output loads·····Fig.1,CL=30pF (-45LL,-45XL)

CL=50pF (-55LL,-55XL)

CL=100pF (-70LL,-70XL)

CL=5pF (for ten,tdis)

Transition is measured ±500mV from steady state voltage. (for ten,tdis)

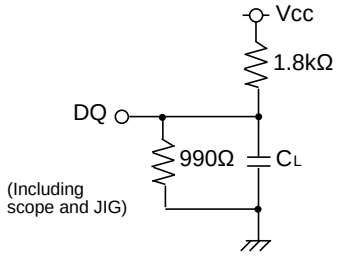


Fig.1 Output load

(2) READ CYCLE

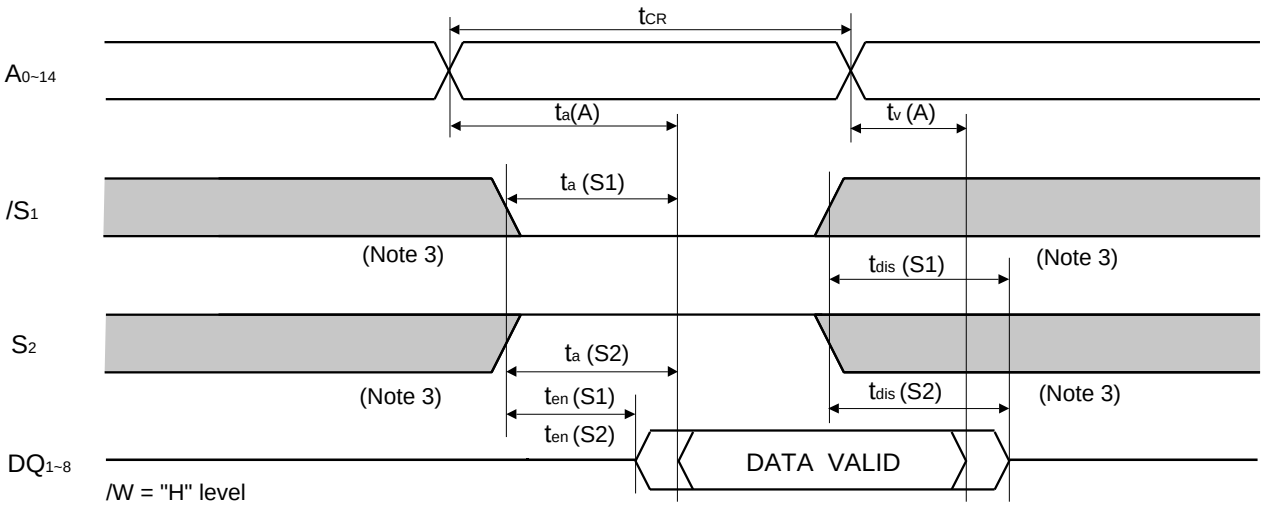
Symbol	Parameter	Limits						Unit
		-45LL, XL		-55LL, XL		-70LL, XL		
		Min	Max	Min	Max	Mi	Max	
t_{CR}	Read cycle time	45		55		70		ns
t_a(A)	Address access time		45		55		70	ns
t_a(S_1)	Chip select 1 access time		45		55		70	ns
t_a(S_2)	Chip select 2 access time		45		55		70	ns
t_{dis}(S_1)	Output disable time after /S_1 high		15		20		25	ns
t_{dis}(S_2)	Output disable time after S_2 low		15		20		25	ns
t_{en}(S_1)	Output enable time after /S_1 low	5		5		5		ns
t_{en}(S_2)	Output enable time after S_2 high	5		5		5		ns
t_v(A)	Data valid time after address	10		10		10		ns

(3) WRITE CYCLE

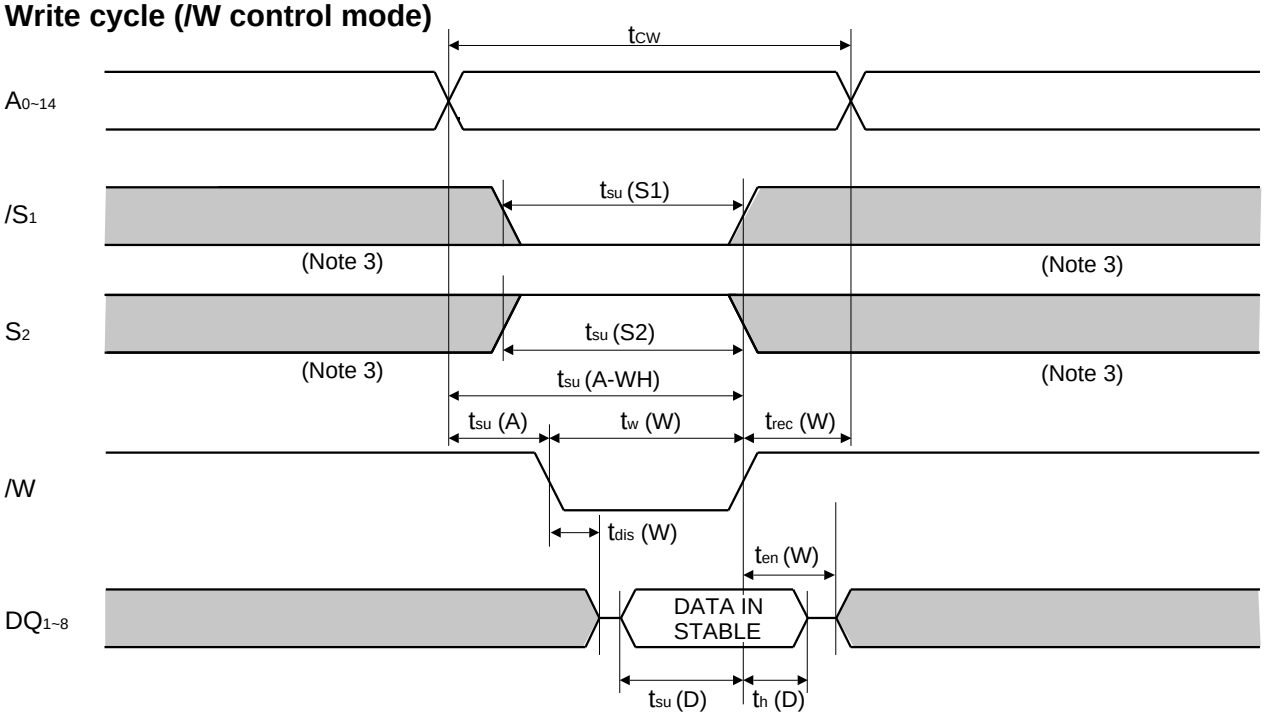
Symbol	Parameter	Limits						Unit
		-45LL, XL		-55LL, XL		-70LL, XL		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	45		55		70		ns
t_w(W)	Write pulse width	35		40		50		ns
t_{su}(A)	Address setup time	0		0		0		ns
t_{su}(A-WH)	Address setup time with respect to /W	40		50		65		ns
t_{su}(S_1)	Chip select 1 setup time	40		50		65		ns
t_{su}(S_2)	Chip select 2 setup time	40		50		65		ns
t_{su}(D)	Data setup time	20		25		30		ns
t_h(D)	Data hold time	0		0		0		ns
t_{rec}(W)	Write recovery time	0		0		0		ns
t_{dis}(W)	Output disable time from /W low		15		20		25	ns
t_{en}(W)	Output enable time from /W high	5		5		5		ns

(4) TIMING DIAGRAMS

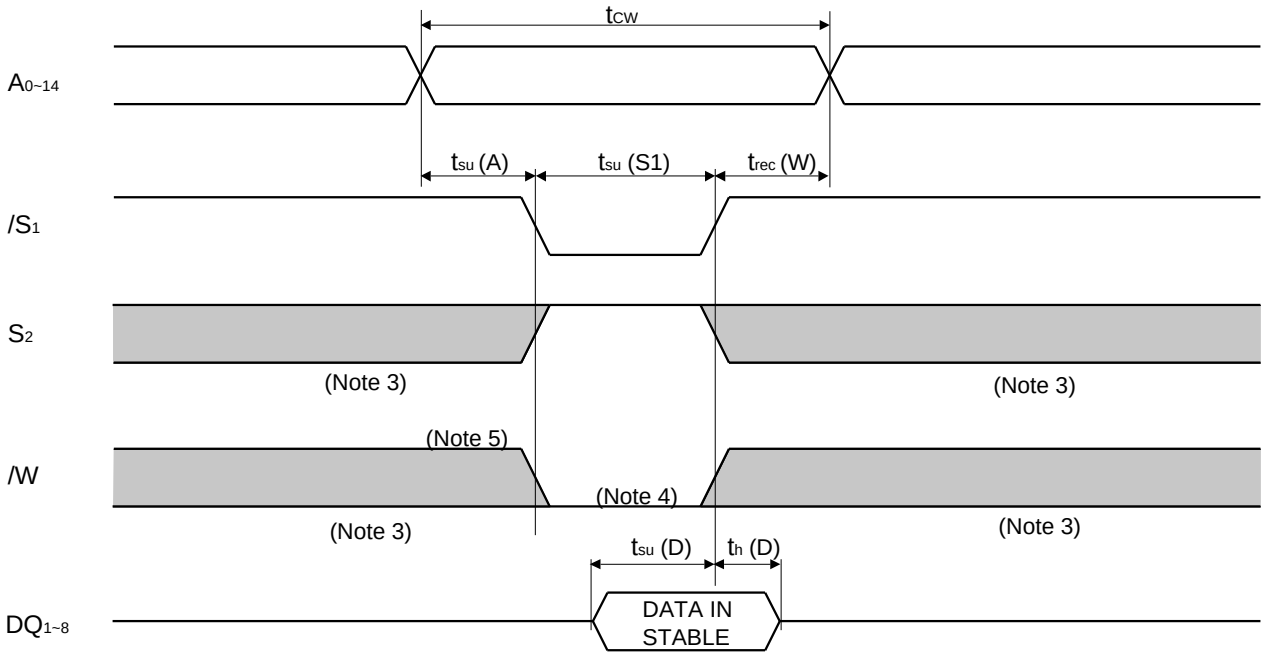
Read cycle



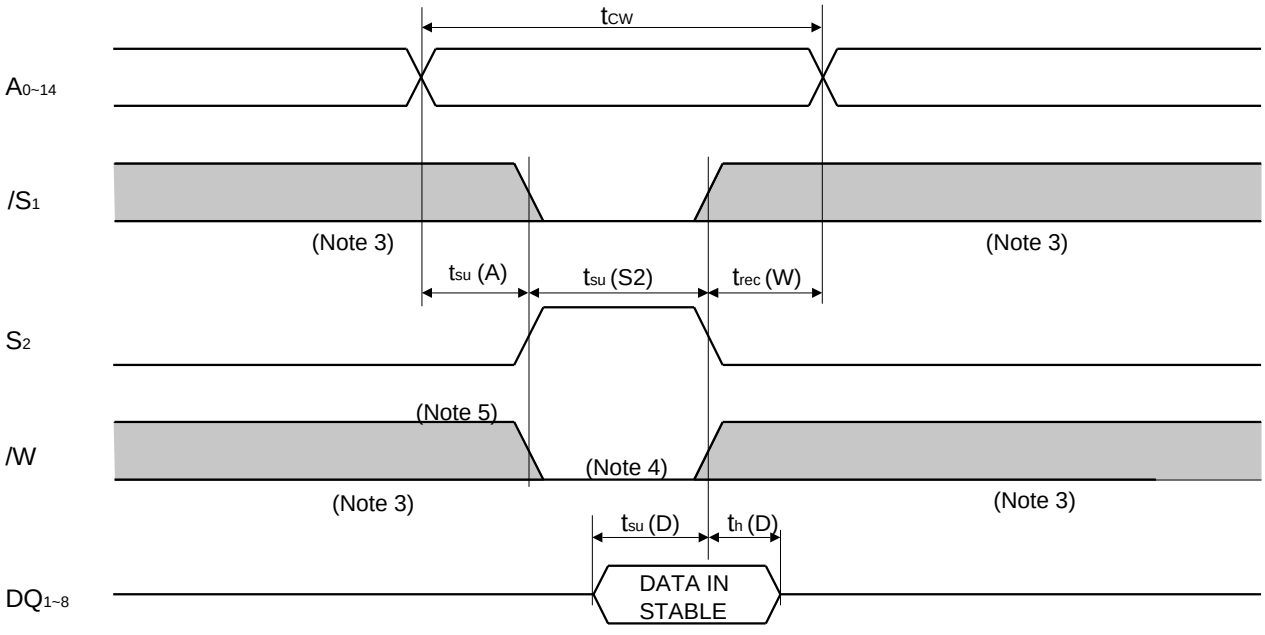
Write cycle (/W control mode)



Write cycle (/S1 control mode)



Write cycle (S2 control mode)



Note 3 : Hatching indicates the state is "don't care".
4 : Writing is executed while S2 high overlaps /S1 and /W low.
5 : When the falling edge of /W is simultaneously or prior to the falling edge of /S1 or rising edge of S2, the outputs are maintained in the high impedance state.
6 : Don't apply inverted phase signal externally when DQ pin is output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC\ (PD)}$	Power down supply voltage			2			V
$V_{I\ (/S1)}$	Chip select input /S_1	2.2V≤$V_{CC(PD)}$		2.2			V
		2V≤$V_{CC(PD)}$≤2.2V			$V_{CC(PD)}$		V
$V_{I\ (S2)}$	Chip select input S_2	4.5V≤$V_{CC(PD)}$				0.8	
		$V_{CC(PD)}$<4.5V				0.2	
$I_{CC\ (PD)}$	Power down supply current	Vcc = 3V S_2≤0.2V or /S_1≥Vcc-0.2V,S_2≥Vcc-0.2V	-LL			10 (Note 7)	uA
			-XL		0.1	2 (Note 8)	

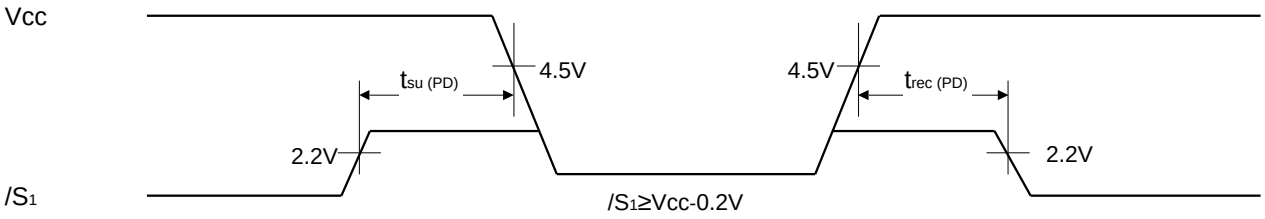
Note7: ICC (PD) = 1uA in case of Ta = 25°C
Note8: ICC (PD) = 0.5uA in case of Ta = 25°C

(2) TIMING REQUIREMENTS (Ta = 0~70°C, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su\ (PD)}$	Power down set up time		0			ns
$t_{rec\ (PD)}$	Power down recovery time		t_{CR}			ns

(3) POWER DOWN CHARACTERISTICS

/S_1 control mode



S_2 control mode