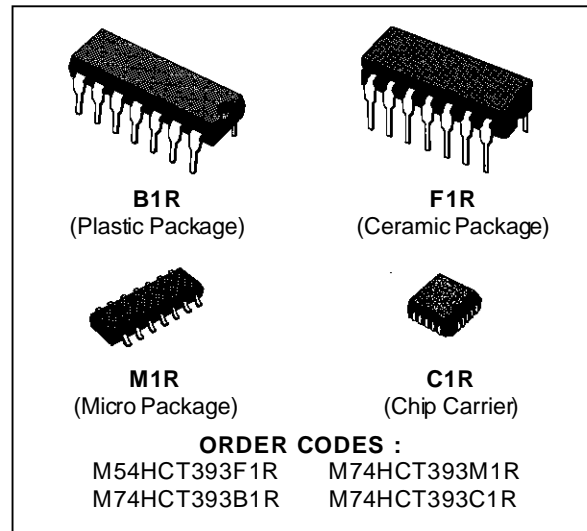


## DUAL BINARY COUNTER

- HIGH SPEED  
 $f_{MAX} = 80 \text{ MHz (TYP.) AT } V_{CC} = 5 \text{ V}$
- LOW POWER DISSIPATION  
 $I_{CC} = 4 \mu\text{A (MAX.) AT } T_A = 25 \text{ }^\circ\text{C}$
- COMPATIBLE WITH TTL OUTPUTS  
 $V_{IH} = 2\text{V (MIN.) } V_{IL} = 0.8\text{V (MAX)}$
- OUTPUT DRIVE CAPABILITY  
 10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE  
 $|I_{OH}| = I_{OL} = 4 \text{ mA (MIN.)}$
- BALANCED PROPAGATION DELAYS  
 $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE  
 WITH 54/74LS393



### DESCRIPTION

The M54/74HCT393 is a high speed CMOS DUAL BINARY COUNTER fabricated in silicon gate C<sup>2</sup>MOS technology. It has the same high speed performance of LSTTL combined with true COMS low power consumption.

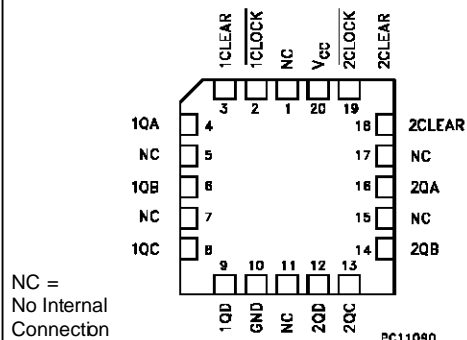
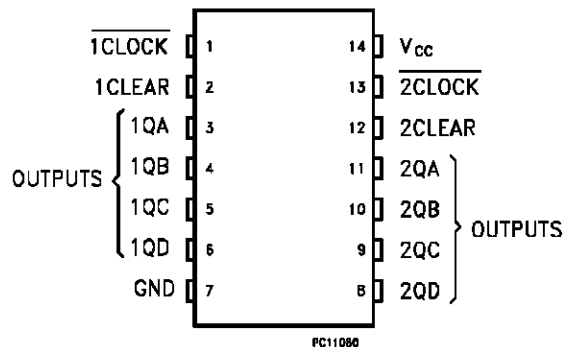
This counter circuit contains independent ripple carry counters and two 4-bit ripple carry binary counters, which can be cascaded to create a single divide by 256 counter.

Each 4-bit counter is incremented on the high to low transition (negative edge) of the clock input, and each has an independent clear input. When clear is set to high all four bits of each counter are set to a low level. This enables count truncation and allows the implementation of divide by N counter configurations.

This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC<sup>2</sup>MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

### PIN CONNECTIONS (top view)



INPUT AND OUTPUT EQUIVALENT CIRCUIT



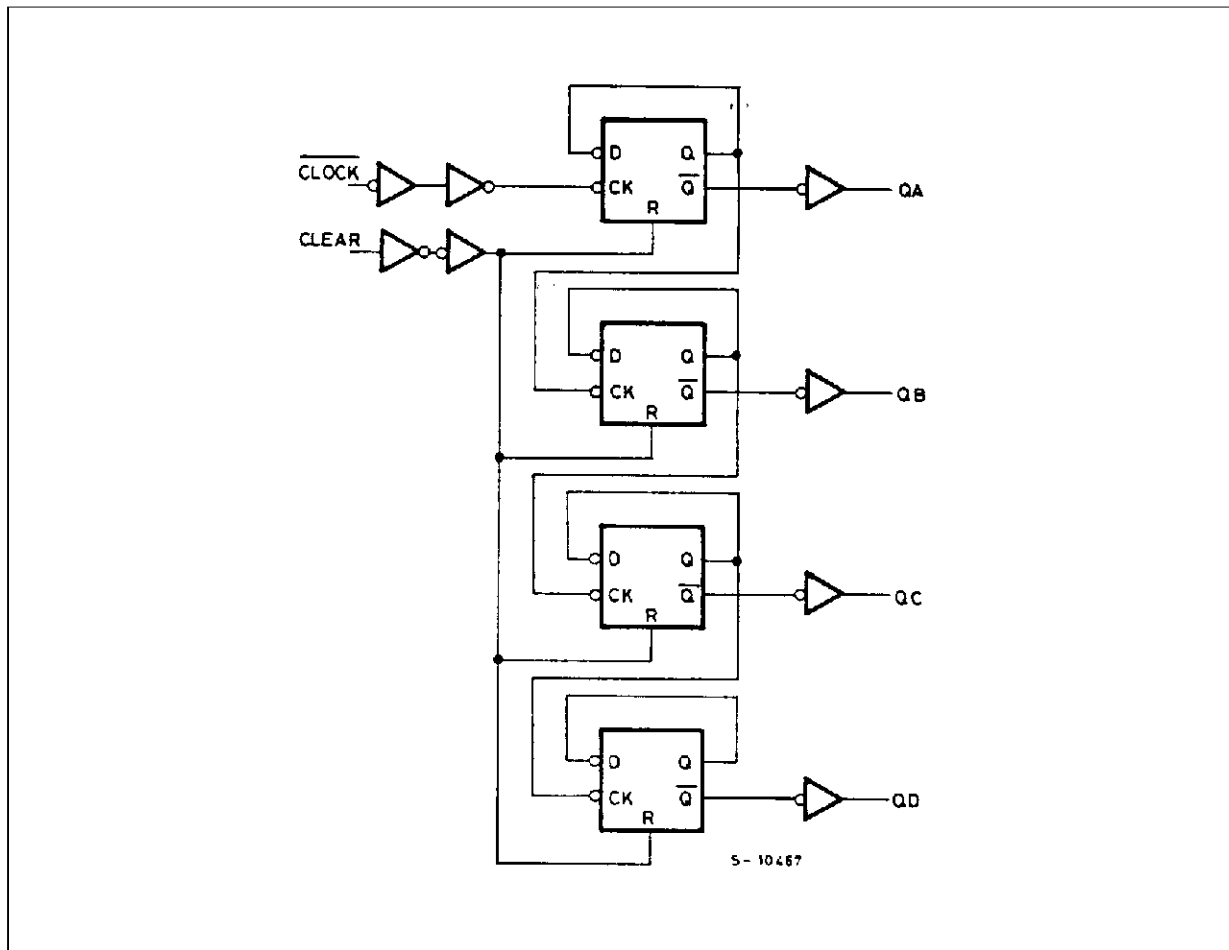
TRUTH TABLE

INPUTS		OUTPUTS			
CLOCK	CLEAR	QD	QC	QB	QA
X	H	L	L	L	L
	L	COUNT UP			
	L	NO CHANGE			

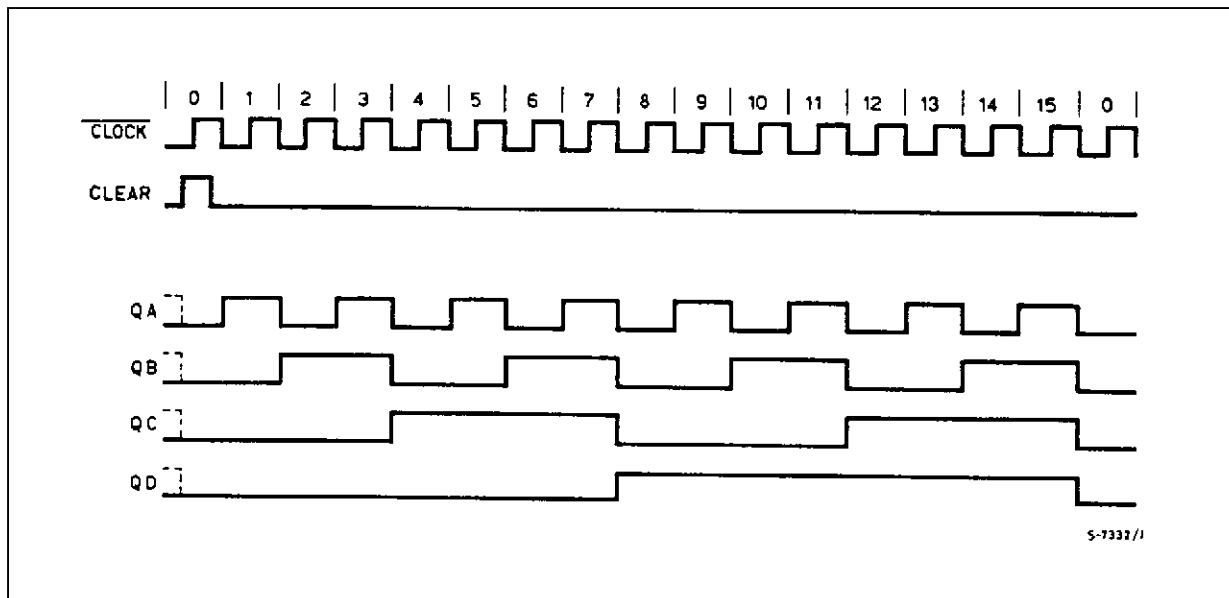
X: Don't Care

COUNT	OUTPUT			
	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

LOGIC DIAGRAM



TIMING CHART

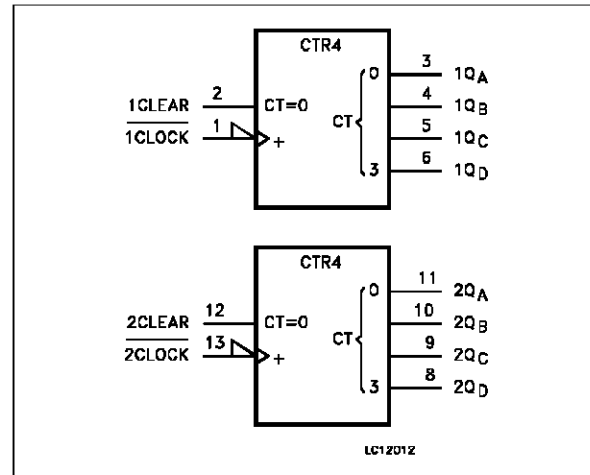


## M54/M74HCT393

### PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 13	1 CLOCK 2 CLOCK	Clock Input (HIGH to LOW Edge triggered)
2, 12	1 CLEAR 2 CLEAR	Asynchronous Master Reset Inputs
3, 4, 5, 6	1QA to 1QD	Flip Flop Outputs
11, 10, 9, 8	2QA to 2QD	Flip Flop Outputs
7	GND	Ground (0V)
14	V <sub>CC</sub>	Positive Supply Voltage

### IEC LOGIC SYMBOL



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	-0.5 to +7	V
V <sub>I</sub>	DC Input Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
V <sub>O</sub>	DC Output Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	DC Input Diode Current	± 20	mA
I <sub>OK</sub>	DC Output Diode Current	± 20	mA
I <sub>O</sub>	DC Output Source Sink Current Per Output Pin	± 25	mA
I <sub>CC</sub> or I <sub>GND</sub>	DC V <sub>CC</sub> or Ground Current	± 50	mA
P <sub>D</sub>	Power Dissipation	500 (*)	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(\*) 500 mW: ± 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	4.5 to 5.5	V
V <sub>I</sub>	Input Voltage	0 to V <sub>CC</sub>	V
V <sub>O</sub>	Output Voltage	0 to V <sub>CC</sub>	V
T <sub>op</sub>	Operating Temperature: <b>M54HC Series</b> <b>M74HC Series</b>	-55 to +125 -40 to +85	°C °C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (V <sub>CC</sub> = 4.5 to 5.5V)	0 to 500	ns

## DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value						Unit		
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC			
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.	
V <sub>IH</sub>	High Level Input Voltage	4.5 to 5.5		2.0			2.0		2.0		V	
V <sub>IL</sub>	Low Level Input Voltage	4.5 to 5.5				0.8		0.8		0.8	V	
V <sub>OH</sub>	High Level Output Voltage	4.5	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = -20 μA	4.4	4.5		4.4		4.4	V	
				I <sub>O</sub> = -4.0 mA	4.18	4.31		4.13		4.10		
V <sub>OL</sub>	Low Level Output Voltage	4.5	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA		0.0	0.1		0.1		0.1	V
				I <sub>O</sub> = 4.0 mA		0.17	0.26		0.33		0.4	
I <sub>I</sub>	Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND				±0.1		±1		±1	μA
I <sub>CC</sub>	Quiescent Supply Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND				4		40		80	μA
ΔI <sub>CC</sub>	Additional worst case supply current	5.5	Per Input pin V <sub>I</sub> = 0.5V or V <sub>I</sub> = 2.4V Other Inputs at V <sub>CC</sub> or GND				2.0		2.9		3.0	mA

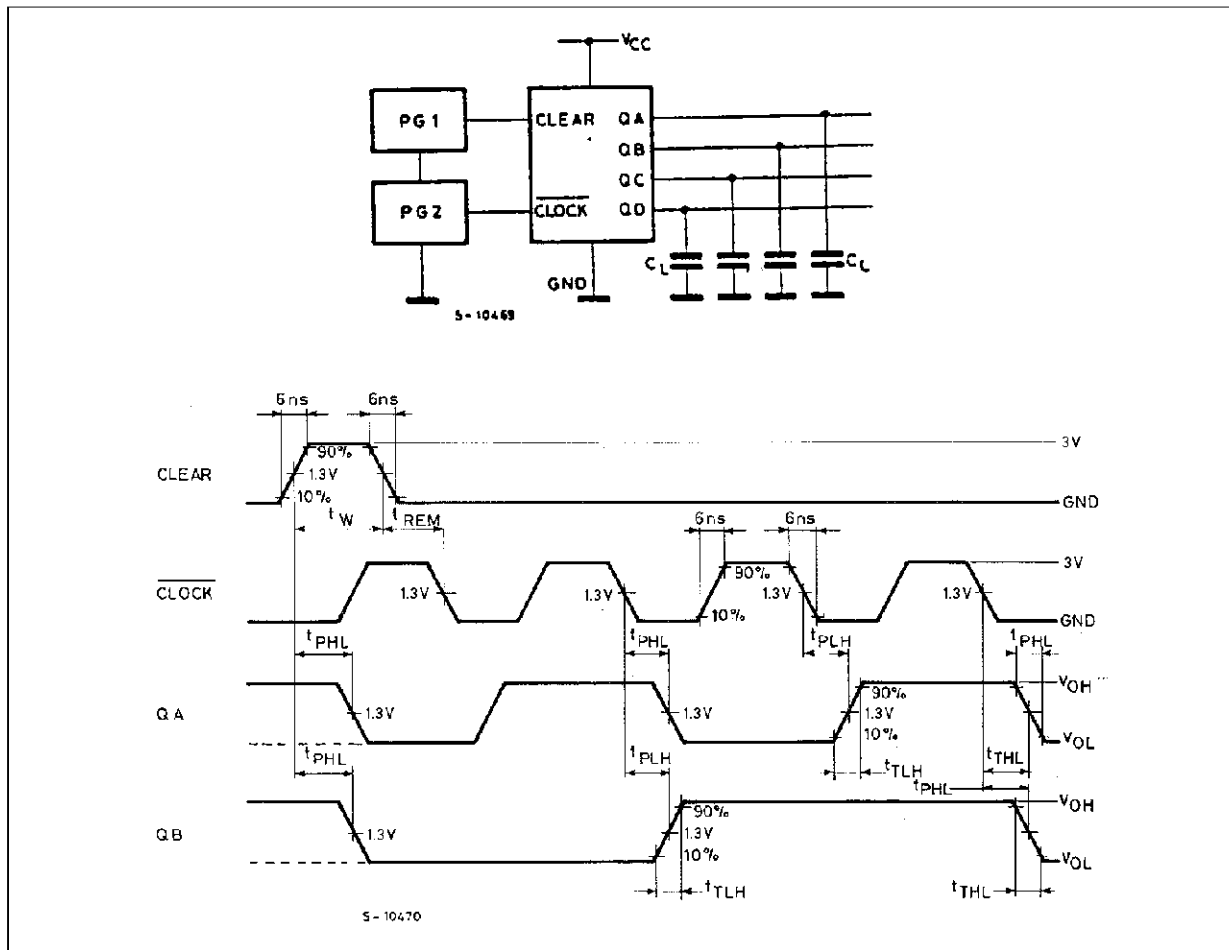
## M54/M74HCT393

### AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

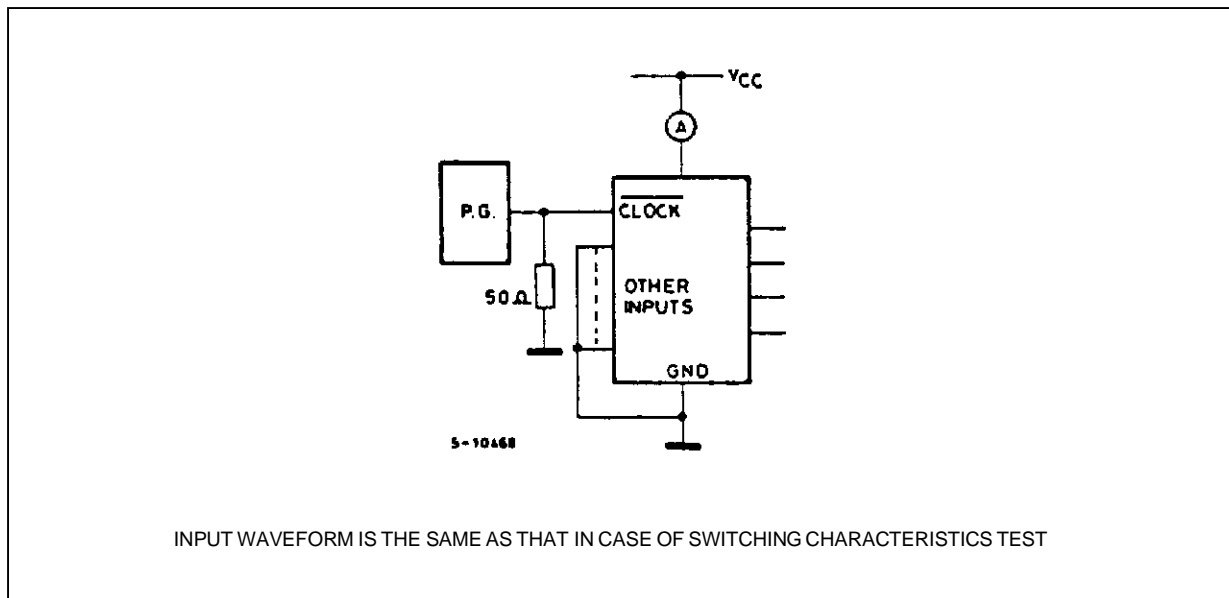
Symbol	Parameter	Test Conditions		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t <sub>TLH</sub> t <sub>THL</sub>	Output Transition Time	4.5			8	15		19		22	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (CLOCK - QA)	4.5			19	30		38		45	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (CLOCK - QB)	4.5			24	37		46		56	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (CLOCK - QC)	4.5			28	43		54		65	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (CLOCK - QD)	4.5			33	51		64		77	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (CLEAR - Qn)	4.5			20	31		39		47	ns
f <sub>MAX</sub>	Maximum Clock Frequency	4.5		4.2	80		34				MHz
t <sub>W(H)</sub> t <sub>W(L)</sub>	Minimum Pulse Width (CLOCK)	4.5			8	15		19		22	ns
t <sub>W(H)</sub>	Minimum Pulse Width (CLEAR)	4.5			8	15		19		22	ns
t <sub>REM</sub>	Minimum Removal Time	4.5				5		6		8	ns
C <sub>IN</sub>	Input Capacitance				5	10		10		10	pF
C <sub>PD</sub> (*)	Power Dissipation Capacitance				66						pF

(\*) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$  (per Flip Flop)

SWITCHING CHARACTERISTICS TEST WAVEFORM

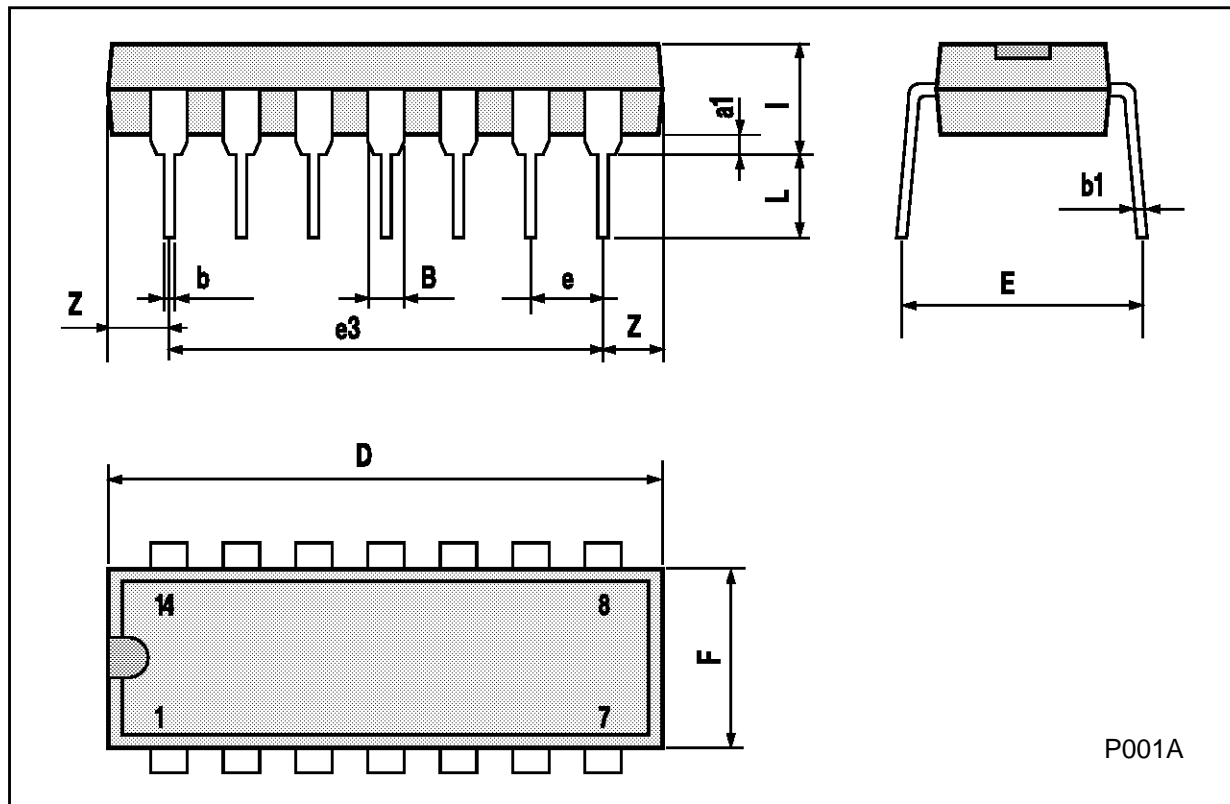


TEST CIRCUIT Icc (Opr.)



**Plastic DIP14 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

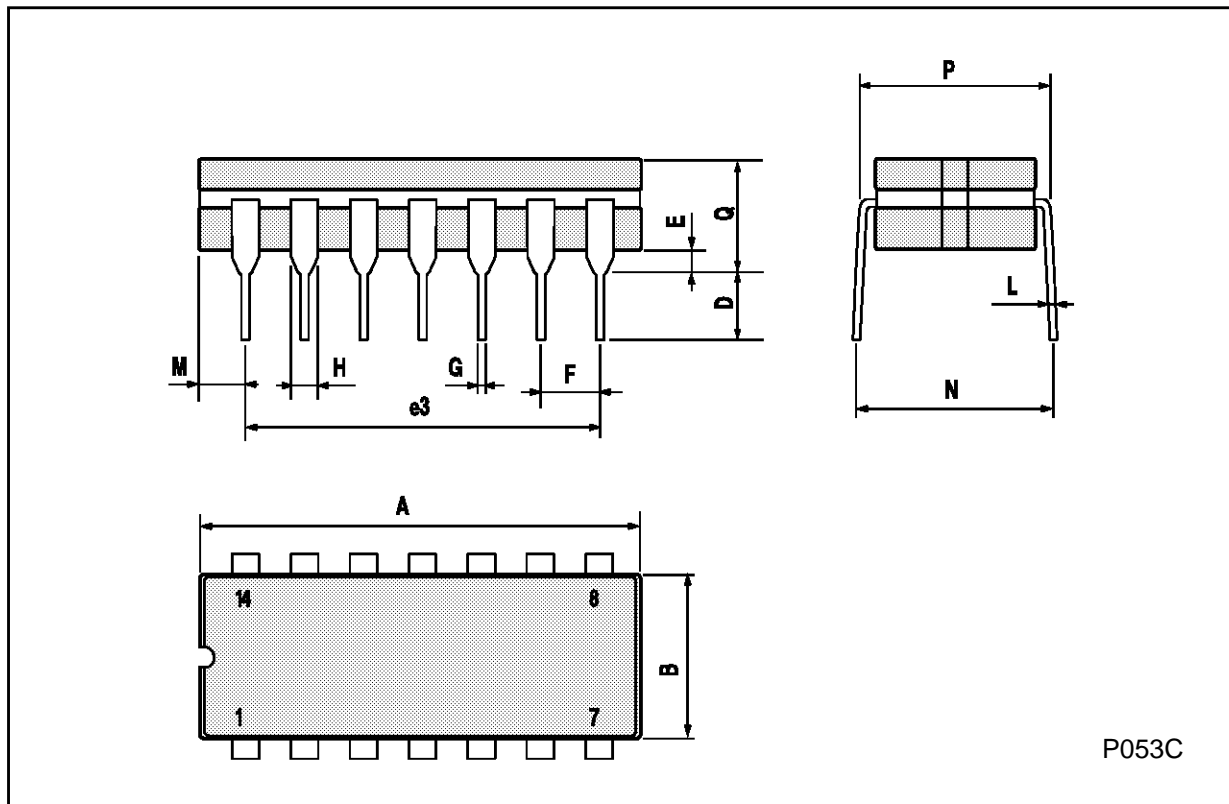


P001A



**Ceramic DIP14/1 MECHANICAL DATA**

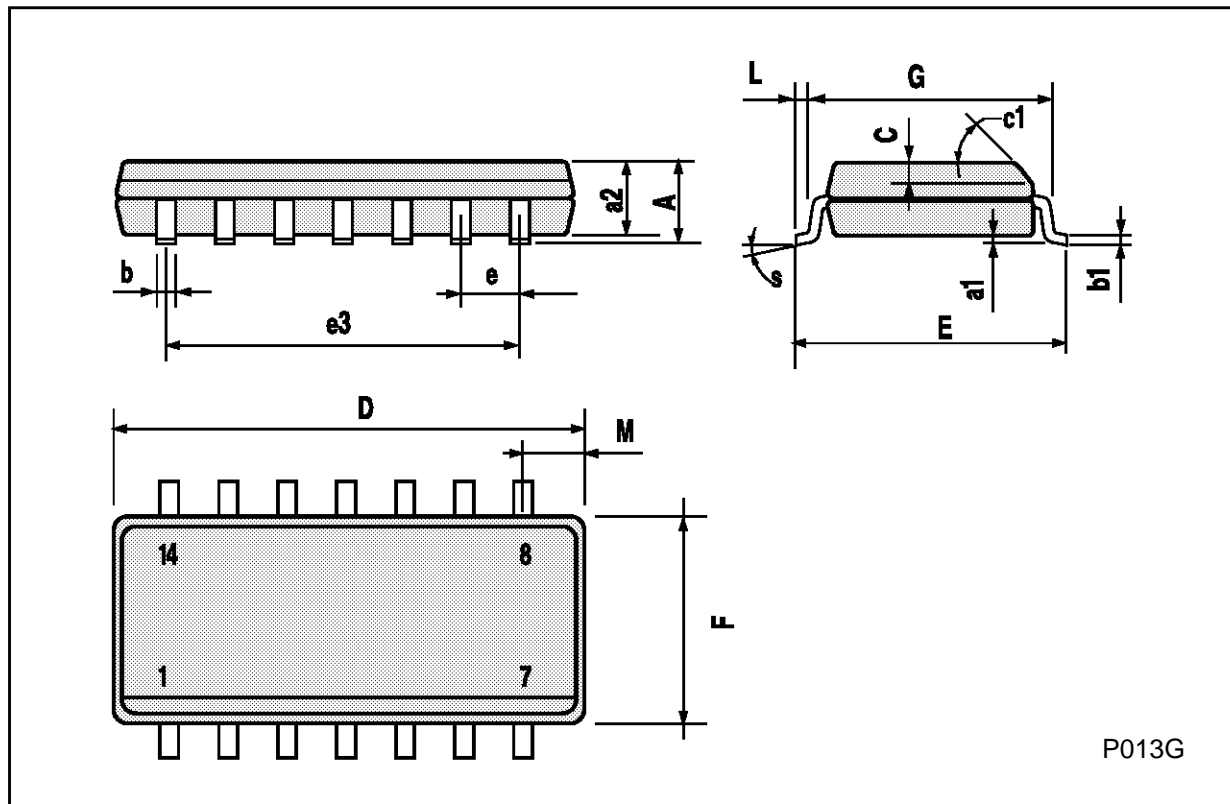
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7.0			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		15.24			0.600	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.54	0.060		0.100
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



P053C

SO14 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



P013G

## PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



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