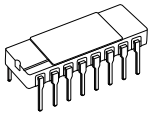
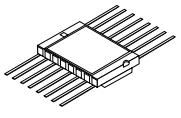
M54HC590

RAD-HARD 8 BINARY COUNTER REGISTER WITH 3 STATE OUTPUT

- HIGH SPEED:
  f_{MAX} = 61 MHz (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION:
  I_{CC} = 4μA(MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY:
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 6mA (MIN) for QA ~ QH OUTPUT
  $|I_{OH}| = I_{OL}$ = 4mA (MIN) for RCO OUTPUT
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 54 SERIES 590
- SPACE GRADE-1: ESA SCC QUALIFIED
- 50 krad QUALIFIED, 100 krad AVAILABLE ON REQUEST
- NO SEL UNDER HIGH LET HEAVY IONS IRRADIATION
- DEVICE FULLY COMPLIANT WITH SCC-9204-071



DILC-16



FPC-16

ORDER CODES

PACKAGE	FM	EM
DILC	M54HC590D	M54HC590D1
FPC	M54HC590K	M54HC590K1

DESCRIPTION

The M54HC590 is an high speed CMOS 8-BIT BINARY COUNTER REGISTER (3 STATE) fabricated with silicon gate C^2MOS technology.
This device contains an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features a direct clear input $\overline{CCLR}$ and a count enable input $\overline{CCKEN}$. For cascading, a ripple carry output $\overline{RCO}$ is provided. Expansion is easily accomplished by tying $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage, etc. Both the counter and register clocks are positive edge triggered. If the user wishes to connect both clocks together, the counter state will always be one count ahead of the register. Internal circuitry prevents clocking from the clock enable. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION

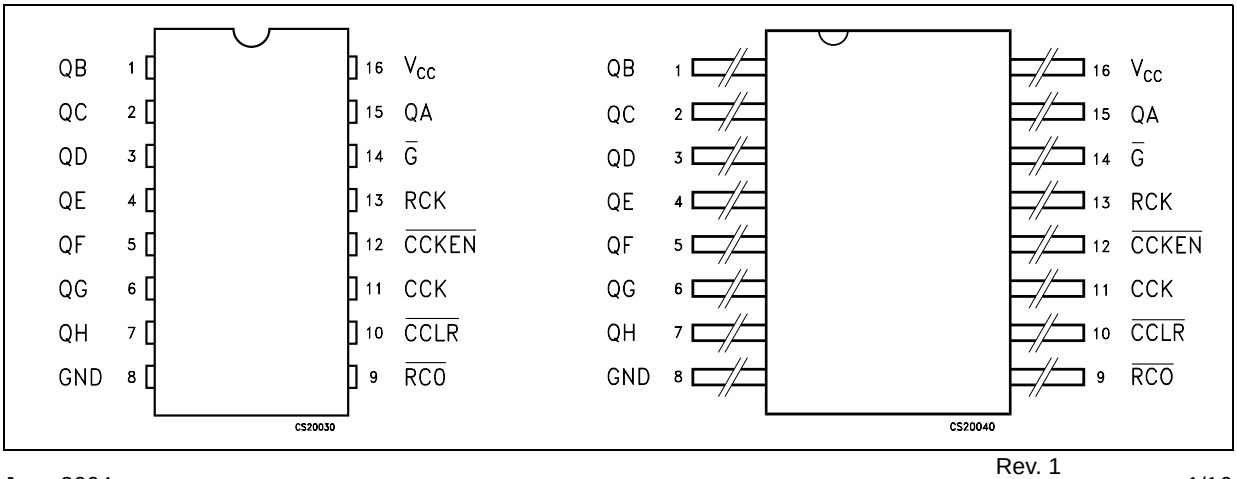


Figure 1: IEC Logic Symbols

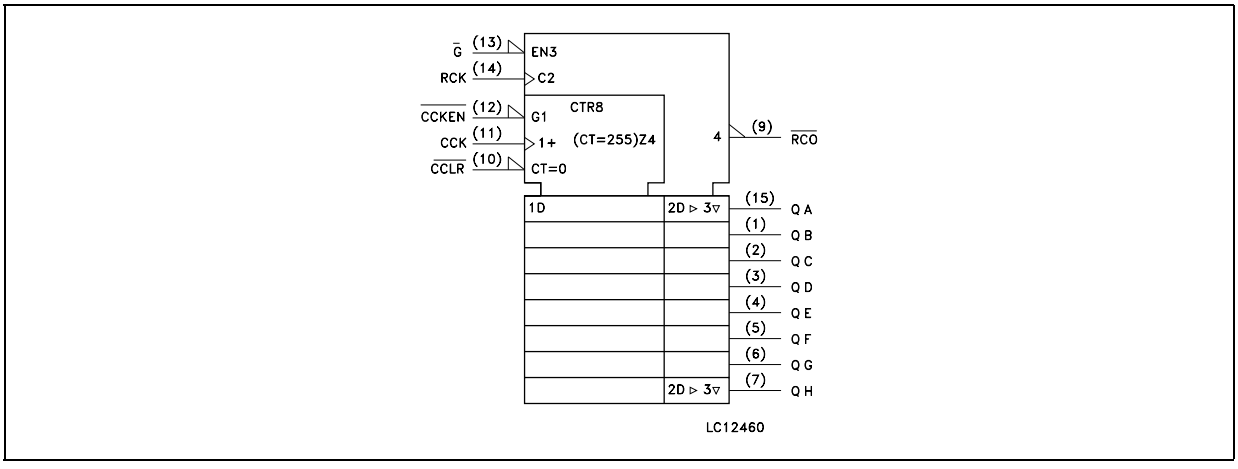


Figure 2: Input And Output Equivalent Circuit

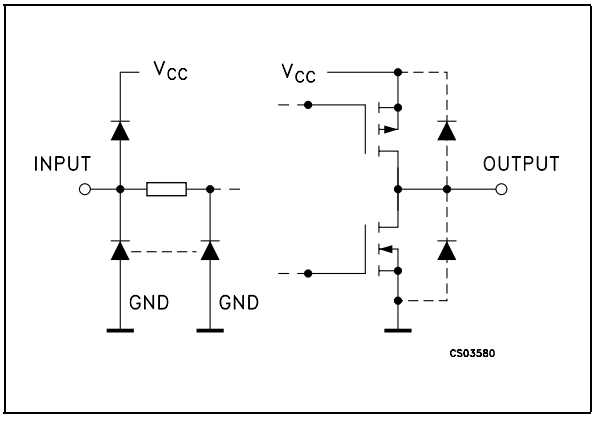


Table 1: Pin Description

PIN N°	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 15	QA to QH	Outputs
11	CCK	Counter Clock Input
12	$\overline{CCKEN}$	Counter Clock Enable Input
13	RCK	Register Clock Input
9	$\overline{RCO}$	Ripple Carry Output
14	G	Output Enable Input
10	$\overline{CCLR}$	Counter Clear Input
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

Table 2: Truth Table

INPUTS					OUTPUT
$\overline{G}$	RCK	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	
H	X	X	X	X	Q OUTPUTS DISABLE
L	X	X	X	X	Q OUTPUTS ENABLE
X	⌐	X	X	X	COUNTER DATA IS STORED INTO REGISTER
X	⌐	X	X	X	REGISTER STAGE IS NOT CHANGED
X	X	L	X	X	COUNTER CLEAR
X	X	H	L	⌐	ADVANCE ONE COUNT
X	X	H	L	⌐	NO COUNT
X	X	H	H	X	NO COUNT

X: Don't Care
RCO = QA'·QB'·QC'·QD'·QE'·QF'·QG'·QH' (QA' to QH': INTERNAL OUTPUTS OF THE COUNTER)

Figure 3: Logic Diagram

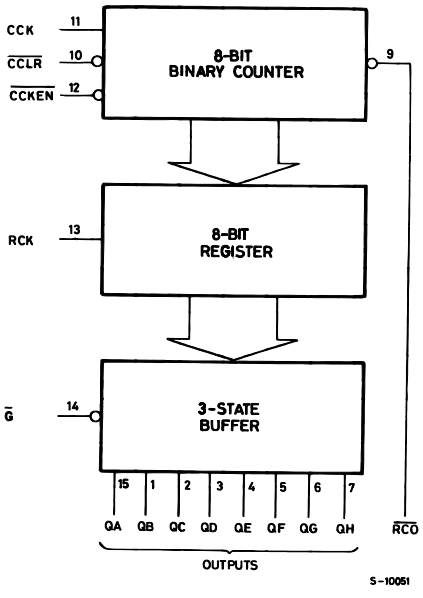
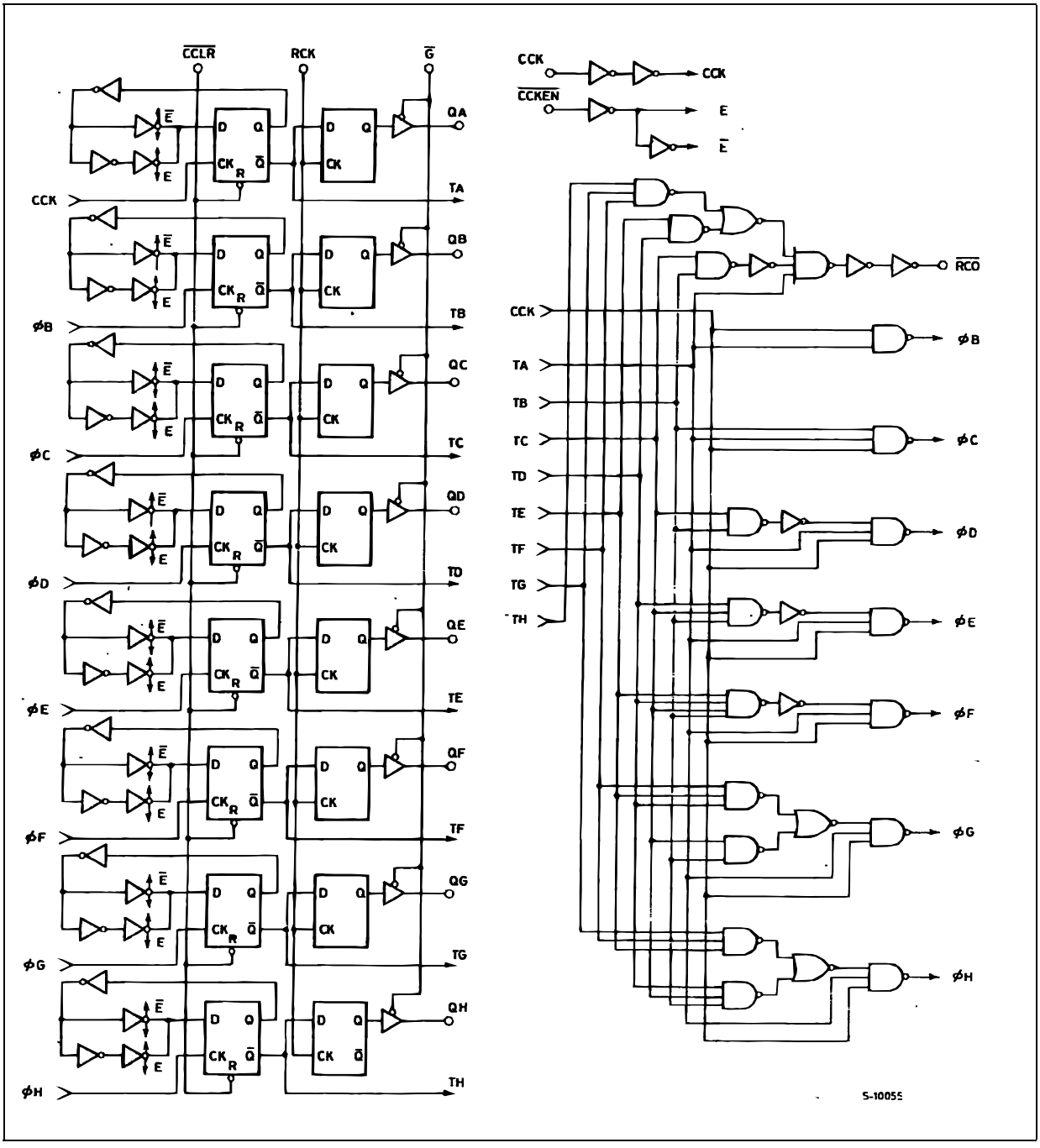


Figure 4: Logic Diagram



This logic diagram has not be used to estimate propagation delays

Figure 5: Timing Chart

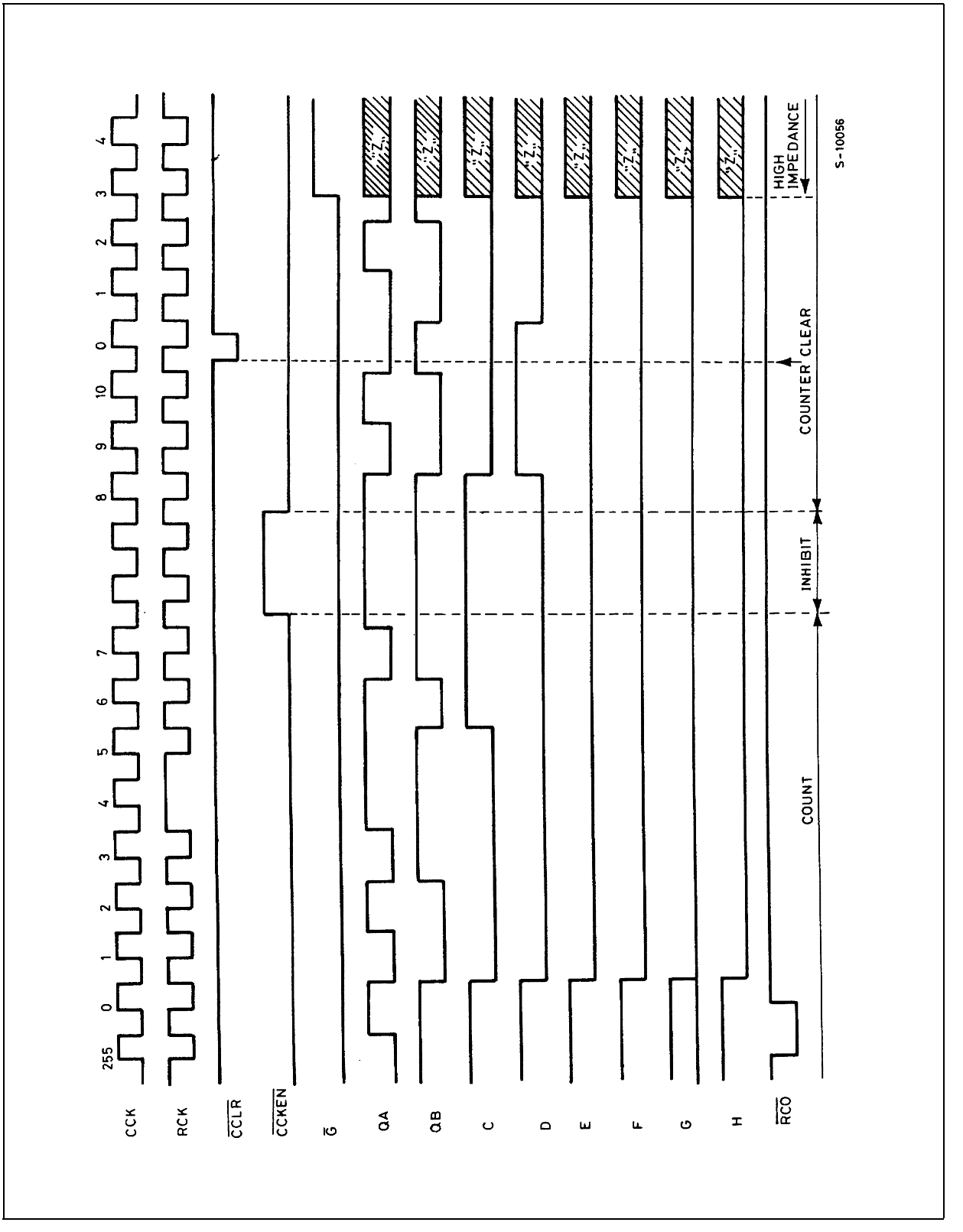


Table 3: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current per Output PIN (RCO) (QA - QH)	± 25 ± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	420	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	265	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

Table 4: Recommended Operating Conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

Table 5: DC Specifications

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V_{OH}	High Level Output Voltage (for $\overline{RCO}$ Output)	2.0	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O=-20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O=-20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OH}	High Level Output Voltage (for QA to QH Outputs)	2.0	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O=-20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O=-20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O=-7.8 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage (for $\overline{RCO}$ Output)	2.0	I_O=20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O=20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O=4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O=5.2 mA		0.18	0.26		0.33		0.40	
V_{OL}	Low Level Output Voltage (for QA to QH Outputs)	2.0	I_O=20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O=20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O=6.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O=7.8 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND			± 0.1		± 1		± 1	µA
I_{OZ}	High Impedance Output Leakage Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND			± 0.5		± 5		± 10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND			4		40		80	µA

Table 6: AC Electrical Characteristics (C_L = 50 pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{TLH} t_{THL}	Output Transition Time ($\overline{RCO}$)	2.0	50			30	75		95		115	ns
		4.5				8	15		19		23	
		6.0				7	13		16		20	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CCK}$ - $\overline{RCO}$)	2.0	50			56	165		205		250	ns
		4.5				19	33		41		50	
		6.0				16	28		35		43	
t_{PLH}	Propagation Delay Time ($\overline{CCLR}$ - $\overline{RCO}$)	2.0	50			53	175		220		265	ns
		4.5				21	35		44		53	
		6.0				18	30		37		45	
t_{PLH} t_{PHL}	Propagation Delay Time (RCK - Q)	2.0	50			48	145		180		220	ns
		4.5				17	29		36		44	
		6.0				14	25		31		37	
		2.0	150			60	185		230		280	ns
		4.5				21	37		46		56	
		6.0				18	31		39		48	
t_{PZL} t_{PZH}	High Impedance Output Enable Time	2.0	50	R_L = 1 KΩ		39	105		130		160	ns
		4.5				13	21		26		32	
		6.0				11	18		22		27	
		2.0	150	R_L = 1 KΩ		51	135		170		205	ns
		4.5				17	27		34		41	
		6.0				14	23		29		35	
t_{PLZ} t_{PHZ}	High Impedance Output Disable Time	2.0	50	R_L = 1 KΩ		28	105		130		160	ns
		4.5				14	21		26		32	
		6.0				12	18		22		27	
f_{MAX}	Maximum Clock Frequency	2.0	50		6.6	13		5.2		4.4		MHz
		4.5			33	52		26		22		
		6.0			39	61		31		26		
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CCK, RCK)	2.0	50			36	100		125		145	ns
		4.5				9	20		25		29	
		6.0				8	17		21		25	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CCLR}$)	2.0	50			32	75		95		110	ns
		4.5				8	15		19		22	
		6.0				7	13		16		19	
t_s	Minimum Set-up Time (CCKEN - CCK)	2.0	50			44	100		125		150	ns
		4.5				11	20		25		30	
		6.0				9	17		21		26	
$t_{s(H)}$	Minimum Set-up Time (CCK - RCK)	2.0	50			76	175		220		255	ns
		4.5				19	35		44		51	
		6.0				16	30		37		43	
t_h	Minimum Hold Time	2.0	50				0		0		0	ns
		4.5					0		0		0	
		6.0					0		0		0	

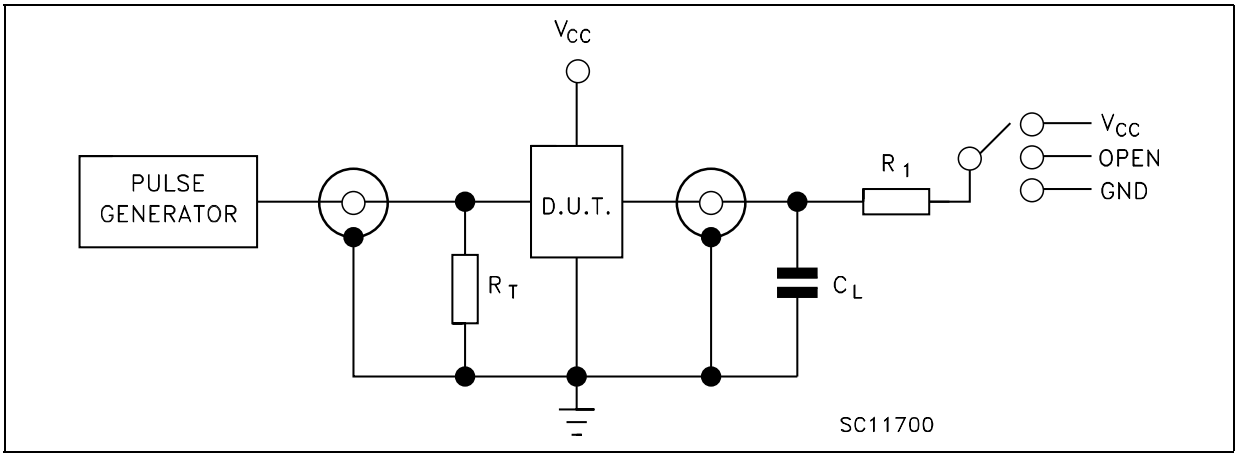
Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{REM}	Minimum Removal Time (CCLR)	2.0	50			28	75		95		110	ns
		4.5				7	15		19		22	
		6.0				6	13		16		19	

Table 7: Capacitive Characteristics

Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)			T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance					5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)					40						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

Figure 6: Test Circuit



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{CC}
t_{PZH}, t_{PHZ}	GND

C_L = 50pF/150pF or equivalent (includes jig and probe capacitance)
R_1 = 1KΩ or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

Figure 7: Waveform - Propagation Delay, Minimum Pulse Width (f=1MHz; 50% duty cycle)

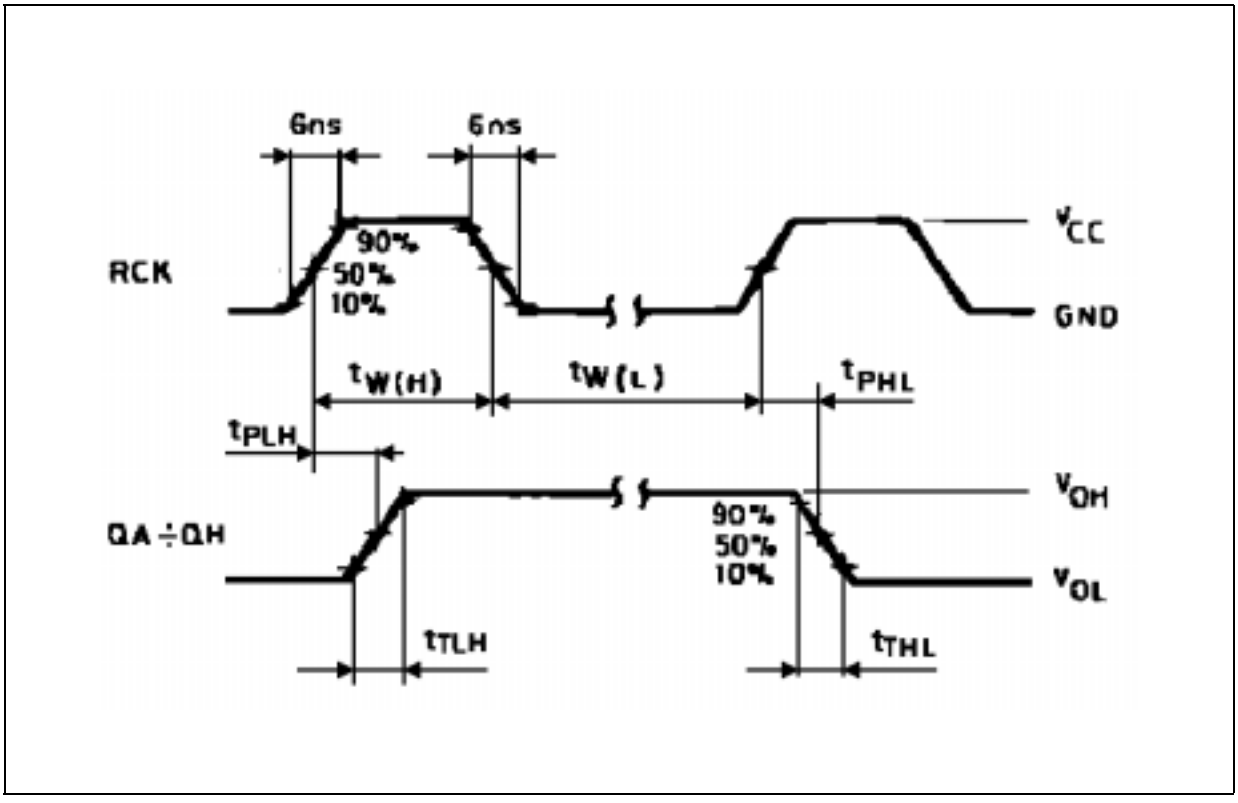


Figure 8: Waveform - Minimum Setup And Hold Time (f=1MHz; 50% duty cycle)

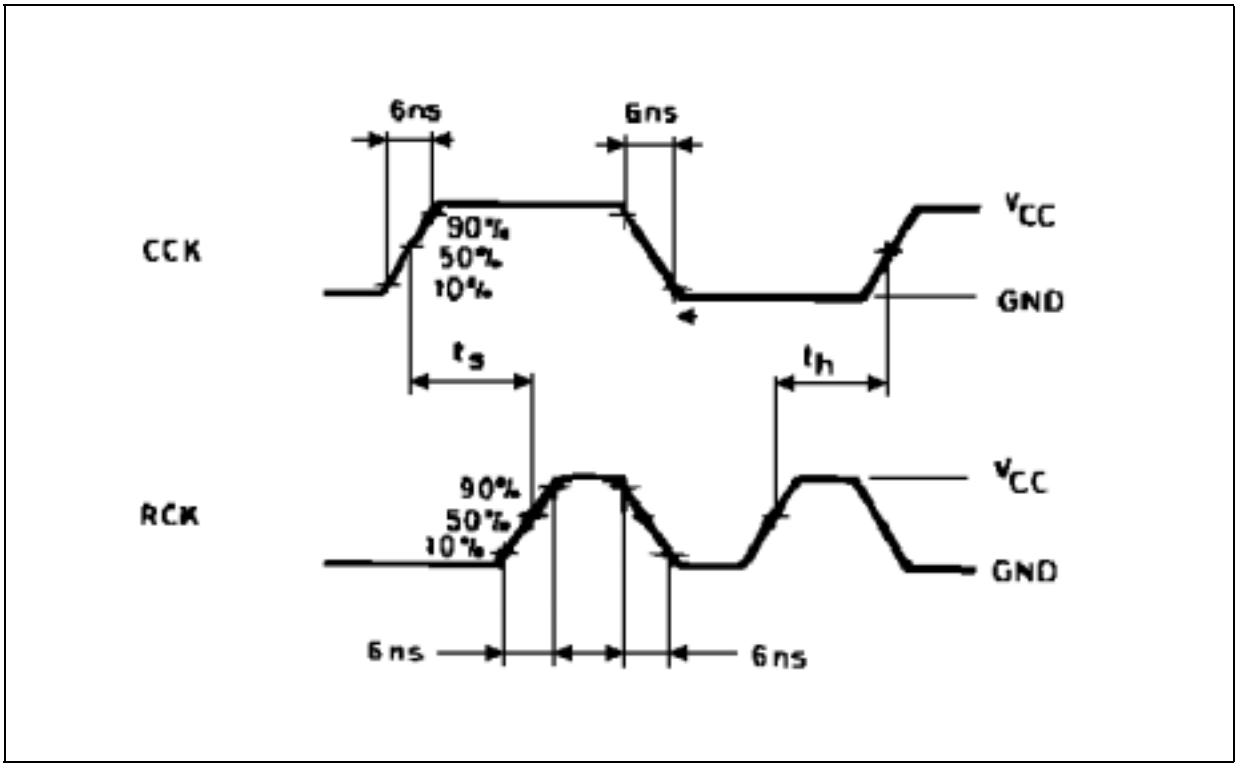


Figure 9: Waveform - Propagation Delay Time (f=1MHz; 50% duty cycle)

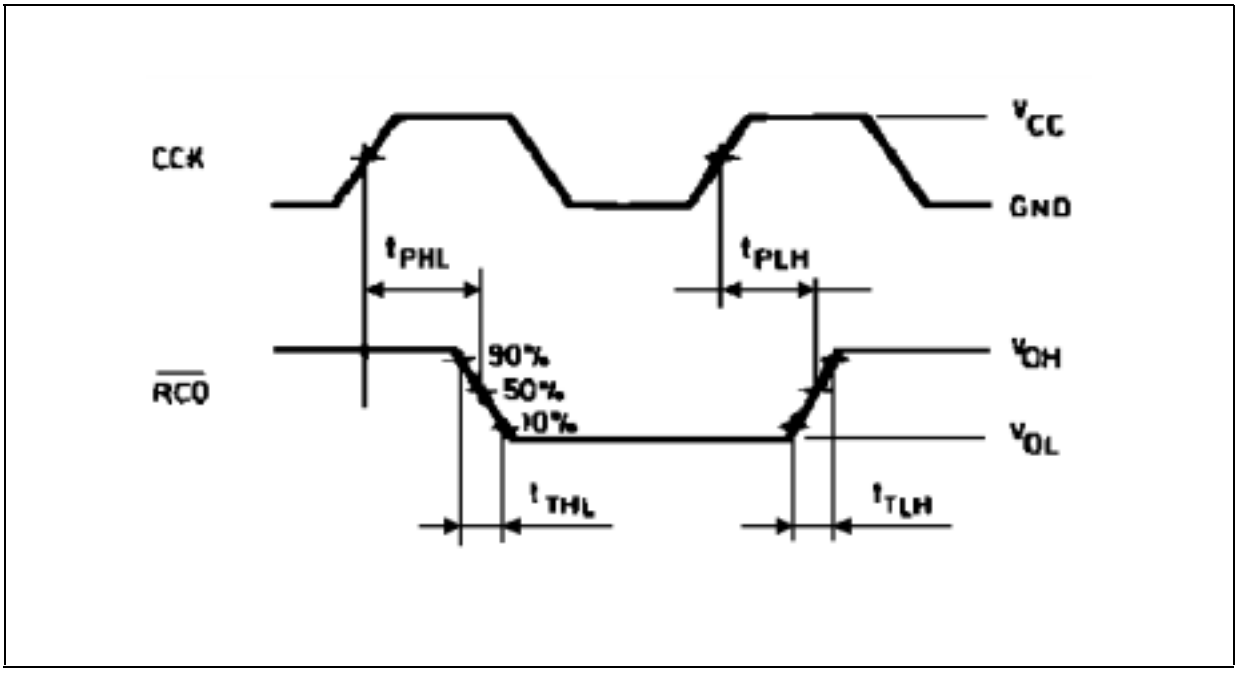


Figure 10: Waveform - Minimum Setup And Hold Time (f=1MHz; 50% duty cycle)

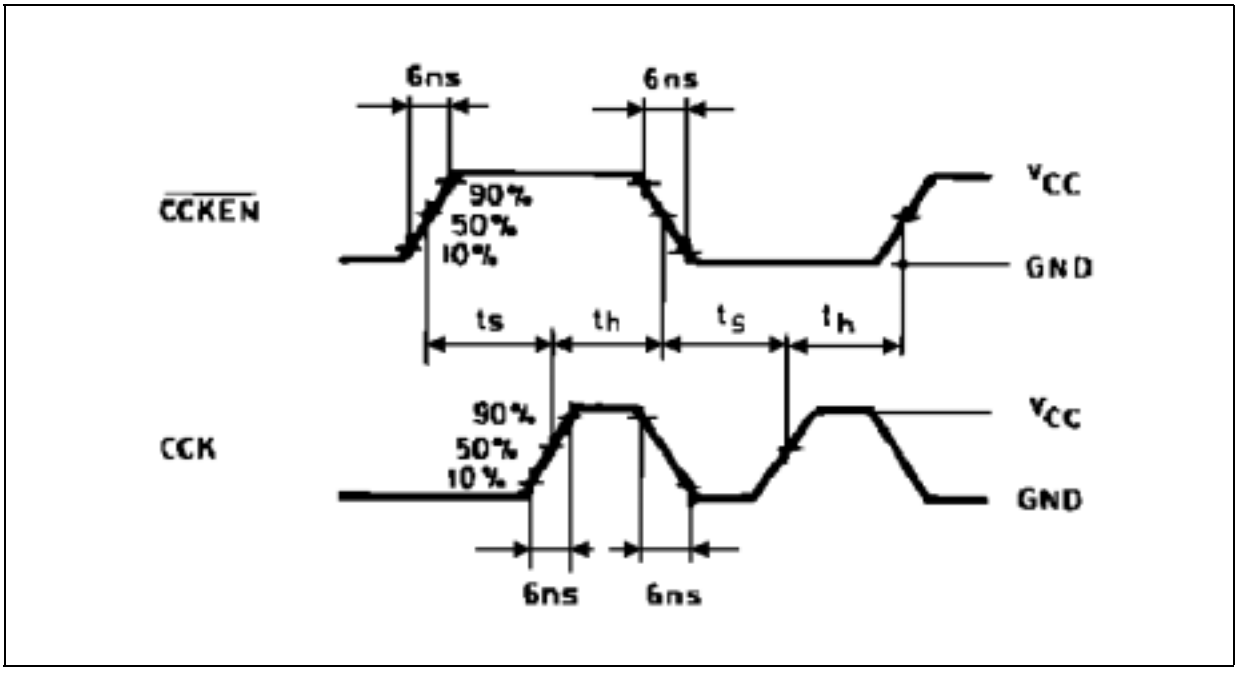


Figure 11: Waveform - Minimum Pulse Width, Removal Time (f=1MHz; 50% duty cycle)

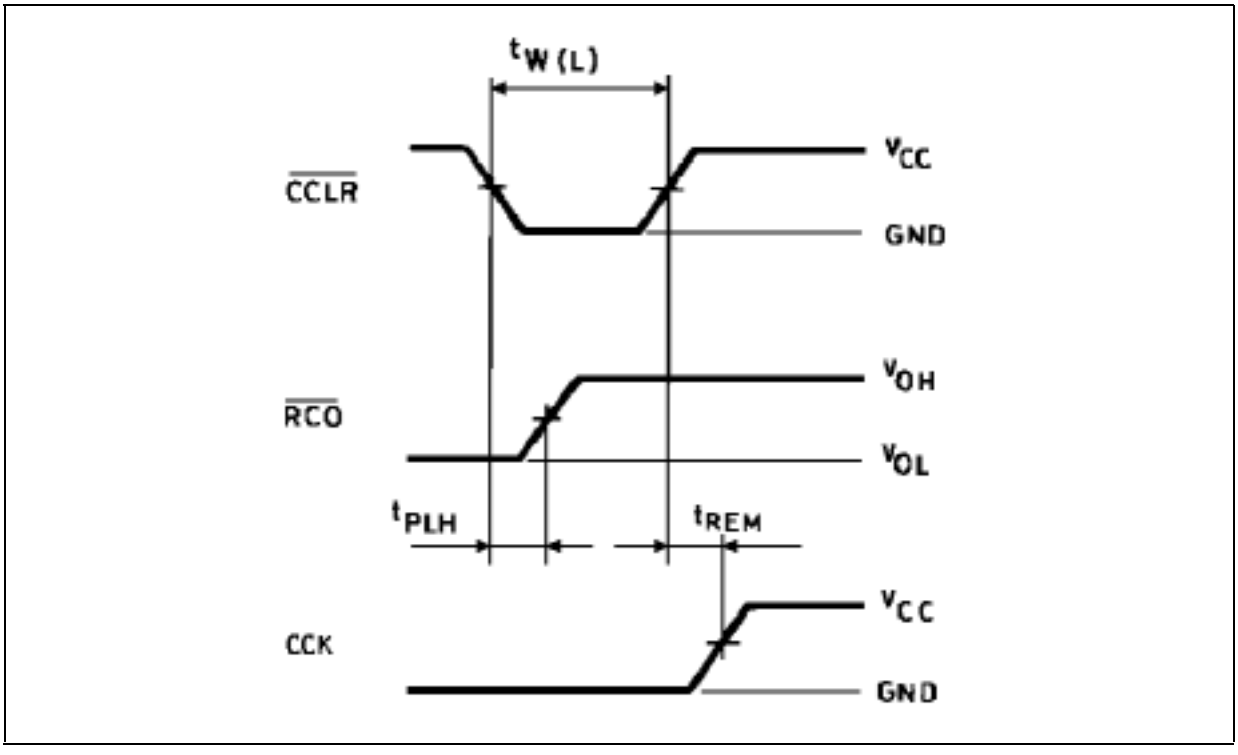
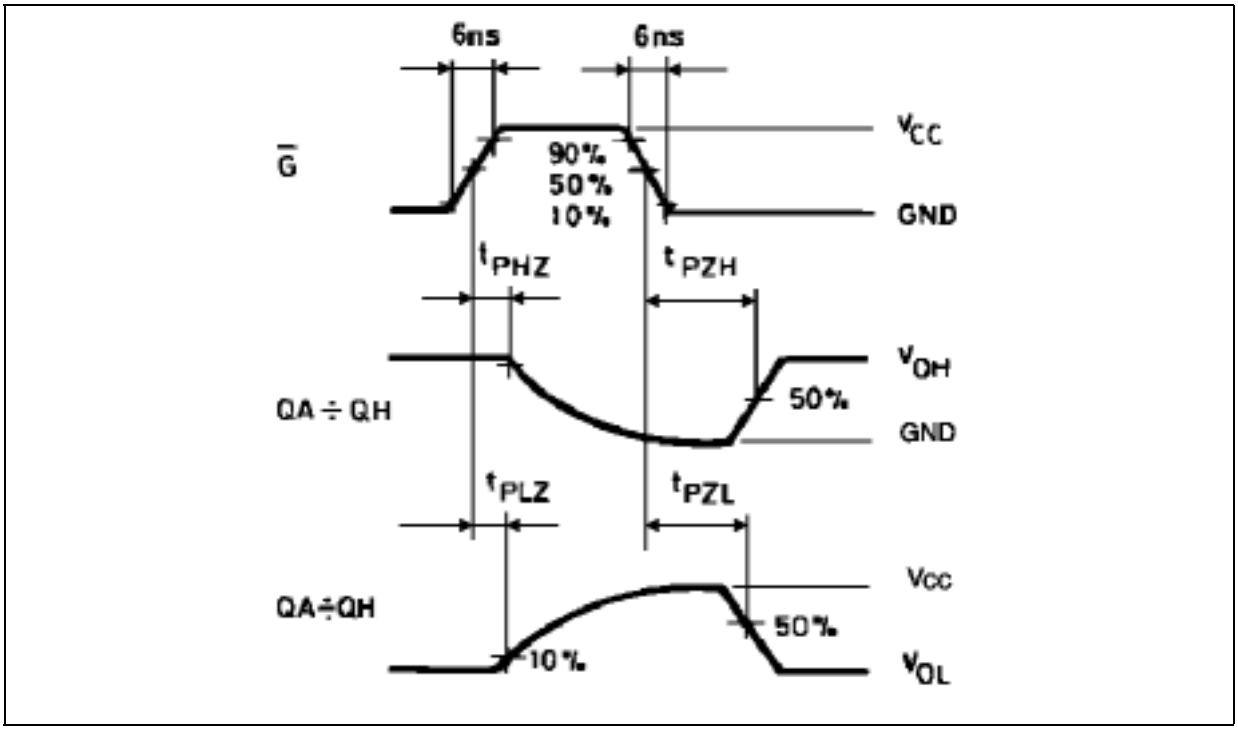
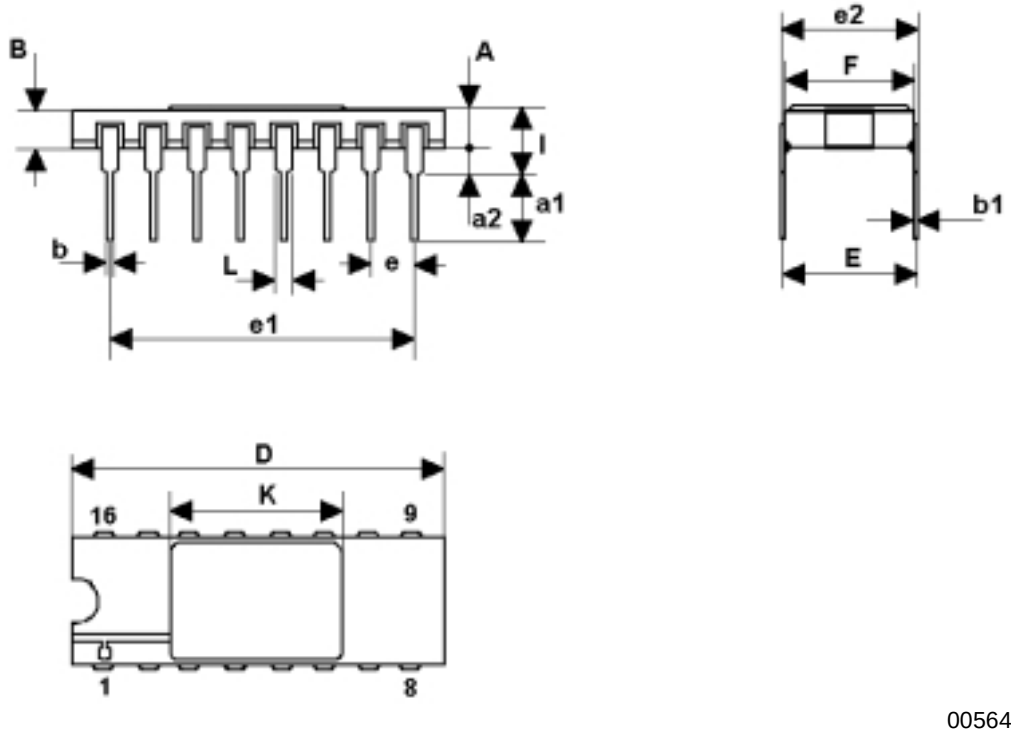


Figure 12: Waveform - Output Enable And Disable Time (f=1MHz; 50% duty cycle)



DILC-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.1		2.71	0.083		0.107
a1	3.00		3.70	0.118		0.146
a2	0.63	0.88	1.14	0.025	0.035	0.045
B	1.82		2.39	0.072		0.094
b	0.40	0.45	0.50	0.016	0.018	0.020
b1	0.20	0.254	0.30	0.008	0.010	0.012
D	20.06	20.32	20.58	0.790	0.800	0.810
E	7.36	7.62	7.87	0.290	0.300	0.310
e		2.54			0.100	
e1	17.65	17.78	17.90	0.695	0.700	0.705
e2	7.62	7.87	8.12	0.300	0.310	0.320
F	7.29	7.49	7.70	0.287	0.295	0.303
I			3.83			0.151
K	10.90		12.1	0.429		0.476
L	1.14		1.5	0.045		0.059



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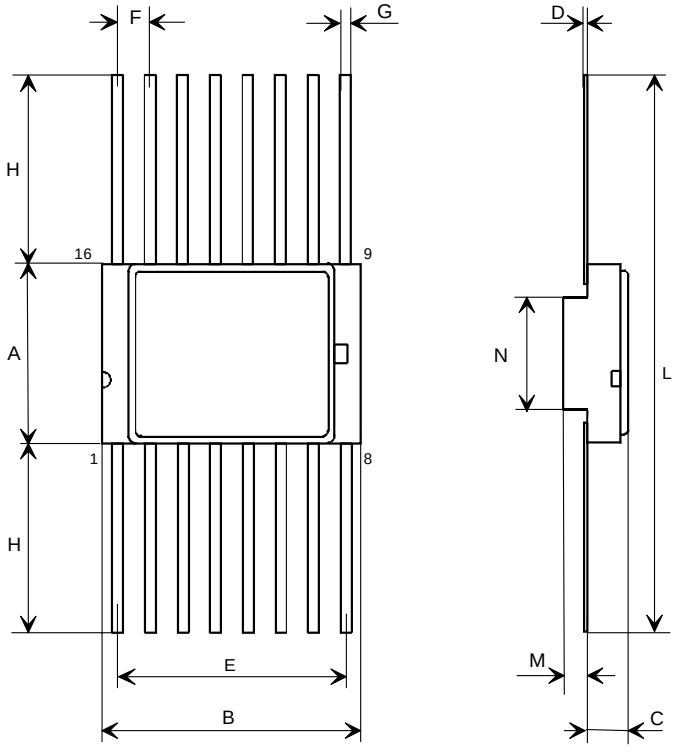
FPC-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	6.75	6.91	7.06	0.266	0.272	0.278
B	9.76	9.94	10.14	0.384	0.392	0.399
C	1.49		1.95	0.059		0.077
D	0.102	0.127	0.152	0.004	0.005	0.006
E	8.76	8.89	9.01	0.345	0.350	0.355
F		1.27			0.050	
G	0.38	0.43	0.48	0.015	0.017	0.019
H	6.0			0.237		
L	18.75		22.0	0.738		0.867
M	0.33	0.38	0.43	0.013	0.015	0.017
N		4.31			0.170	



0016030E

Table 8: Revision History

Date	Revision	Description of Changes
01-Jun-2004	1	First Release

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