

BURST LOCK CLOCK GENERATOR

DESCRIPTION

The M52693SP is a semiconductor integrated circuit developed for analog signal processing of a picture-in-picture system, consisting of a sync separator, an ACC, a burst lock clock generator circuit, an analog switch and a clamp circuit, etc. It is also available on digital video signal systems other than the above.

FEATURES

- Low power dissipation of supply voltage 5.0V and circuit current 32mA (Typ.)
- Built-in 4fsc burst lock clock generator circuit required for digital video signal processing
- Small picture chroma level following main picture burst level
- Main picture pedestal level matching small picture pedestal level
- Built-in reference voltage source for A/D converter

APPLICATION

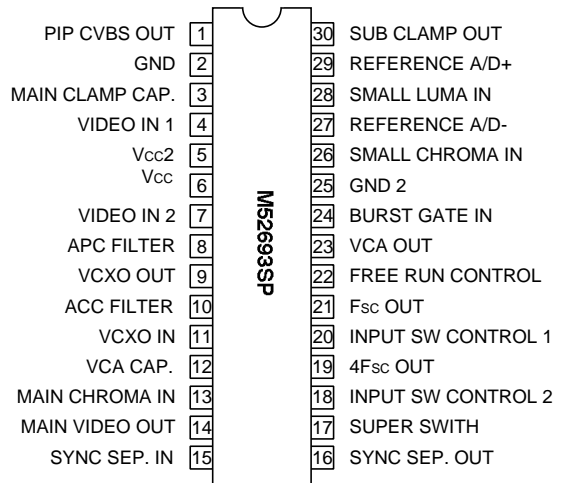
TV, VCR

RECOMMENDED OPERATING CONDITION

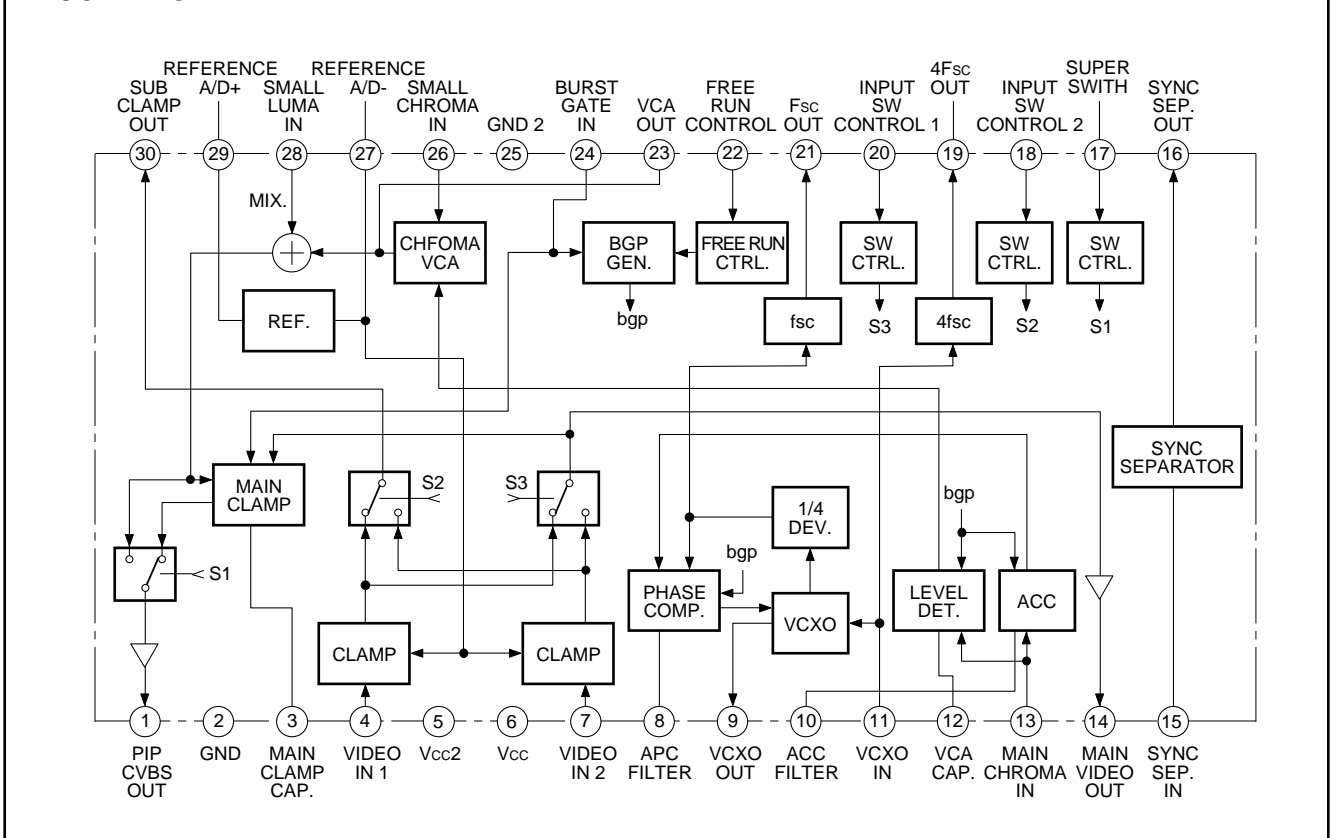
Supply voltage range..... 4.7 to 5.3V

Rated supply voltage.....5.0V

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
Vcc	Supply voltage	6.0	V
Pd	Power dissipation	1265	mW
Topr	Operating temperature	-20 to +75	°C
Tstg	Storage temperature	-40 to +125	°C

ELECTRICAL CHARACTERISTICS (cont.)

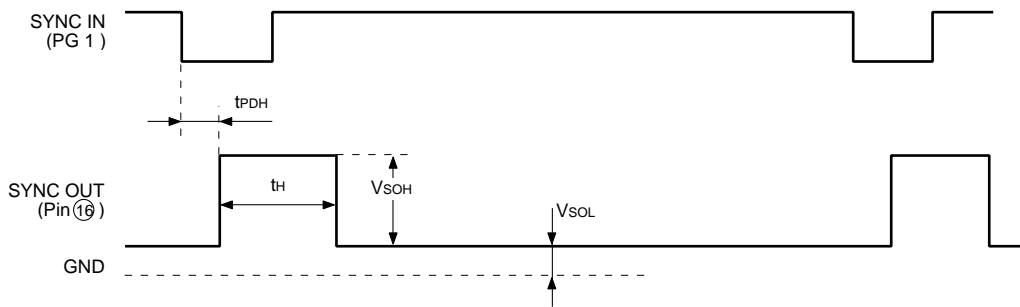
Symbol	Parameter	Test point	Test conditions																												Limits			Unit					
			Pin conditions														Switch conditions														Min.	Typ.	Max.						
			4	5	6	7	11	13	14	15	16	17	18	19	20	21	22	23	26	27	28	29	30	SW4	SW7	SW11	SW13	SW26	SW28	SW									
V4fscL	4fsc output voltage L	(19)	-	5.0 V	5.0 V	-	-	-	SG 2	-	1	PG	-	0 V	5.0 V	0 V	-	-	-	-	-	-	-	-	-	-	-	-	-	a	a	OFF	b	a	a	-	0.1	0.5	V
VfSCH	fsc output voltage H	(21)	-	5.0 V	5.0 V	-	-	-	SG 2	-	1	PG	-	0 V	5.0 V	0 V	-	-	-	-	-	-	-	-	-	-	-	-	-	a	a	OFF	b	a	a	3.4	3.9	-	V
VfscL	fsc output voltage L	(21)	-	5.0 V	5.0 V	-	-	-	SG 2	-	1	PG	-	0 V	5.0 V	0 V	-	-	-	-	-	-	-	-	-	-	-	-	-	a	a	OFF	b	a	a	-	0.1	0.5	V
4fsc	4fsc output frequency	(19)	-	5.0 V	5.0 V	-	-	-	SG 2	-	1	PG	-	0 V	5.0 V	0 V	-	-	-	-	-	-	-	-	-	-	-	-	a	a	OFF	b	a	a	-	14.318	-	MHz	
fsc	fsc output frequency	(21)	-	5.0 V	5.0 V	-	-	-	SG 2	-	1	PG	-	0 V	5.0 V	0 V	-	-	-	-	-	-	-	-	-	-	-	-	a	a	OFF	b	a	a	-	3.5795	-	MHz	
fcp (+)	Capture range (+)	(19)	-	5.0 V	5.0 V	-	-	-	SG 8	-	1	PG	-	0 V	5.0 V	0 V	-	-	-	-	-	-	-	-	-	-	-	a	a	OFF	b	a	a	400	650	-	Hz		
fcp (-)	Capture range (-)	(19)	-	5.0 V	5.0 V	-	-	-	SG 8	-	1	PG	-	0 V	5.0 V	0 V	-	-	-	-	-	-	-	-	-	-	-	a	a	OFF	b	a	a	-	-1200	-400	Hz		
C-IN	Chroma signal input level (burst)	(19)	-	5.0 V	5.0 V	-	-	-	SG2 ¹ SG2	-	1	PG	-	0 V	5.0 V	0 V	-	-	-	-	-	-	-	-	-	-	-	a	a	OFF	b	a	a	0.01	0.10	0.20	Vp-P		

ELECTRICAL CHARACTERISTICS TEST METHOD

VR

$VR = VRH - VRL$

V_{SOH}, V_{SOL}, t_H and t_{PDH}



Sync-in

Measure t_H and t_{PDH} when the input amplitude of pin ⑮ is 0.1V_{P-P}. Make sure that t_H and t_{PDH} are within the allowable range. When the input amplitude of pin ⑮ is 0.6V_{P-P}, make sure that t_H and t_{PDH} are within the allowable range.

If the voltage which appears at pin ⑳ when pin ⑮ is "H" is taken as V_{sub1}, and the voltage which appears at pin ⑳ when pin ⑮ is "L" is taken as V_{sub2}, the clamp offset is given by the following expression:

$DV_{SRB} = (V_{sub1} - V_{27}), (V_{sub2} - V_{27})$

V_{sub} and V_{SRB}

Measure pin ⑳ DC output voltage in correspondence to the "H" and "L" states of pin ⑮ .

G_{sub}

Measure pin ⑳ gain in correspondence to the "H" and "L" states of pin ⑮ .

CT_{sub}, C_{main}, and CT_{PIP}

Measure crosstalk under the following input conditions:

Parameter		Input signal	Pin connection Switching condition:Left Input condition:Right						
			4	7	17	18	20		
CT _{sub}	CT _{sub} 1	Sine wave Amplitude : 0.3V _{P-P} Frequency : 3.58MHz	b	IN	a	--	0V	5 ⇔ 0V	0V
	C _{tsub} 2		a	--	b	IN	0V	0 ⇔ 5V	0V
CT _{main}	CT _{main} 1		b	IN	a	--	0V	0V	5 ⇔ 0V
	CT _{main} 2		a	--	b	IN	0V	0V	0 ⇔ 5V
CT _{PIP}	CT _{PIP} 1		b	IN	a	--	0 ⇔ 5V	0V	5V
	CT _{PIP} 2		a	--	b	IN	0 ⇔ 5V	0V	0V

f_{BWsub}

Measure pin ⑳ frequency characteristics in correspondence to the "H" and "L" states of pin ⑮. Condition: -3dB

f_{BWmain}

Measure pin ⑭ frequency characteristics in correspondence to the "H" and "L" states of pin ⑳. Condition: -3dB

V_{main}

Measure pin ⑭ DC output voltage in correspondence to the "H" and "L" states of pin ⑳ .

V_{PIP}

If the voltage which appears at pin ① when pin ⑳ is "H" is taken as V_{pip1}, and the voltage which appears at pin ① when pin ⑳ is "L" is taken as V_{pip2}, V_{PIP} is given by the following expression:

$V_{PIP} = |V_{pip1} - V_{PIP}|, |V_{pip2} - V_{PIP}|$

G_{main}

Measure pin ⑭ gain in correspondence to the "H" and "L" states of pin ⑳ .

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GPIPS

Pin ② = 2.185V V_1 = Amplitude of pin ① V_{23} = Amplitude of pin ②③
 $GPIPS = 20 \log (V_1/V_{23})$

GPIP

Measure pin ① gain in correspondence to the "H" and "L" states of pin ②③ .

fBWPIP

Measure pin ① frequency characteristics in correspondence to the "H" and "L" states of pin ②③. Condition: -3dB

fBWPIPS

Condition: -3dB

CTPIPS

Apply 5.0V to pin ②③ . Define as V_{OS1} the amplitude which appears at pin ① a when pin ①⑦ is "H", and as V_{OM1} the amplitude which appears when pin ①⑦ is "L". Then apply 0V to pin ②③ . Define as V_{OS2} the amplitude which appears at pin ① when pin ①⑦ is "H", and as V_{OM2} the amplitude which appears at pin ① when "L".
 CTPIPS is given under the above conditions by the equation given below.

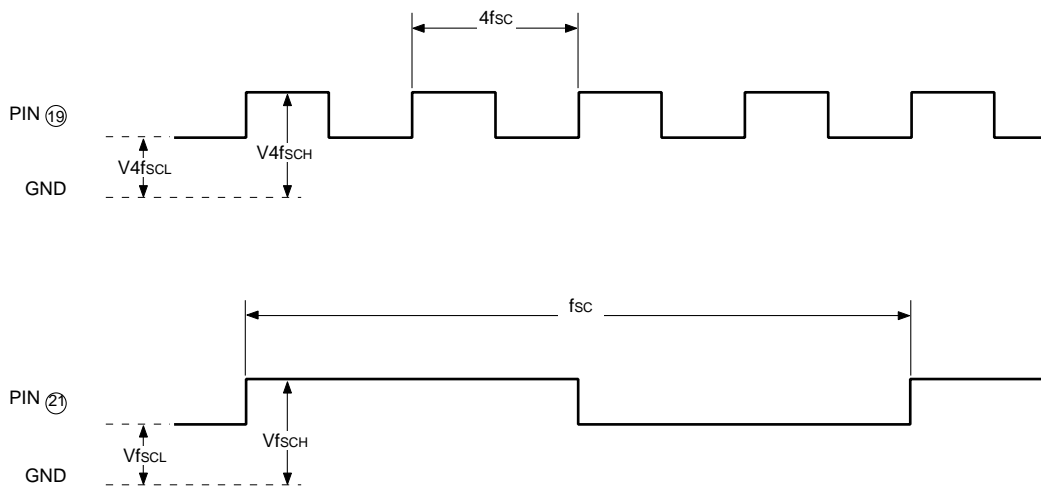
$CTPIPS = 20 \log (V_{OM1}/V_{OS1}), 20 \log (V_{OM2}/V_{OS2})$

VCA_{typ}, VCA_{max}, VCA_{min}, G_{max}, Lv_{ca}

$20 \log \{ (\text{amplitude of pin 23})/SG5 \}$

V_{4fSCH, L}; V_{fSCH, L}; 4f_{sc}; f_{sc}

Make sure that the input signal at pin ①③ is synchronous with the output signal at pin ①⑨ .



f_{cp} (+)

- 1) Raise the frequency of SG8 input signal so that the signal is synchronous with pin ①⑨ output signal.
- 2) Lower the SG8 frequency.
- 3) Measure the SG8 frequency (f_1) when the SG8 input signal is synchronous with the pin ①⑨ output signal.
- 4) $f_{cp}(+) = f_1 - f_c$ ($f_c = 3.579545\text{MHz}$)

f_{cp} (-)

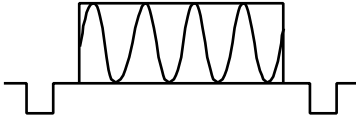
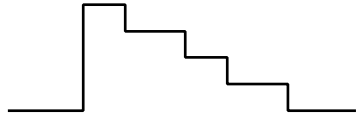
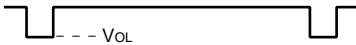
- 1) Lower the frequency of SG8 input signal so that the signal is synchronous with pin ①⑨ output signal.
- 2) Raise the SG8 frequency.
- 3) Measure the SG8 frequency (f_2) when the SG8 input signal is synchronous with the pin ①⑨ output signal.
- 4) $f_{cp}(-) = f_2 - f_c$ ($f_c = 3.579545\text{MHz}$)

C-IN

Make sure that the pin ①③ input signal is synchronous with the pin ①⑨ output signal when the input amplitude of pin ①③ is 0.20V_{P-P}. Then make sure that the pin ①③ input signal is synchronous with the pin ①⑨ output signal when the input amplitude is 0.01V_{P-P}.

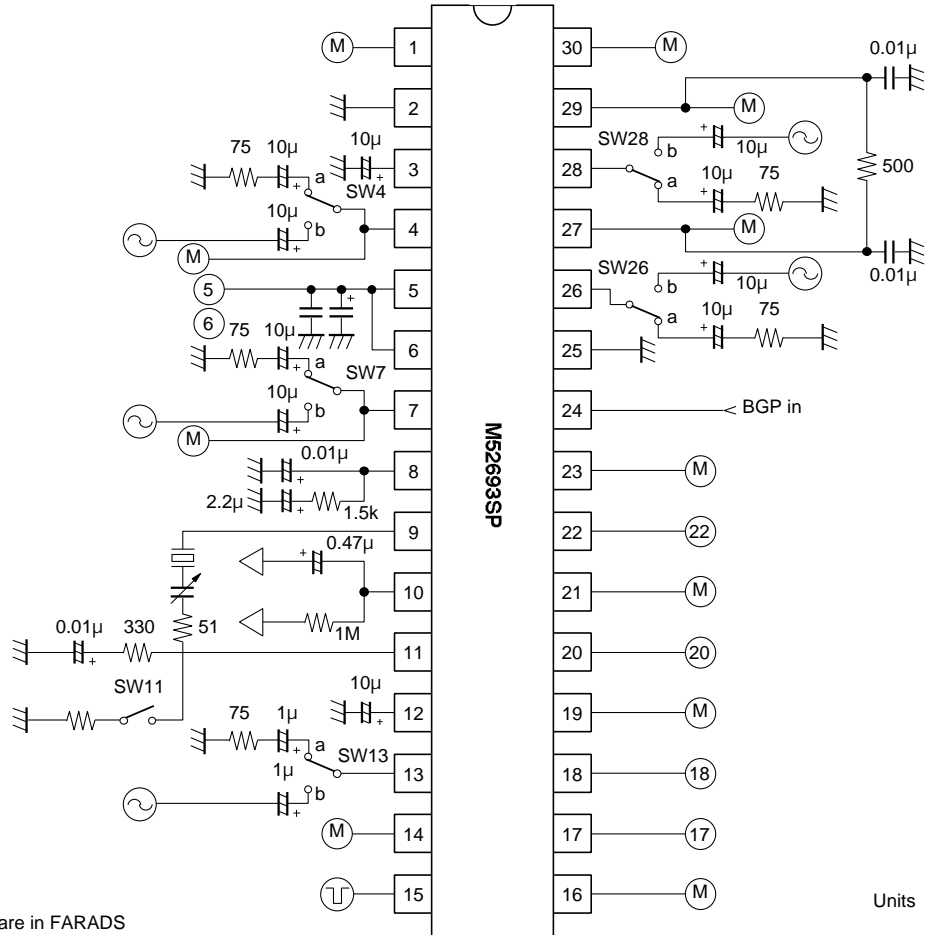
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INPUT SIGNAL

SG No.	Input signal	Remarks
SG1	NTSC system composite video signal (1V _{P-P})	- - -
SG2	Sine wave Frequency: 3.58MHz Amplitude : 0.1V _{P-P}	- - -
SG2'	Sine wave Frequency: 3.58MHz Amplitude : 0.2V _{P-P}	- - -
SG2''	Sine wave Frequency: 3.58MHz Amplitude : 0.01V _{P-P}	- - -
SG3	Sine wave Frequency: 3.58MHz Amplitude : 0.3V _{P-P}	
SG4	C-Sync + sine wave C-Sync Frequency: 15.734kHz Amplitude : 0.285V _{P-P} Sine wave Frequency: 1/10MHz Amplitude : 0.715V _{P-P}	
SG5	Sine wave Frequency: 3.58MHz Amplitude : 0.2V _{P-P}	- - -
SG6	Y signal Amplitude : 0.715V _{P-P}	
SG7	Sine wave Frequency: 1/10MHz Amplitude : 0.2V _{P-P}	- - -
SG8	Sine wave Frequency: Variable Amplitude : 0.1V _{P-P}	- - -
PG1	C-Sync Frequency: 15.734kHz Amplitude : 0.3V _{P-P} VOL=2.75V	
PG1'	C-Sync Amplitude : 0.1V _{P-P} 0.6V _{P-P}	- - -

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TEST CIRCUIT



Notes:

1. Capacitance values are in FARADS
2. Resistors are in OHMS
3. : Vcc : GND

Units Resistance :
Capacitance : F

TYPICAL CHARACTERISTICS

THERMAL DERATING (MAXIMUM RATING)

