



## M3028 Series SPECIFICATION FOR 5.0x7.0mm LVPECL/LVDS SMT VCXO

### FEATURES

LVPECL/LVDS Differential Output  
 Low RMS jitter performance 12 kHz to 20 MHz  
 Low Phase Noise  
 Compliant to RoHS directive

### APPLICATIONS

Base station controllers  
 4G/LTE applications  
 Ethernet, SyncE  
 Test and Measurement

### Ordering Information:

| Product Family | Temperature Range |                  | Stability* | Enable/Disable |                     | Absolute Pull Range (APR) |         | Logic Type |                | Package/Lead Configuration |          | Frequency    |
|----------------|-------------------|------------------|------------|----------------|---------------------|---------------------------|---------|------------|----------------|----------------------------|----------|--------------|
|                | Code              | Value            | Code       | Code           | Value               | Code                      | Value   | Code       | Value          | Code                       | Value    |              |
| M3028          | 2                 | -40 °C to +85 °C | 0          | B              | Enable High (pad 2) | G                         | ±20 ppm | P          | LVPECL<br>LVDS | N                          | Leadless | XXX.XXXX MHz |
|                | 6                 | -20 °C to +70 °C |            | U              | No Enable/Disable   | C                         | ±25 ppm |            |                |                            |          |              |

Example: M302820BGPN 122.8800 MHz

|       |   |   |   |   |   |   |             |
|-------|---|---|---|---|---|---|-------------|
| M3028 | 2 | 0 | B | G | P | N | 122.8800MHz |
|-------|---|---|---|---|---|---|-------------|

\* Stability is included in the APR specification.

### LVPECL Electrical Specifications:

| Parameter                                     | Symbol                         | Min.   | Typ.  | Max.                  | Units | Conditions                     |
|---|--------------------------------|--|-------|-----------------------|-------|--------------------------------|
| Frequency of Operation                        | F <sub>O</sub>                 | 30   |       | 170                   | MHz   |                                |
| <b>Frequency Stability</b>                    |                                |  |       |                       |       |                                |
| Frequency Stability                           | ΔF/F                           | See ordering information                       |       |                       |       |                                |
| Aging   |                                | -5   |       | +5                    | ppm   | 1 <sup>st</sup> year           |
|   |                                | -3   |       | +3                    |       | Per year thereafter            |
| <b>RF Output</b>                              |                                |  |       |                       |       |                                |
| Output Type                                   |                                | LVPECL Compatible                              |       |                       |       |                                |
| Output Load                                   |                                | 50 Ω to (V <sub>CC</sub> -2.0) V <sub>DC</sub> |       |                       | V     |                                |
| Symmetry (duty cycle)                         |                                | 45   |       | 55                    | %     | Ref. to 50% of waveform        |
| Logic Level "0"                               | V <sub>OL</sub>                |  |       | V <sub>CC</sub> -1.63 | V     |                                |
| Logic Level "1"                               | V <sub>OH</sub>                | V <sub>CC</sub> -1.085                         |       |                       | V     |                                |
| Rise/Fall Time                                | T <sub>R</sub> /T <sub>F</sub> |  |       | 0.7                   | ns    | 20% to 80% of waveform         |
| Start-up Time                                 | T <sub>SU</sub>                |  |       | 10                    | ms    | T <sub>ambient</sub> = +25°C   |
| Enable Logic (Pad 2)                          |                                | 70% V <sub>CC</sub> or<br>N/C                  |       |                       | V     | Output Enabled                 |
| Disable Logic (Pad 2)                         |                                |  |       | 30% V <sub>CC</sub>   | V     | Output Disabled to high-Z      |
| <b>Frequency Adjustment</b>                   |                                |  |       |                       |       |                                |
| Control Voltage                               |                                | 0.00   | 1.65  | 3.30                  | V     | Pad 1                          |
| Absolute Pull Range                           | APR                            | See ordering information                       |       |                       |       |                                |
| Modulation Bandwidth                          | f <sub>m</sub>                 | 10   | 20    |                       | kHz   | -3 dB                          |
| Input Impedance                               | Z <sub>in</sub>                | 100  |       |                       | kΩ    | Pad 1                          |
| Linearity                                     |                                |  |       | 10                    | %     |                                |
| <b>Supply Voltage &amp; Power Consumption</b> |                                |  |       |                       |       |                                |
| Operating Voltage                             | V <sub>CC</sub>                | 3.135  | 3.300 | 3.465                 | V     |                                |
| Supply Current                                | I <sub>CC</sub>                |  |       | 80                    | mA    |                                |
| <b>Other Parameters</b>                       |                                |  |       |                       |       |                                |
| Phase Jitter (RMS)                            | Φ <sub>J</sub>                 |  | 0.1   |                       | ps    | 12 KHz to 20 MHz<br>122.88 MHz |



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### LVDS Electrical Specifications:

| Parameter                                     | Symbol                         | Min.                       | Typ.  | Max.                | Units | Conditions                               |  |
|---|--------------------------------|----------------------------|-------|---------------------|-------|--|--|
| Frequency of Operation                        | F <sub>O</sub>                 | 30                         |       | 170                 | MHz   |  |  |
| <b>Frequency Stability</b>                    |                                |                            |       |                     |       |  |  |
| Frequency Stability                           | ΔF/F                           | See ordering information   |       |                     |       |  |  |
| Aging   |                                | -5                         |       | +5                  | ppm   | 1 <sup>st</sup> year                     |  |
|   |                                | -3                         |       | +3                  |       | Per year thereafter                      |  |
| <b>RF Output</b>                              |                                |                            |       |                     |       |  |  |
| Output Type                                   |                                | LVDS Compatible            |       |                     |       |  |  |
| Output Load                                   |                                | 100 Ω Differential         |       |                     | V     |  |  |
| Symmetry (duty cycle)                         | V <sub>OH</sub>                | 45                         |       | 55                  | %     | Ref. to 50% of waveform                  |  |
| Differential Output Voltage                   | V <sub>DIFF</sub>              | 250                        | 350   | 450                 | mV    | peak-to-peak differential output voltage |  |
| Output Offset Voltage                         | V <sub>OS</sub>                | 1.125                      | 1.250 | 1.375               | V     |  |  |
| Rise/Fall Time                                | T <sub>R</sub> /T <sub>F</sub> |                            | 0.4   | 0.7                 | ns    | 20% to 80% of waveform                   |  |
| Start-up Time                                 | T <sub>SU</sub>                |                            |       | 10                  | ms    | T <sub>ambient</sub> = +25°C             |  |
| Enable Logic (Pad 2)                          |                                | 70% V <sub>CC</sub> or N/C |       |                     | V     | Output Enabled                           |  |
| Disable Logic (Pad 2)                         |                                |                            |       | 30% V <sub>CC</sub> | V     | Output Disabled to high-Z                |  |
| <b>Frequency Adjustment</b>                   |                                |                            |       |                     |       |  |  |
| Control Voltage                               |                                | 0.30                       | 1.65  | 3.00                | V     | Pad 1                                    |  |
| Absolute Pull Range                           | APR                            | See ordering information   |       |                     |       |  |  |
| Modulation Bandwidth                          | f <sub>m</sub>                 | 10                         |       |                     | kHz   | -3 dB                                    |  |
| Input Impedance                               | Z <sub>in</sub>                | 100                        |       |                     | kΩ    | Pad 1                                    |  |
| Linearity                                     |                                |                            |       | 10                  | %     |  |  |
| <b>Supply Voltage &amp; Power Consumption</b> |                                |                            |       |                     |       |  |  |
| Operating Voltage                             | V <sub>CC</sub>                | 3.135                      | 3.300 | 3.465               | V     |  |  |
| Supply Current                                | I <sub>CC</sub>                |                            |       | 60                  | mA    |  |  |
| <b>Other Parameters</b>                       |                                |                            |       |                     |       |  |  |
| Phase Jitter (RMS)                            | Φ <sub>J</sub>                 |                            | 0.2   |                     | ps    | 12 KHz to 20 MHz<br>156.25 MHz           |  |

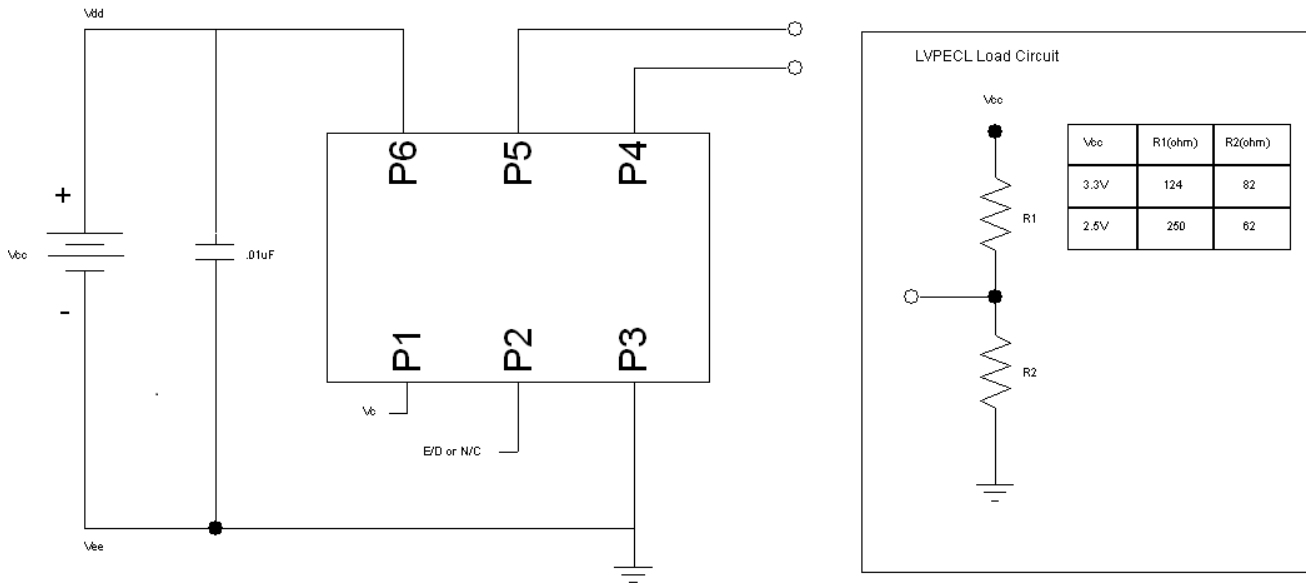
### Environmental & Packaging Requirements:

|                            |   |
|----------------------------|---|
| Storage Temperature        | -55°C to 125°C  |
| Mechanical Shock           | Per MIL-STD-202, Method 213, Condition E                              |
| Vibration                  | Per MIL-STD-202, Method 204D, Condition D                             |
| Aging                      | +85°C ±3°C, 720H (No BIAS)  |
| Humidity                   | +40°C ±2°C X90~95%, 96H (NO BIAS)                                     |
| Thermal Cycle              | Per MIL-STD-883, Method 1011, Condition A                             |
| Hermeticity                | Per MIL-STD-202, Method 112 (1 x 10 <sup>-8</sup> atm cc/s of Helium) |
| Moisture Sensitivity Level | MSL1  |
| Solderability              | Per EIAJ-STD-002, Method 208  |
| Max. Soldering Conditions  | See solder profile, Figure 1  |
| Pad Termination            | Gold, 1 μm maximum thickness  |
| Package Type               | 6-pad 5.0 X 7.0 mm leadless ceramic. RoHS compliant.                  |

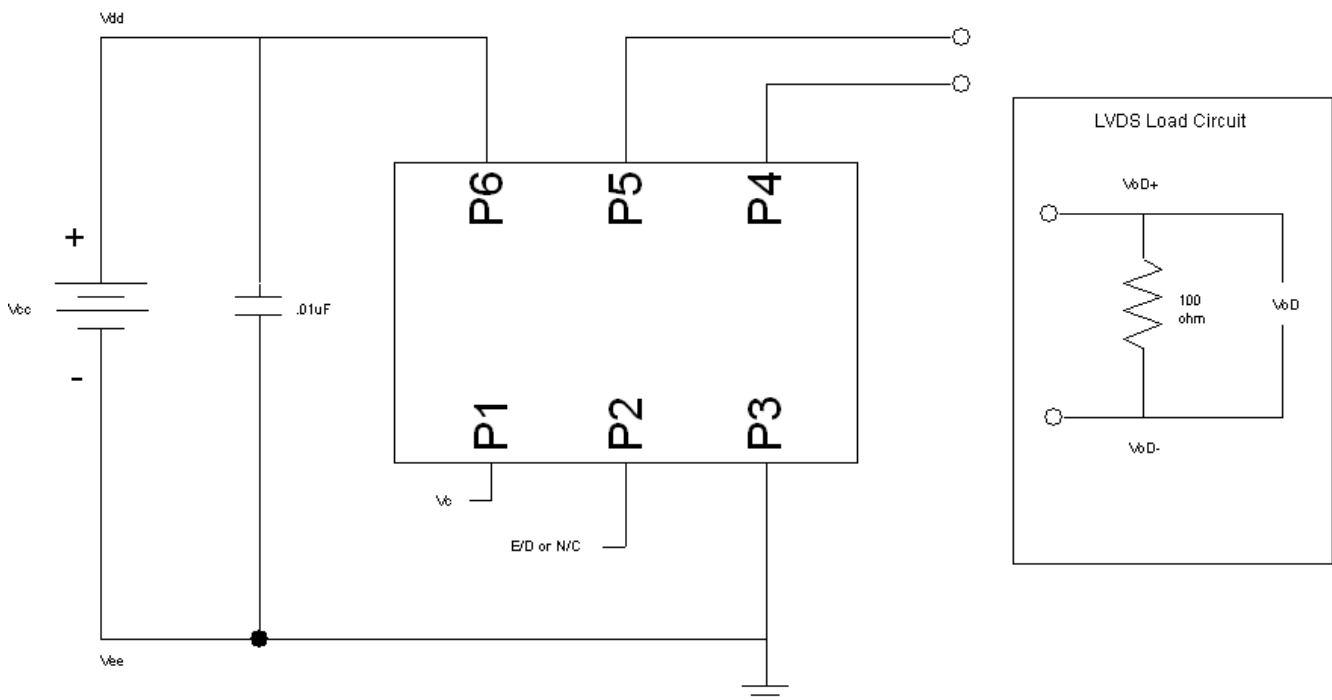


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**Typical LVPECL Test Circuit & Load Circuit Diagrams:**



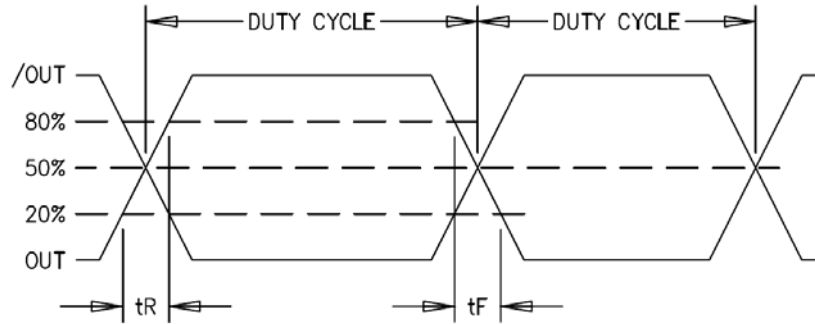
**Typical LVDS Test Circuit & Load Circuit Diagrams:**



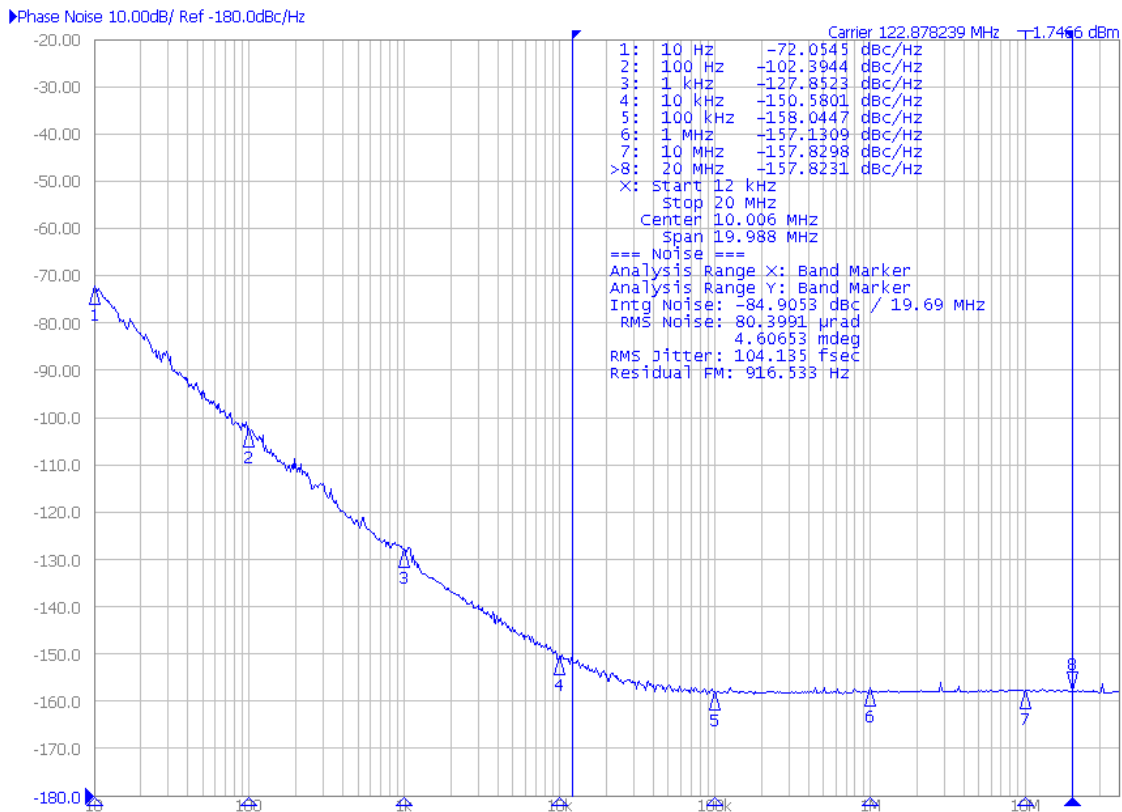


## M3028 Series SPECIFICATION FOR 5.0x7.0mm LVPECL/LVDS SMT VCXO

### Output Waveform:



### LVPECL Phase Noise Plot:





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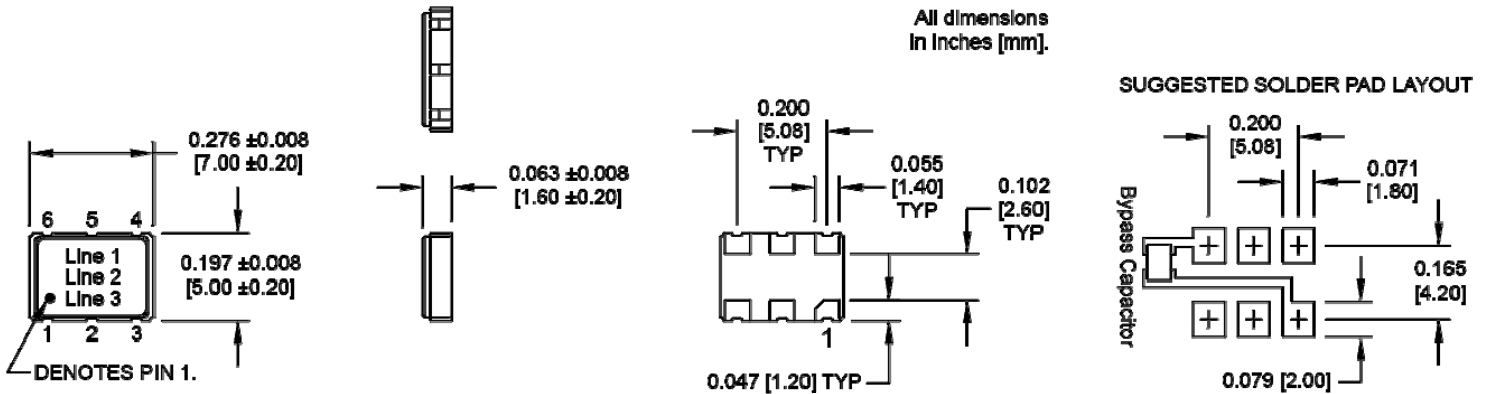
### Marking, Pin Out:

| Pad | Function              |
|-----|-----------------------|
| 1   | Control Voltage       |
| 2   | Enable/Disable or N/C |
| 3   | Ground                |
| 4   | Output                |
| 5   | Complementary Output  |
| 6   | +V <sub>CC</sub>      |

| Part Marking |                    |
|--------------|--------------------|
| Line 1       | [part designation] |
| Line 2       | FFFFFFFFFF         |
| Line 3       | M yy ww vv         |

| Legend |              |
|--------|--------------|
| M      | MtronPTI     |
| F      | Frequency    |
| yy     | Year         |
| ww     | Work Week    |
| vv     | Factory code |

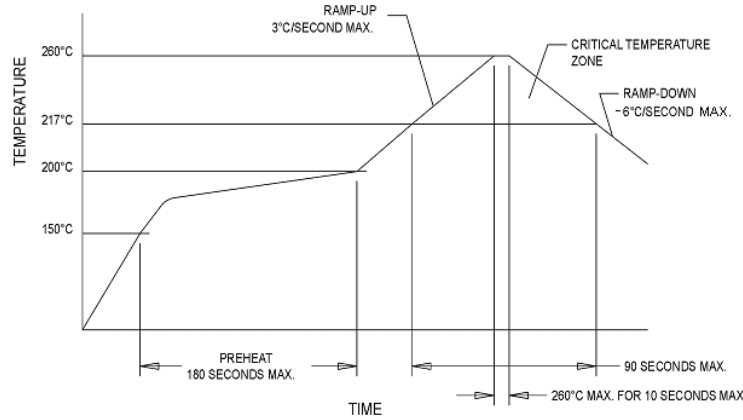
### Dimensions:





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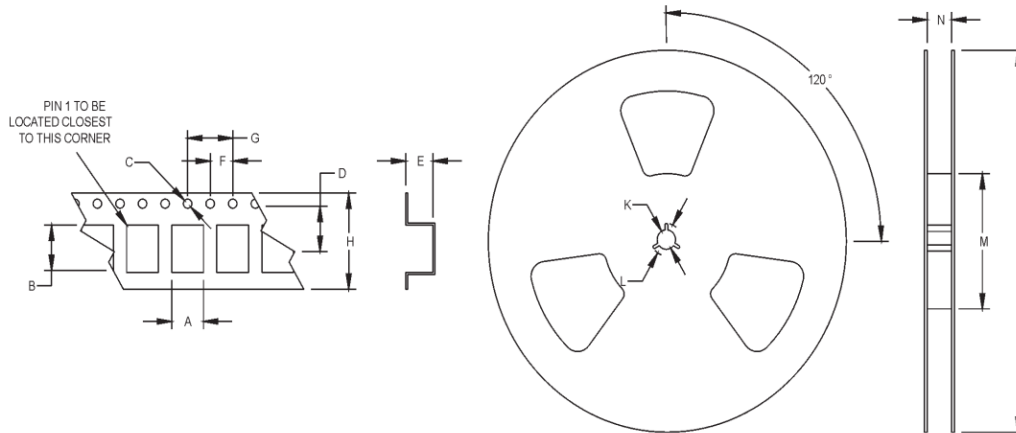
### Soldering Conditions:



**Figure 1**

### Tape and Reel Specifications:

All units in mm



| Tape and Reel Specifications |      |     |     |     |   |   |    |     |      |      |    |
|------------------------------|------|-----|-----|-----|---|---|----|-----|------|------|----|
| A                            | B    | C   | D   | E   | F | G | H  | J   | K    | L    | M  |
| 5.32                         | 7.28 | 1.5 | 7.5 | 2.2 | 4 | 8 | 16 | 178 | 13.5 | 24.8 | 80 |