



PRELIMINARY

M30240

M30240 Group Specification

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**MITSUBISHI ELECTRONICS
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Features

1.0 Description

The M30240 group is a 16-bit microcomputer based on the M16C family core technology. They are single-chip USB peripheral microcontrollers based on the Universal Serial Bus (USB) Version 1.1 specification. They are packaged in an 80-pin, molded plastic QFP. These single-chip microcontrollers operate using sophisticated instructions featuring a high level of instruction efficiency, making them capable of executing instructions at high speed. They also feature a built-in multiplier and DMAC, making them ideal for controlling office communications, industrial equipment, and other high-speed processing applications.

1.1 Features

- CPU 16-bit (including a hardware multiplier)
- Number of instructions 91
- Shortest instruction execution time 83ns $f(X_{IN})=12\text{MHz}$
- USB Features:..... Five endpoint pairs (IN/OUT)
 FIFO Sizes (endpoints 0-4):32,128, 32, 32, 32
 Conforms to USB V1.1 Specification
- USB Transceiver Conforms to USB V1.1 Specification-Internal Vref
- Frequency Synthesizer..... PLL for 48MHz clock
- Memory capacity (mask device):..... ROM (40K, 48K) / RAM (3.0 K)
- Memory capacity (OTP device):..... PROM (128K) / RAM (5K)
- Supply Voltage 4.1 to 5.25V $f(X_{IN})=12\text{MHz}$
- Interrupts 21 internal and 4 external interrupt sources,
 4 software interrupt sources; 7 levels (including key input interrupt X 16)
- Multifunction timer 5 X 16-bit, w/integrated 20mA (peak) PWM outputs
- General purpose timer 3 X 16-bit, internal interrupt only
- UART..... 3 X 7/8/9 bits;
 Configurable for synchronous or asynchronous mode
- DMAC..... 2 channels (trigger: 18 sources)
- A-D Converter 10 bits X 8 channels
- CRC calculation circuit..... 1 circuit (industry standard polynomial)
- Watchdog timer 1 line (15 bit)
- Programmable I/O 63 lines
- High current and LED Drivers 5 high current and 8 LED drivers
- Clock-generating circuit..... 1 built-in circuit including feedback resistor
- Package: 80P6N (0.8 mm pitch)

1.2 Applications

USB peripherals, such as telephones, audio systems, scanners, and digital cameras.

Pin Configuration

1.3 Pin Configuration

Figure 1.1 shows the pin configuration (top view).

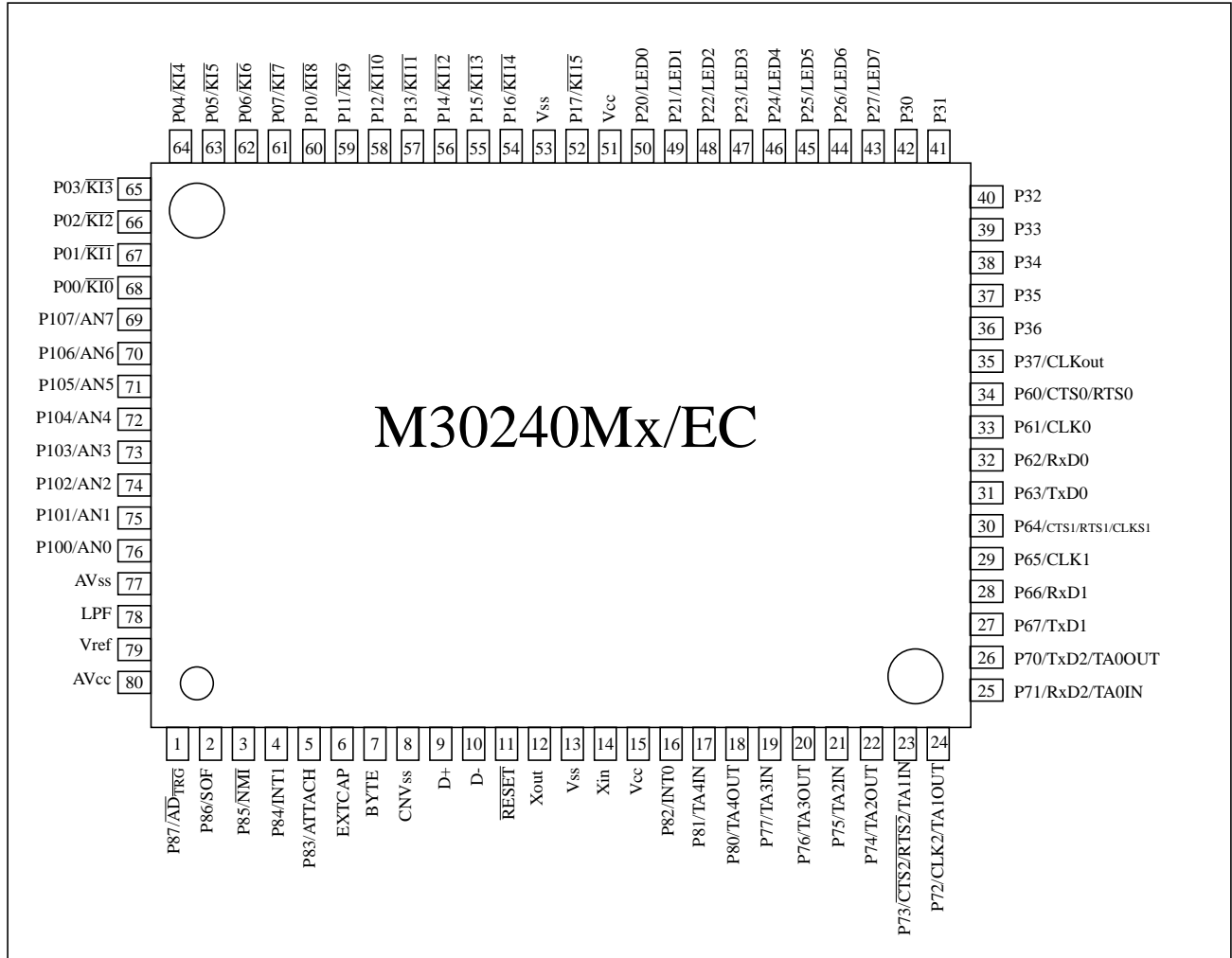


Figure 1.1: Pin Configuration (top view)

Block Diagram

1.4 Block Diagram

Figure 1.2 is a block diagram of the M30240 group.

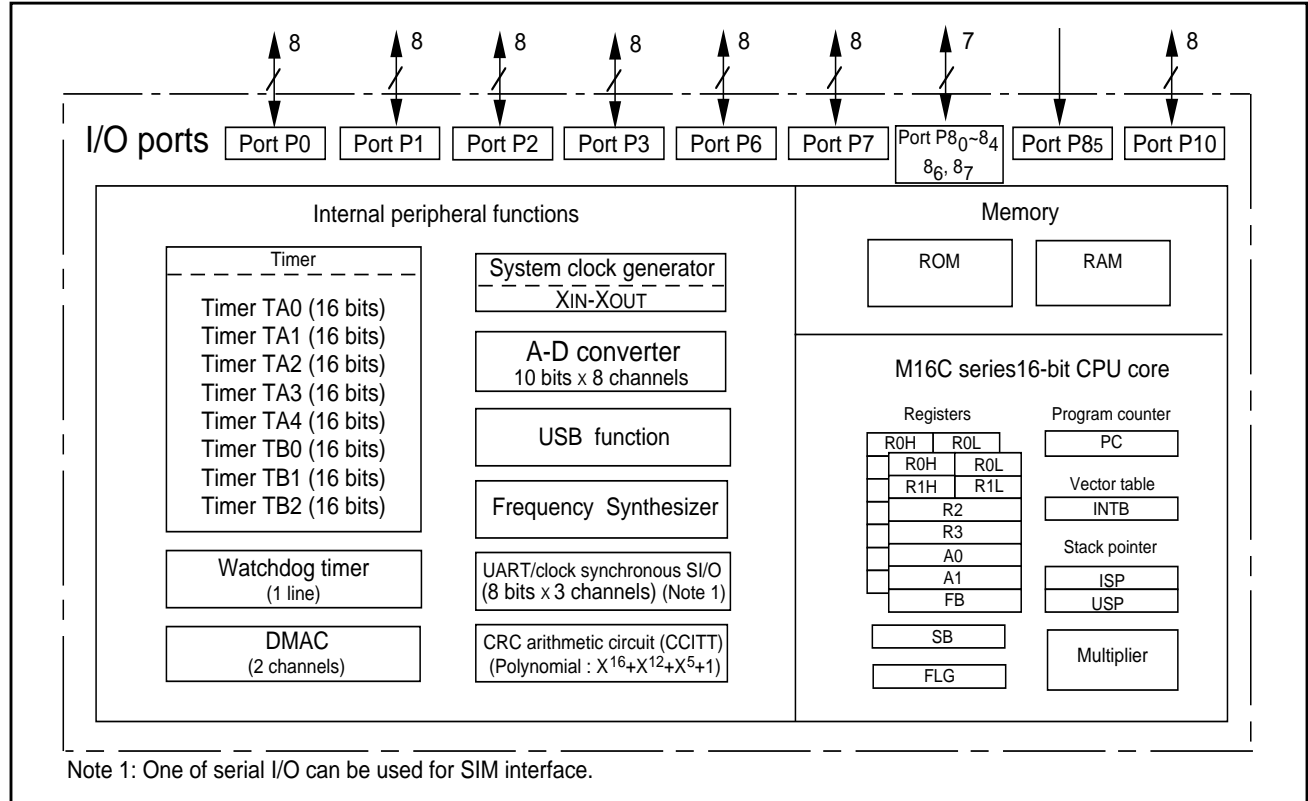


Figure 1.2: Block diagram of M30240 group



Performance outline

1.5 Performance outline

Table 1.1 is a performance outline of the M30240 group.

Table 1.1: Performance outline of M30240 group

Item		Performance
Number of basic instructions		91 instructions
Shortest instruction execution time		83ns (f(XIN) =12MHz)
Memory capacity	ROM	(See Figure 3: ROM capacity field)
	RAM	
I/O port	P0 to P3, P6,P7, P8 (except P85), P10	8 bits x 7, 7 bits x 1
Input port	P85	1 bit x 1
Multifunction Timer	TA0, TA1, TA2, TA3, TA4	16 bits x 5
General purpose Timer	TB0, TB1, TB2	16 bits x 3
Serial I/O	UART0, UART1, UART2	(UART or clock synchronous) x 3
A-D converter		10 bits x 8 channels
DMAC		2 channels (trigger:18 sources)
CRC calculation circuit		CRC-CCITT
Watchdog timer		15 bits x 1 (with prescaler)
Interrupt		21 internal and 4 external sources, 4 software sources, 7 levels
Clock-generating circuit		Built-in clock generation circuit (built-in feedback resistor, and external ceramic or quartz oscillator)
Supply voltage (typical)		4.1 to 5.25V, (f(XIN)=12MHz, without software wait)
Power consumption (typical)		250 mwatt, Vcc=5.0V, 12MHz
I/O characteristics	I/O withstand voltage	5V
	Average output current	5 mA available on ports P0, P1, P3,P6, P7 ₁ , P7 ₃ , P7 ₅ , P7 ₇ , P8 ₁ ~P8 ₄ , P8 ₆ , P8 ₇ , P10 10 mA available on ports P2, P7 ₀ , P7 ₂ , P7 ₄ , P7 ₆ , P8 ₀
Operating temperature		0 to 70°C
Device configuration		CMOS high performance silicon gate
Package		80-pin plastic molded QFP



Performance outline

Mitsubishi plans to release the following products in the M30240 group:

- (1) Support for mask ROM version and one-time PROM version
- (2) ROM capacity
- (3) Package
 - 80P6N: Plastic molded QFP (mask ROM version and one-time PROM version)

Figure 1.3 shows the type number, memory size and package for the M30240 group.

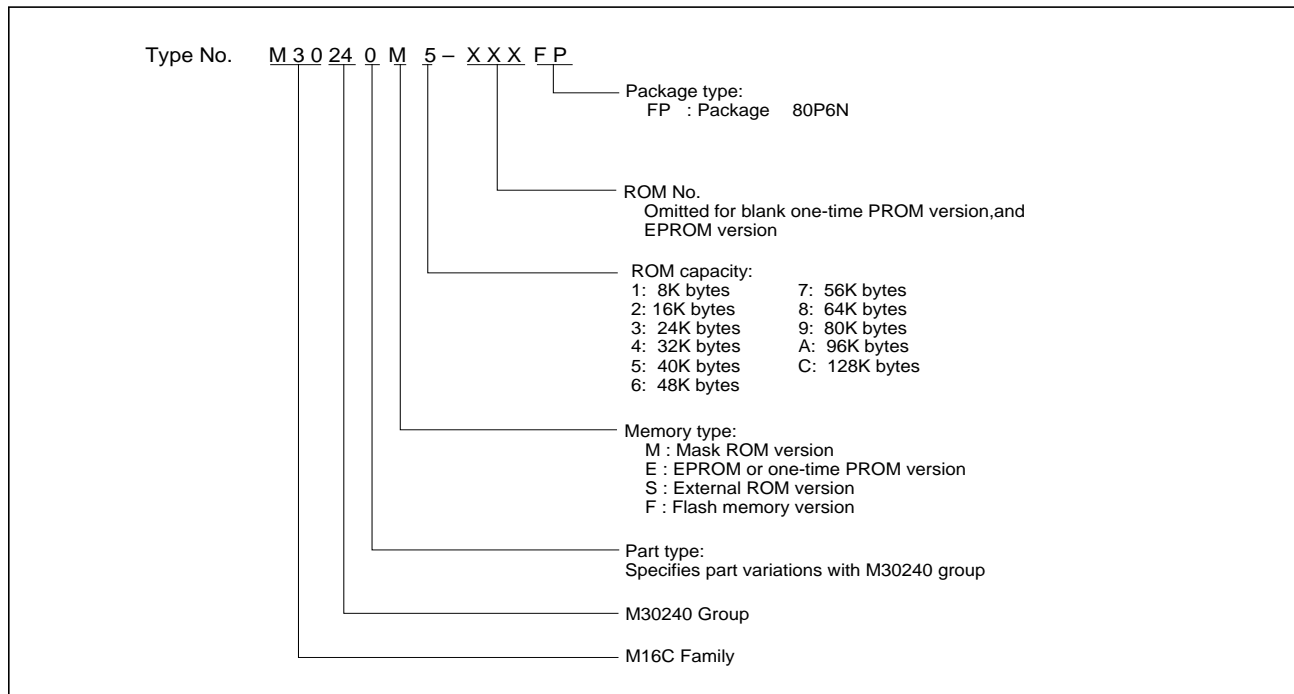


Figure 1.3: Type number, memory size, and package

Table 1.2 shows the Package Number, type, ROM and RAM Capacity for M30240 Group.

Table 1.2: M30240 Group

Type	ROM Capacity	RAM Capacity	Package Type	Remarks
M30240M5	40K bytes	3K bytes	80P6N	Mask ROM Version
M30240M6	48K bytes	3K bytes	80P6N	Mask ROM Version
M30240ECFP	128K bytes	5K bytes	80P6N	One-time PROM version

Pin Description

1.6 Pin Description

Table 1.3: Figure Pin Description

Pin #	Name	I/O	Description
1	P8 ₇	I/O	CMOS I/O port. This pin also functions as an external trigger for A-D conversion.
2	P8 ₆	I/O	CMOS I/O port. This pin also functions as the start of frame (SOF) pulse for the USB module.
3	P8 ₅ / $\overline{\text{NMI}}$	I	CMOS input port. This pin also functions as a non-maskable external interrupt.
4,5	P8 ₄ ~ P8 ₃	I/O	CMOS I/O port. These pins also functions as external interrupt 1 and are used to enable the stealth detach function for the USB transceiver.
6	EXTCAP	–	An external capacitor (Ext. Cap) pin. When the USB transceiver voltage converter is used, a 2.2 μF and a 0.1 μF capacitor should connect between this pin and V_{SS} to ensure proper operation of the USB line driver. This option is enabled by setting bit 4 of the USB control register (000C ₁₆) to a "1".
7	BYTE	I	Connect this pin to V_{SS}
8	CNV _{SS}	I	Connect this pin to V_{SS}
9	USB D ⁺	I/O	USB D+ voltage line interface, a series resistor of 33 Ω is connected to this pin.
10	USB D ⁻	I/O	USB D- voltage line interface, a series resistor of 33 Ω is connected to this pin.
11	$\overline{\text{RESET}}$	I	A "L" on this input resets the microcomputer.
12	Xout	O	See Xin
13	V_{SS}	I	Ground: $V_{\text{SS}} = 0\text{V}$
14	Xin	I	Input and output signals to and from the internal clock generation circuit. Connect a ceramic resonator or quartz crystal between Xin and Xout pins to set the oscillation frequency. If an external clock is used, connect the clock source to the Xin pin and leave the Xout pin open.
15	V_{CC}	I	Power: $V_{\text{CC}} = 4.1 \sim 5.25\text{V}$
16	P8 ₂	I/O	CMOS I/O port. This pin also functions as external interrupt 0.
17-18	P8 ₁ ~ P8 ₀	I/O	CMOS I/O port. Pins in this port also function as TimerA4 input and output as selected by software.
19-22	P7 ₇ ~ P7 ₄	I/O	CMOS I/O port. Pins in this port also function as timer pins. P7 ₇ and P7 ₆ can function as TimerA3 input and output as selected by software. P7 ₅ and P7 ₄ can function as TimerA2 input and output as selected by software.
23-26	P7 ₃ ~ P7 ₀	I/O	CMOS I/O port. Pins in this port also function as UART2 CTS, RTS, CLK, RXD, and TXD as selected by software. P7 ₃ and P7 ₂ can function as TimerA1 input and output as selected by software. P7 ₁ and P7 ₀ can function as TimerA0 input and output as selected by software.
27-30	P6 ₇ ~ P6 ₄	I/O	CMOS I/O port. Pins in this port also function as UART1 CTS, RTS, CLK, Serial Clock, RXD, and TXD as selected by software. TXD(OE \sim) and RTS(SUSPEND) in addition to D+ and D- can be used to run the device in USB bypass mode.
31-34	P6 ₃ ~ P6 ₀	I/O	CMOS I/O port. Pins in this port also function as UART0 CTS, RTS, CLK, RXD, and TXD as selected by software.
35-42	P3 ₇ ~ P3 ₀	I/O	CMOS I/O port.
43-50	P2 ₇ /LED7 ~ P2 ₀ /LED0	I/O	CMOS I/O port. These pins are capable of driving up to 20mA (peak) for LEDs.



Pin Description

Table 1.3: Figure Pin Description

Pin #	Name	I/O	Description
51	V _{CC}	I	Power: V _{CC} = 4.1~ 5.25V
52	P1 ₇ /K1 ₁₅	I/O	CMOS I/O port. This port can also function as the key-on wakeup interrupt K1 ₁₅ .
53	V _{SS}	I	Ground: V _{SS} = 0V
54-60	P1 ₆ /K1 ₁₄ ~ P1 ₀ /K1 ₈	I/O	CMOS I/O port. This port can also function as the key-on wakeup interrupts (K1 ₈ ~ K1 ₁₄).
61-68	P0 ₇ /K1 ₇ ~ P0 ₀ /K1 ₀	I/O	CMOS I/O port. This port can also function as the key-on wakeup interrupts (K1 ₀ ~ K1 ₇).
69-76	P10 ₇ ~ P10 ₀	I/O	CMOS I/O port. These pins also function as Analog inputs 7-0 for A-D conversion
77	AV _{SS}	I	This pin is a power supply input for the AD converter. (Connect to V _{SS})
78	LPF	O	Loop filter for the frequency synthesizer.
79	V _{REF}	I	This pin is the reference voltage input for the A-D converter.
80	AV _{CC}	I	This pin is a power supply input for the AD converter. (Connect to V _{CC})

Central Processing Unit (CPU)

2.0 Operation of Functional Blocks

The M30240 group accommodates certain units in a single chip. These units include ROM and RAM to store instructions and data, and the central processing unit (CPU) to execute arithmetic/logic operations. Also included are peripheral units such as USB, timers, serial I/O, DMAC, CRC calculation circuit, A-D converter, and I/O ports.

The following explains each unit.

2.1 Central Processing Unit (CPU)

The CPU has a total of 13 registers shown in Figure 1.5. Seven of these registers (R0, R1, R2, R3, A0, A1, and FB) come in two sets; therefore, these have two register banks.

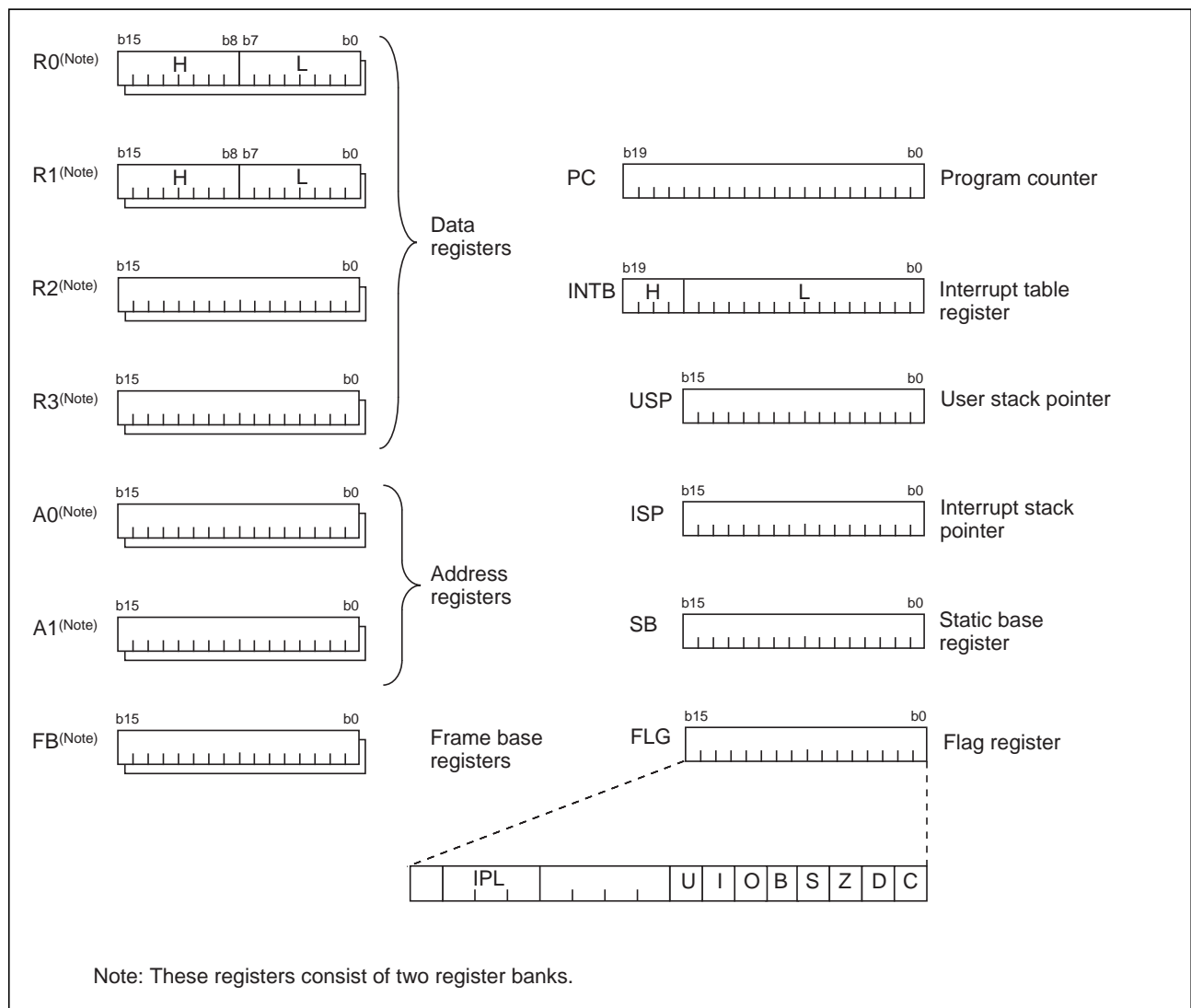


Figure 1.5: Central processing unit register

2.1.1 Data registers (R0, R0H, R0L, R1, R1H, R1L, R2, and R3)

Data registers (R0, R1, R2, and R3) are configured with 16 bits, and are used primarily for transfer and arithmetic/logic operations.



Central Processing Unit (CPU)

Registers R0 and R1 each can be used as separate 8-bit data registers, high-order bits as (R0H/R1H), and low-order bits as (R0L/R1L). In some instructions, registers R2 and R0, as well as R3 and R1, can be used as 32-bit data registers (R2R0/R3R1).

2.1.2 Address registers (A0 and A1)

Address registers (A0 and A1) are configured with 16 bits, and have functions equivalent to those of data registers. These registers can also be used for address register indirect addressing and address register relative addressing.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.1.3 Frame base register (FB)

Frame base register (FB) is configured with 16 bits, and is used for FB relative addressing.

2.1.4 Program counter (PC)

Program counter (PC) is configured with 20 bits, indicating the address of an instruction to be executed.

2.1.5 Interrupt table register (INTB)

Interrupt table register (INTB) is configured with 20 bits, indicating the start address of an interrupt vector table. INTB can be used as separate registers of four high-order bits and 16 low-order bits.

2.1.6 Stack pointer (USP/ISP)

Stack pointer comes in two types: user stack pointer (USP) and interrupt stack pointer (ISP), each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by a stack pointer select flag (U flag). This flag is located at the position of bit 7 in the flag register (FLG).

2.1.7 Static base register (SB)

Static base register (SB) is configured with 16 bits, and is used for SB relative addressing.

2.1.8 Flag register (FLG)

Flag register (FLG) is configured with 11 bits, each bit is used as a flag. Figure 1.6 shows the flag register (FLG). The following explains the function of each flag:

2.1.8.1 Bit 0: Carry flag (C flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.1.8.2 Bit 1: Debug flag (D flag)

This flag enables a single-step interrupt.

When this flag is "1", a single-step interrupt is generated after instruction execution. This flag is cleared to "0" when the interrupt is acknowledged.

2.1.8.3 Bit 2: Zero flag (Z flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, cleared to "0".

2.1.8.4 Bit 3: Sign flag (S flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, cleared to "0".

2.1.8.5 Bit 4: Register bank select flag (B flag)

This flag chooses a register bank. Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

2.1.8.6 Bit 5: Overflow flag (O flag)

This flag is set to "1" when an arithmetic operation resulted in overflow; otherwise, cleared to "0".

Central Processing Unit (CPU)

2.1.8.7 Bit 6: Interrupt enable flag (I flag)

This flag enables a maskable interrupt.

An interrupt is disabled when this flag is “0”, and is enabled when this flag is “1”. This flag is cleared to “0” when the interrupt is acknowledged.

2.1.8.8 Bit 7: Stack pointer select flag (U flag)

Interrupt stack pointer (ISP) is selected when this flag is “0”; user stack pointer (USP) is selected when this flag is “1”.

This flag is cleared to “0” when a hardware interrupt is acknowledged or an INT instruction of software interrupts 0 to 31 is executed.

2.1.8.9 Bits 8 to 11: Reserved area

2.1.8.10 Bits 12 to 14: Processor interrupt priority level (IPL)

Processor interrupt priority level (IPL) is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than the processor interrupt priority level (IPL), the interrupt is enabled.

2.1.8.11 Bit 15: Reserved area

The C, Z, S, and O flags are changed when instructions are executed. See the M16C software manual for details.

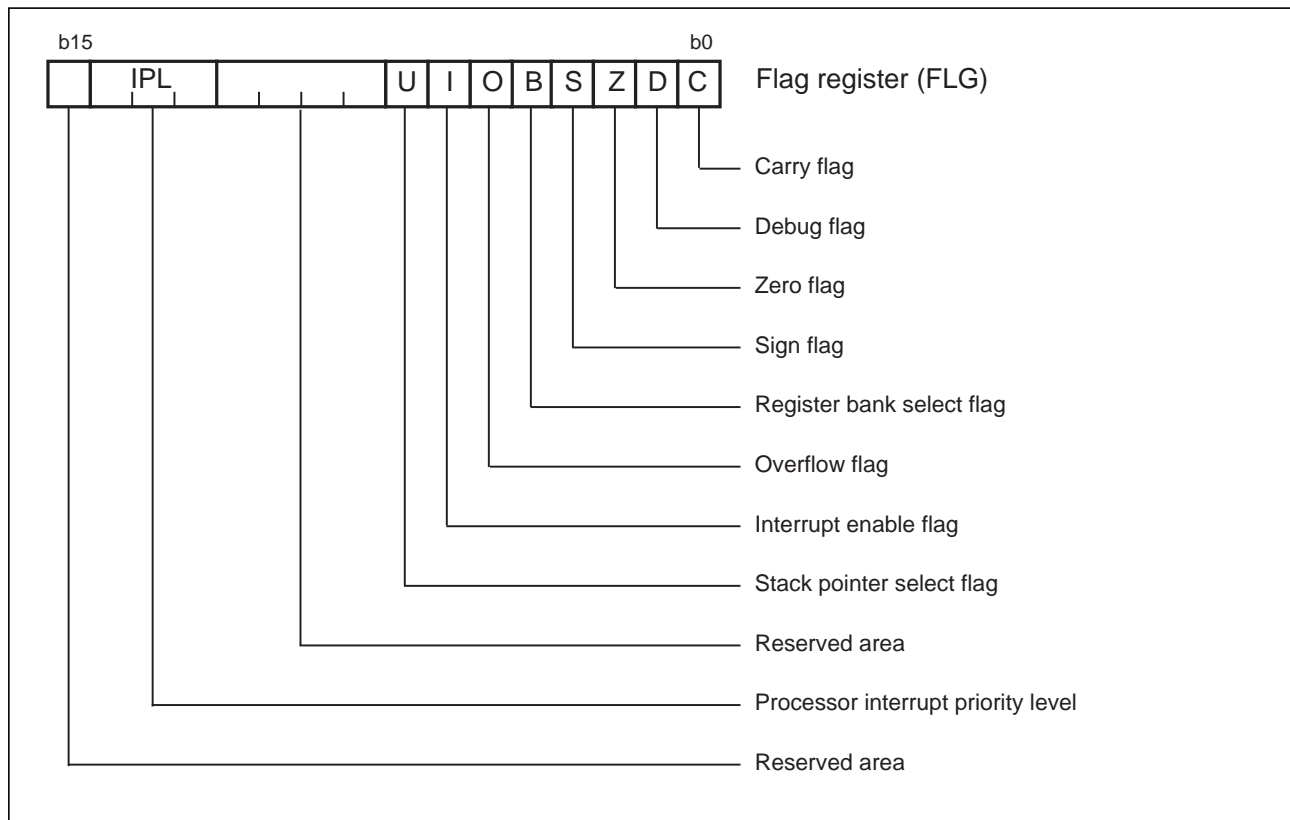


Figure 1.6: Flag register (FLG)

Processor Mode

2.2 Processor Mode

Figure 1.7 shows the processor mode registers 0 and 1.

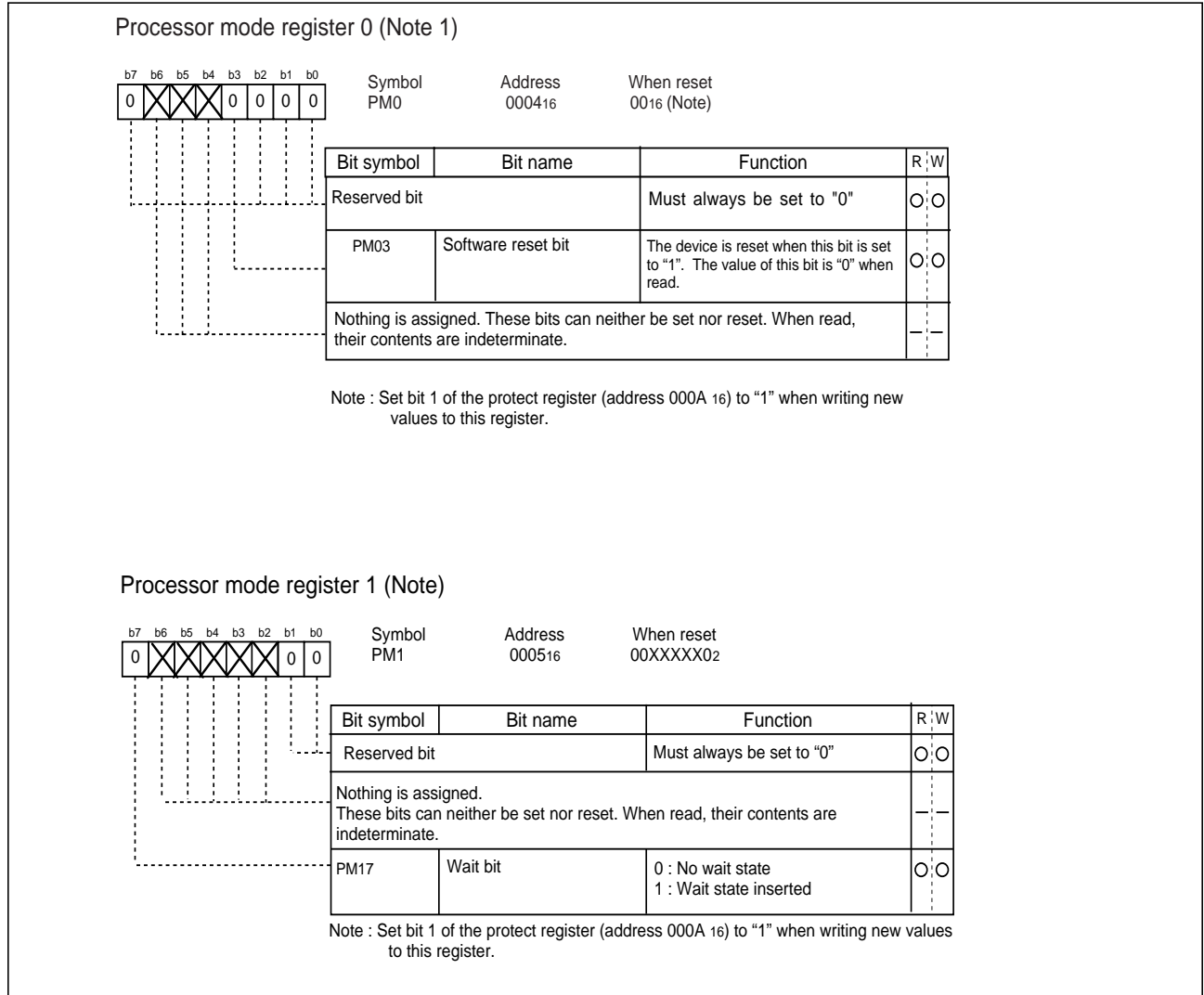


Figure 1.7: Processor mode registers 0 and 1

Memory

2.3 Memory

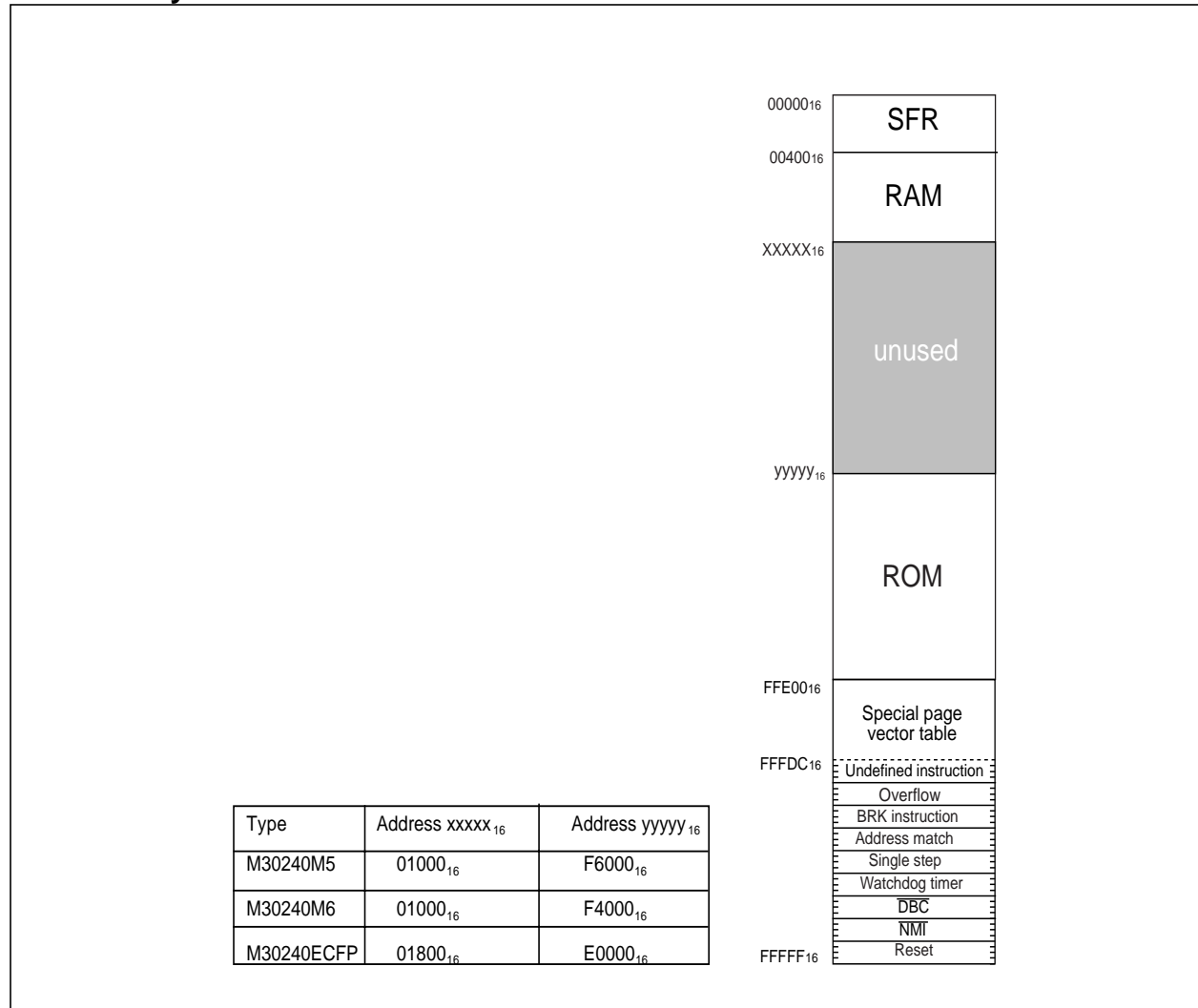


Figure 1.8: Memory Map

Figure 1.8 is a memory map of the M30240 group. The address space extends the 1M bytes from address 00000₁₆ to FFFFF₁₆. Addresses above yyyyy₁₆ are ROM. For example, in the M30240ECFP, there is 128K bytes of internal ROM from E0000₁₆ to FFFFF₁₆. The special page vector table is mapped from FFE00₁₆ to FFFDB₁₆. If the starting addresses of subroutines or the destination addresses of jumps are stored here, subroutine call instructions and jump instructions can be used as two-byte instructions, reducing the number of program steps.

The vector table for fixed interrupts such as the reset and $\overline{\text{NMI}}$ are mapped from FFFDC₁₆ to FFFFF₁₆. The starting addresses of the interrupt routines are stored here. The address of the vector table for software interrupts can be set as desired using the internal register (INTB). See Section 2.12 on interrupts for further details.

Addresses below xxxxx₁₆ are RAM. For example, in M30240ECFP, 5K bytes of internal RAM are mapped to the space from 00400₁₆ to 017FF₁₆. In addition to storing data, the RAM also stores the stack used when calling subroutines and when interrupts are generated. The SFR area is mapped to 00000₁₆ to 003FF₁₆. This area accommodates control registers for peripheral devices such as I/O ports, A-D converter, serial I/O, and timers. Section 2.4 describes the SFR area for peripheral unit control registers. Any part of the SFR area that is unoccupied is reserved and cannot be used for other purposes.

SFR MAP

2.4 SFR MAP

The table below shows the peripheral control registers, their addresses, names, acronyms, and values after reset.

Address	Register name	Acronym	Value after reset
0000 ₁₆			
0001 ₁₆			
0002 ₁₆			
0003 ₁₆			
0004 ₁₆	Processor mode register 0	PM0	00 ₁₆
0005 ₁₆	Processor mode register 1	PM1	0 0 0
0006 ₁₆	System clock control register 0	CM0	48 ₁₆
0007 ₁₆	System clock control register 1	CM1	20 ₁₆
0008 ₁₆			
0009 ₁₆	Address match interrupt enable register	AIER	 0 0
000A ₁₆	Protect register	PRCR	 0 0 0
000B ₁₆			
000C ₁₆	USB control register	USBC	00 ₁₆
000D ₁₆			
000E ₁₆	Watchdog timer start register	WDTS	
000F ₁₆	Watchdog timer control register	WDC	0 0 0 0 ? ? ? ?
0010 ₁₆			
0011 ₁₆	Address match interrupt register 0	RMAD0	00 ₁₆
0012 ₁₆			 0 0 0 0
0013 ₁₆			
0014 ₁₆			
0015 ₁₆	Address match interrupt register 1	RMAD1	00 ₁₆
0016 ₁₆			 0 0 0 0
0017 ₁₆			
0018 ₁₆			
0019 ₁₆			
001A ₁₆			
001B ₁₆			
001C ₁₆			
001D ₁₆			
001E ₁₆	Reserved		
001F ₁₆	USB attach / detach register	USBAD	00 ₁₆
0020 ₁₆			
0021 ₁₆	DMA0 source pointer	SAR0	
0022 ₁₆			
0023 ₁₆			
0024 ₁₆			
0025 ₁₆	DMA0 destination pointer	DAR0	
0026 ₁₆			
0027 ₁₆			
0028 ₁₆			
0029 ₁₆	DMA0 transfer counter	TCR0	
002A ₁₆			
002B ₁₆			
002C ₁₆	DMA0 control register	DM0CON	0 0 0 0 0 0 ? 0 0
002D ₁₆			
002E ₁₆			
002F ₁₆			
0030 ₁₆			
0031 ₁₆	DMA1 source pointer	SAR1	
0032 ₁₆			
0033 ₁₆			
0034 ₁₆			
0035 ₁₆	DMA1 destination pointer	DAR1	
0036 ₁₆			
0037 ₁₆			
0038 ₁₆			
0039 ₁₆	DMA1 transfer counter	TCR1	
003A ₁₆			
003B ₁₆			
003C ₁₆	DMA1 control register	DM1CON	0 0 0 0 0 0 ? 0 0
003D ₁₆			
003E ₁₆			
003F ₁₆			



SFR MAP

Address	Register name	Acronym	Value after reset
0040 ₁₆			
0041 ₁₆			
0042 ₁₆			
0043 ₁₆			
0044 ₁₆	Suspend interrupt control register	SUSPIC	? 0 0 0
0045 ₁₆			
0046 ₁₆	Resume interrupt control register	RSMIC	? 0 0 0
0047 ₁₆	USB SOF interrupt control register	SOFIC	0 0 ? 0 0 0
0048 ₁₆			
0049 ₁₆			
004A ₁₆	Bus collision detection interrupt control register	BCNIC	? 0 0 0
004B ₁₆	DMA0 interrupt control register	DM0IC	? 0 0 0
004C ₁₆	DMA1 interrupt control register	DM1IC	? 0 0 0
004D ₁₆	Key input interrupt control register	KUPIC	? 0 0 0
004E ₁₆	A-D conversion interrupt control register	ADIC	? 0 0 0
004F ₁₆	UART2 transmit interrupt control register	S2TIC	? 0 0 0
0050 ₁₆	UART2 receive interrupt control register	S2RIC	? 0 0 0
0051 ₁₆	UART0 transmit interrupt control register	S0TIC	? 0 0 0
0052 ₁₆	UART0 receive interrupt control register	S0RIC	? 0 0 0
0053 ₁₆	UART1 transmit interrupt control register	S1TIC	? 0 0 0
0054 ₁₆	UART1 receive interrupt control register	S1RIC	? 0 0 0
0055 ₁₆	TIMER A0 interrupt control register	TA0IC	? 0 0 0
0056 ₁₆	TIMER A1 interrupt control register	TA1IC	? 0 0 0
0057 ₁₆	TIMER A2 interrupt control register	TA2IC	? 0 0 0
0058 ₁₆	TIMER A3 interrupt control register	TA3IC	? 0 0 0
0059 ₁₆	TIMER A4 interrupt control register	TA4IC	? 0 0 0
005A ₁₆	TIMER B0 interrupt control register	TB0IC	? 0 0 0
005B ₁₆	TIMER B1 interrupt control register	TB1IC	? 0 0 0
005C ₁₆	Reset interrupt control register	RSTIC	? 0 0 0
005D ₁₆	INT0 interrupt control register	INT0IC	0 0 ? 0 0 0
005E ₁₆	INT1 interrupt control register	INT1IC	0 0 ? 0 0 0
005F ₁₆	USB function interrupt control register	USBFIC	? 0 0 0

0300 ₁₆	USB address register	USBA	00 ₁₆
0301 ₁₆	USB power management register	USBPM	00 ₁₆
0302 ₁₆	USB interrupt status register 1	USBIS1	00 ₁₆
0303 ₁₆	USB interrupt status register 2	USBIS2	00 ₁₆
0304 ₁₆	USB interrupt enable register 1	USBIE1	FF ₁₆
0305 ₁₆	USB interrupt enable register 2	USBIE2	33 ₁₆
0306 ₁₆	USB frame number register low	USBSOFL	00 ₁₆
0307 ₁₆	USB frame number register high	USBSOFH	00 ₁₆
0308 ₁₆	USB ISO control register	USBSOC	00 ₁₆
0309 ₁₆	USB DMA0 source register	USBSAR0	00 ₁₆
030A ₁₆	USB DMA1 source register	USBSAR1	00 ₁₆
030B ₁₆	USB endpoint enable	USBEPEN	FF ₁₆
030C ₁₆			
030D ₁₆			
030E ₁₆			
030F ₁₆			
0310 ₁₆	USB reserved		
0311 ₁₆	USB EP 0 control/status register	EP0CS	00 ₁₆
0312 ₁₆	USB reserved		
0313 ₁₆	USB EP 0 max packet size register	EP0MP	08 ₁₆
0314 ₁₆	USB reserved		
0315 ₁₆	USB EP 0 OUT write count	EP0WC	00 ₁₆
0316 ₁₆	USB reserved		
0317 ₁₆	USB reserved		
0318 ₁₆	USB reserved		
0319 ₁₆	USB EP 1 IN control/status register	EP1ICS	00 ₁₆
031A ₁₆	USB EP 1 OUT control/status register	EP1OCS	00 ₁₆
031B ₁₆	USB EP 1 IN max packet size register	EP1IMP	00 ₁₆
031C ₁₆	USB EP 1 OUT max packet size register	EP1OMP	00 ₁₆
031D ₁₆	USB EP 1 OUT write count	EP1WC	00 ₁₆
031E ₁₆	USB reserved		
031F ₁₆	USB reserved		



SFR MAP

Address	Register name	Acronym	Value after reset	
0320 ₁₆	USB reserved			
0321 ₁₆	USB EP 2 IN control/status register	EP2ICS	00 ₁₆	
0322 ₁₆	USB EP 2 OUT control/status register	EP2OCS	00 ₁₆	
0323 ₁₆	USB EP 2 IN max packet size register	EP2IMP	00 ₁₆	
0324 ₁₆	USB EP 2 OUT max packet size register	EP2OMP	00 ₁₆	
0325 ₁₆	USB EP 2 OUT write count	EP2WC	00 ₁₆	
0326 ₁₆	USB reserved			
0327 ₁₆	USB reserved			
0328 ₁₆	USB reserved			
0329 ₁₆	USB EP 3 IN control/status register	EP3ICS	00 ₁₆	
032A ₁₆	USB EP 3 OUT control/status register	EP3OCS	00 ₁₆	
032B ₁₆	USB EP 3 IN max packet size register	EP3IMP	00 ₁₆	
032C ₁₆	USB EP 3 OUT max packet size register	EP3OMP	00 ₁₆	
032D ₁₆	USB EP 3 OUT write count	EP3WC	00 ₁₆	
032E ₁₆	USB reserved		00 ₁₆	
032F ₁₆	USB reserved			
0330 ₁₆	USB reserved			
0331 ₁₆	USB EP 4 IN control/status register	EP4ICS	00 ₁₆	
0332 ₁₆	USB EP 4 OUT control/status register	EP4OCS	00 ₁₆	
0333 ₁₆	USB EP 4 IN max packet size register	EP4IMP	00 ₁₆	
0334 ₁₆	USB EP 4 OUT max packet size register	EP4OMP	00 ₁₆	
0335 ₁₆	USB EP 4 OUT write count	EP4WC	00 ₁₆	
0336 ₁₆	USB reserved			
0337 ₁₆	USB reserved			
0338 ₁₆	USB EP 0 FIFO	EP0		
0339 ₁₆	USB EP 1 FIFO	EP1		
033A ₁₆	USB EP 2 FIFO	EP2		
033B ₁₆	USB EP 3 FIFO	EP3		
033C ₁₆	USB EP 4 FIFO	EP4		
033D ₁₆	reserved			
033E ₁₆	reserved			
033F ₁₆	reserved			
0340 ₁₆				
0341 ₁₆				
0342 ₁₆				
0343 ₁₆				
0344 ₁₆				
0345 ₁₆				
0346 ₁₆				
0347 ₁₆				
0348 ₁₆				
0349 ₁₆				
034A ₁₆				
034B ₁₆				
034C ₁₆				
034D ₁₆				
034E ₁₆				
034F ₁₆				
0350 ₁₆				
0351 ₁₆				
0352 ₁₆				
0353 ₁₆				
0354 ₁₆				
0355 ₁₆				
0356 ₁₆				
0357 ₁₆				
0358 ₁₆				
0359 ₁₆				
035A ₁₆				
035B ₁₆				
035C ₁₆				
035D ₁₆				
035E ₁₆				
035F ₁₆				



SFR MAP

Address	Register name	Acronym	Value after reset	
0370 ₁₆				
0371 ₁₆				
0372 ₁₆				
0373 ₁₆				
0374 ₁₆				
0375 ₁₆				
0376 ₁₆				
0377 ₁₆	Reserved			
0378 ₁₆	UART2 transmit / receive mode register	U2MR	00 ₁₆	
0379 ₁₆	UART2 bit rate generator	U2BRG		
037A ₁₆	UART2 transmit buffer register	U2TB		
037B ₁₆	UART2 transmit / receive control register 0	U2C0	08 ₁₆	
037C ₁₆	UART2 transmit / receive control register 1	U2C1	02 ₁₆	
037D ₁₆				
037E ₁₆	UART2 receive buffer register	U2RB		
037F ₁₆				
0380 ₁₆	Count start flag	TABSR	00 ₁₆	
0381 ₁₆	Reserved			
0382 ₁₆	One-shot start flag	ONSF	0 0 0 0 0 0 0	
0383 ₁₆	Trigger select register	TRGSR	00 ₁₆	
0384 ₁₆	Up-down flag	UDF	00 ₁₆	
0385 ₁₆				
0386 ₁₆	Timer A0	TA0		
0387 ₁₆				
0388 ₁₆	Timer A1	TA1		
0389 ₁₆				
038A ₁₆	Timer A2	TA2		
038B ₁₆				
038C ₁₆	Timer A3	TA3		
038D ₁₆				
038E ₁₆	Timer A4	TA4		
038F ₁₆				
0390 ₁₆	Timer B0	TB0		
0391 ₁₆				
0392 ₁₆	Timer B1	TB1		
0393 ₁₆				
0394 ₁₆	Timer B2	TB2		
0395 ₁₆				
0396 ₁₆	Timer A0 mode register	TA0MR	00 ₁₆	
0397 ₁₆	Timer A1 mode register	TA1MR	00 ₁₆	
0398 ₁₆	Timer A2 mode register	TA2MR	00 ₁₆	
0399 ₁₆	Timer A3 mode register	TA3MR	00 ₁₆	
039A ₁₆	Timer A4 mode register	TA4MR	00 ₁₆	
039B ₁₆	Timer B0 mode register	TB0MR	0 0 ? 0 0 0 0	
039C ₁₆	Timer B1 mode register	TB1MR	0 0 ? 0 0 0 0	
039D ₁₆	Timer B2 mode register	TB2MR	0 0 ? 0 0 0 0	
039E ₁₆				
039F ₁₆				
03A0 ₁₆	UART0 transmit / receive mode register	U0MR	00 ₁₆	
03A1 ₁₆	UART0 bit rate generator	U0BRG		
03A2 ₁₆	UART0 transmit buffer register	U0TB		
03A3 ₁₆				
03A4 ₁₆	UART0 transmit / receive control register 0	U0C0	08 ₁₆	
03A5 ₁₆	UART0 transmit / receive control register 1	U0C1	02 ₁₆	
03A6 ₁₆				
03A7 ₁₆	UART0 receive buffer register	U0RB		
03A8 ₁₆	UART1 transmit / receive mode register	U1MR	00 ₁₆	
03A9 ₁₆	UART1 bit rate generator	U1BRG		
03AA ₁₆	UART1 transmit buffer register	U1TB		
03AB ₁₆				
03AC ₁₆	UART1 transmit / receive control register 0	U1C0	08 ₁₆	
03AD ₁₆	UART1 transmit / receive control register 1	U1C1	02 ₁₆	
03AE ₁₆				
03AF ₁₆	UART1 receive buffer register	U1RB		



SFR MAP

Address	Register name	Acronym	Value after reset								
			0	0	0	0	0	0	0	0	
03B0 ₁₆	UART transmit / receive control register 2	UCON	0	0	0	0	0	0	0	0	
03B1 ₁₆											
03B2 ₁₆											
03B3 ₁₆											
03B4 ₁₆											
03B5 ₁₆											
03B6 ₁₆											
03B7 ₁₆											
03B8 ₁₆	DMA0 cause select register	DM0SL								00 ₁₆	
03B9 ₁₆											
03BA ₁₆	DMA1 cause select register	DM1SL								00 ₁₆	
03BB ₁₆											
03BC ₁₆											
03BD ₁₆	CRC data register	CRCD									
03BE ₁₆	CRC input register	CRCIN									
03BF ₁₆											
03C0 ₁₆	A-D register 0	AD0									
03C1 ₁₆											
03C2 ₁₆	A-D register 1	AD1									
03C3 ₁₆											
03C4 ₁₆	A-D register 2	AD2									
03C5 ₁₆											
03C6 ₁₆	A-D register 3	AD3									
03C7 ₁₆											
03C8 ₁₆	A-D register 4	AD4									
03C9 ₁₆											
03CA ₁₆	A-D register 5	AD5									
03CB ₁₆											
03CC ₁₆	A-D register 6	AD6									
03CD ₁₆											
03CE ₁₆	A-D register 7	AD7									
03CF ₁₆											
03D0 ₁₆											
03D1 ₁₆											
03D2 ₁₆											
03D3 ₁₆											
03D4 ₁₆	A-D control register 2	ADCON2								0	
03D5 ₁₆											
03D6 ₁₆	A-D control register 0	ADCON0	0	0	0	0	0	?	?	?	
03D7 ₁₆	A-D control register 1	ADCON1								00 ₁₆	
03D8 ₁₆											
03D9 ₁₆											
03DA ₁₆											
03DB ₁₆	Frequency synthesizer clock control	FSCCR								00 ₁₆	
03DC ₁₆	Frequency synthesizer control	FSC								60 ₁₆	
03DD ₁₆	Frequency synthesizer multiplier control	FSM								FF ₁₆	
03DE ₁₆	Frequency synthesizer prescaler control	FSP								FF ₁₆	
03DF ₁₆	Frequency synthesizer divider	FSD								FF ₁₆	
03E0 ₁₆	Port P0	P0									
03E1 ₁₆	Port P1	P1									
03E2 ₁₆	Port P0 direction register	PD0								00 ₁₆	
03E3 ₁₆	Port P1 direction register	PD1								00 ₁₆	
03E4 ₁₆	Port P2	P2									
03E5 ₁₆	Port P3	P3									
03E6 ₁₆	Port P2 direction register	PD2								00 ₁₆	
03E7 ₁₆	Port P3 direction register	PD3								00 ₁₆	
03E8 ₁₆											
03E9 ₁₆											
03EA ₁₆											
03EB ₁₆											
03EC ₁₆	Port P6	P6									
03ED ₁₆	Port P7	P7									
03EE ₁₆	Port P6 direction register	PD6								00 ₁₆	
03EF ₁₆	Port P7 direction register	PD7								00 ₁₆	

SFR MAP

Address	Register name	Acronym	Value after reset
03F0 ₁₆	Port P8	P8	
03F1 ₁₆			
03F2 ₁₆	Port P8 direction register	PD8	0 0 0 0 0 0
03F3 ₁₆			
03F4 ₁₆	Port P10	P10	
03F5 ₁₆			
03F6 ₁₆	Port P10 direction register	PD10	00 ₁₆
03F7 ₁₆			
03F8 ₁₆			
03F9 ₁₆			
03FA ₁₆	P2 drive capacity	P2DR	00 ₁₆
03FB ₁₆	Timer A Output Drive Capacity	TADR	00 ₁₆
03FC ₁₆	Pull-up control register 0	PUR0	00 ₁₆
03FD ₁₆	Pull-up control register 1	PUR1	00 ₁₆
03FE ₁₆			
03FF ₁₆			

Reset

2.5 Reset

There are two types of resets: hardware and software. In both cases, operation is the same after the reset. (See "Software Reset" for further details regarding software resets.) This section explains on hardware resets.

When the supply voltage is within the range where operation is guaranteed, a reset is effected by holding the reset pin level "L" (0.2V_{CC} max.) for at least 20 f(X_{IN}) cycles. When the reset pin level is then returned to the "H" level while main clock is stable, the reset status is cancelled and program execution resumes from the address in the reset vector table.

Figure 1.9 shows an example of a reset circuit. Figure 1.10 shows the reset sequence.

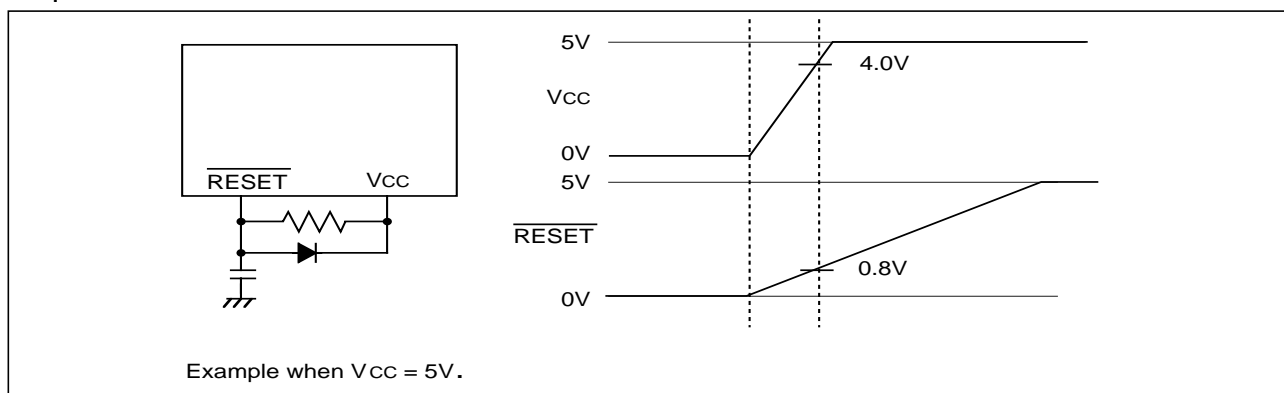


Figure 1.9: Reset circuit

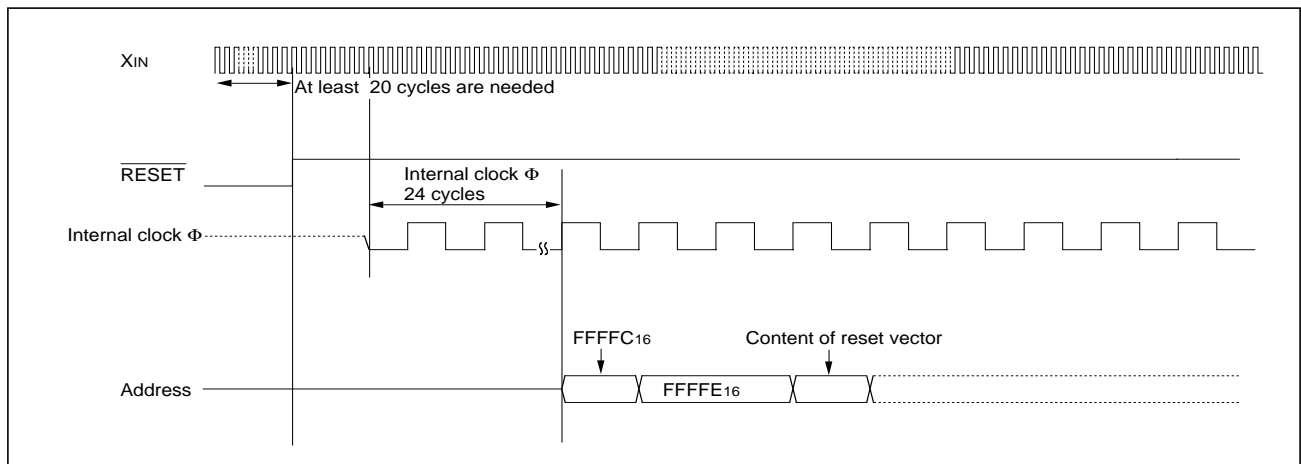


Figure 1.10: Reset sequence

Software Reset

When the RESET pin level = "L", all ports change to input mode (floating.) Table 1.4 shows the status of the other pins while the RESET pin level is "L".

Table 1.4: Main clock-generating circuits

Functions	Main clock-generating circuit
Use of clock	<ul style="list-style-type: none"> • CPU's operating clock source • Internal peripheral units' operating clock source
Usable oscillator	Ceramic or crystal oscillator
Pins to connect oscillator	Xin, Xout
Oscillation stop/restart function	Available
Oscillator status immediately after reset	Oscillating

2.6 Software Reset

Writing a "1" to bit 3 of the processor mode register 0 (address 0004₁₆) applies a (software) reset to the microcomputer. A software reset has almost the same effect as a hardware reset with the following exceptions:

- The contents of internal RAM are preserved
- All USB, DC-DC converter, and PLL SFR values are preserved. (See Section 2.4)

2.7 Clock-Generating Circuit

The clock-generating circuit contains one oscillator circuit that supplies the operating clock sources to the CPU and internal peripheral units. Example of oscillator circuit

Figure 1.11 shows some examples of the main clock circuit, one using an oscillator connected to the circuit, and the other one using an externally derived clock for input. Circuit constants in Figure 1.11 vary with each oscillator used. Use circuit constant values recommended by the oscillator manufacturer.

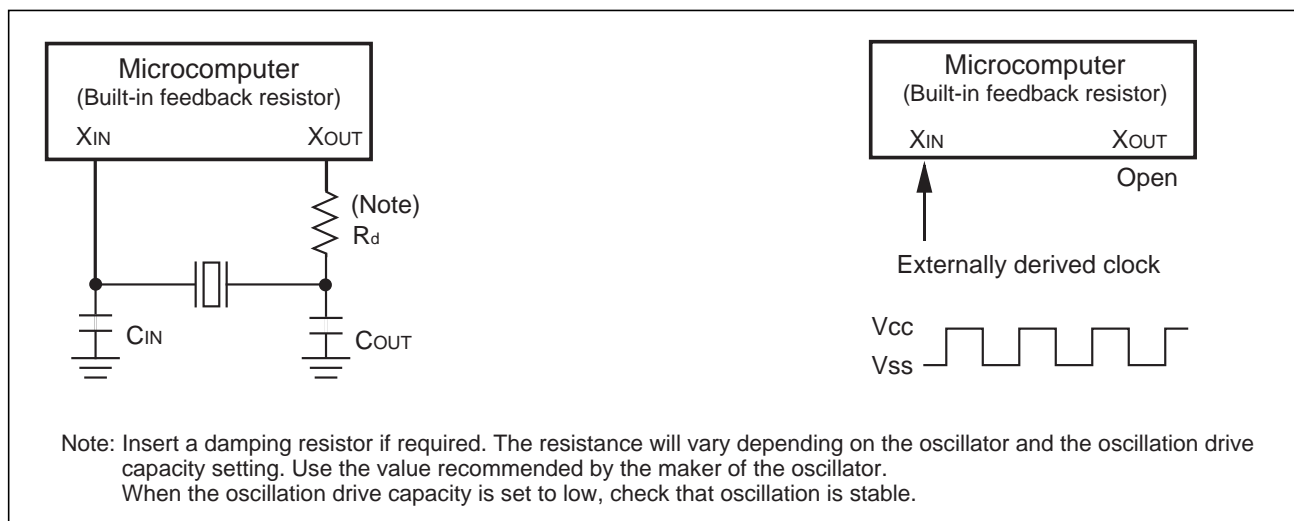


Figure 1.11: Examples of clock source

Clock Control

2.8 Clock Control

Figure 1.12 shows the block diagram of the clock-generating circuit.

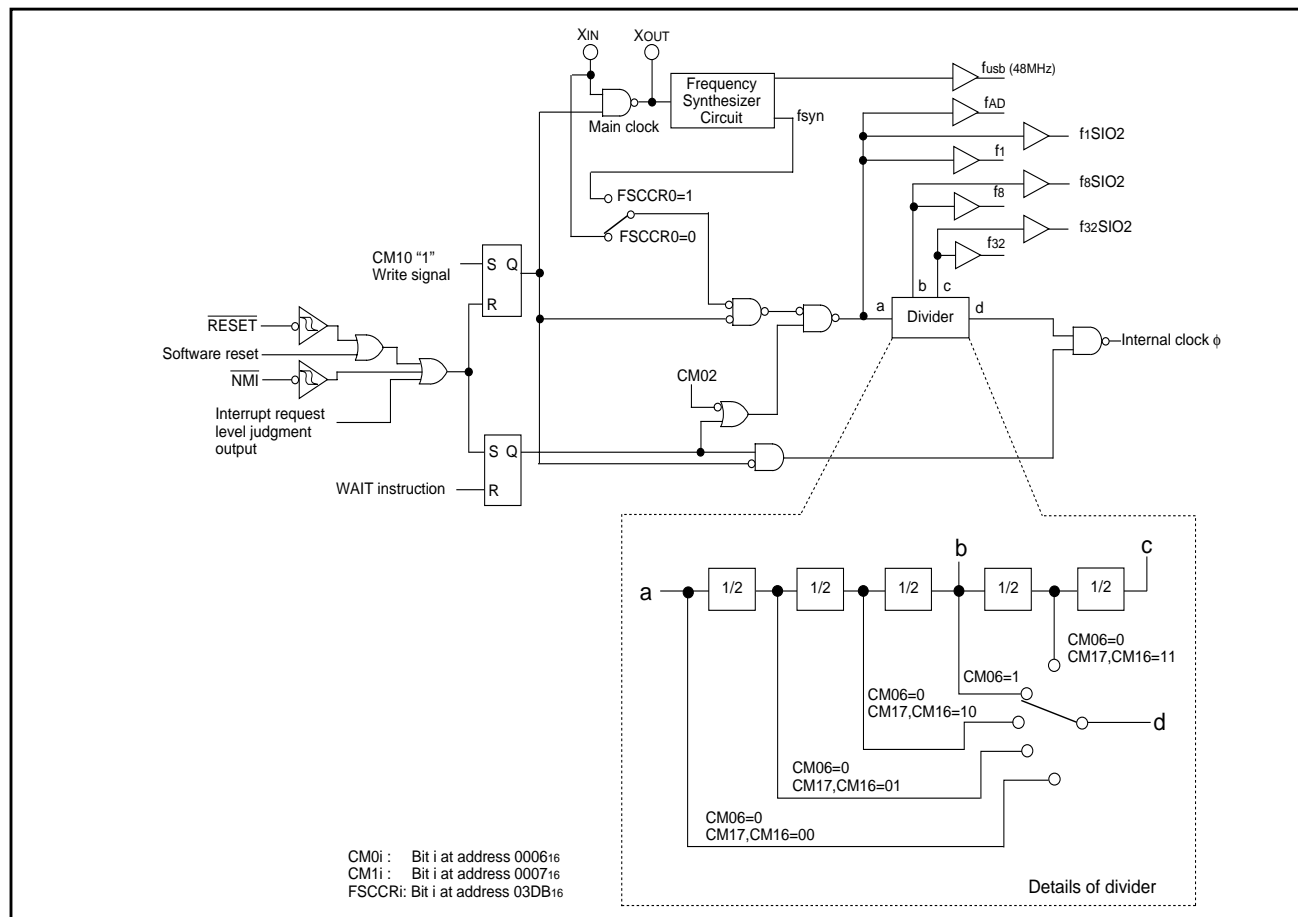


Figure 1.12: Clock-generating circuit

The following paragraphs describe the clocks generated by the clock-generating circuit.

2.8.1 Main clock

The main clock is generated by the main clock oscillation circuit. After a reset, the clock is divided by 8 to the internal clock Φ . The clock can be stopped using the main clock stop bit (bit 5 at address 0006₁₆). Stopping the clock reduces the power dissipation.

After the oscillation of the main clock oscillation circuit has stabilized, the drive capacity of the f(Xout) pin can be reduced using the f(Xin)-f(Xout) drive capacity select bit (bit 5 at address 0007₁₆). Reducing the drive capacity of the f(Xout) pin reduces the power dissipation. This bit defaults to "1" when shifting to stop mode and after a reset.

2.8.2 Internal clock Φ

The internal clock Φ is the clock that drives the CPU, and is either the main clock or is derived by dividing the main clock by 2, 4, 8, or 16. The internal clock Φ is derived by dividing the main clock by 8 after a reset.

When shifting to stop mode, the main clock division select bit (bit 6 at 0006₁₆) is set to "1".

Clock Control

2.8.3 Peripheral function clock

2.8.3.1 • f1, f8, f32

The clock for the peripheral devices is derived from the main clock or by dividing it by 8 or 32. The peripheral function clock is stopped by stopping the main clock or by setting the WAIT peripheral function clock stop bit (bit 2 at 0006₁₆) to "1" and then executing a WAIT instruction.

2.8.3.2 • fAD

This clock has the same frequency as the main clock and is used for A-D conversion.

2.8.4 Clock Output

In single-chip mode, the clock output function select bits (bits 0 and 1 at address 0006₁₆) enable f8 or f32 to be output from the P37/CLKOUT pin. When the WAIT peripheral function clock stop bit (bit 2 at address 0006₁₆) is set to "1", the output of f8 and f32 stops when a WAIT instruction is executed.

Figure 1.13 shows the system clock control registers 0 and 1.

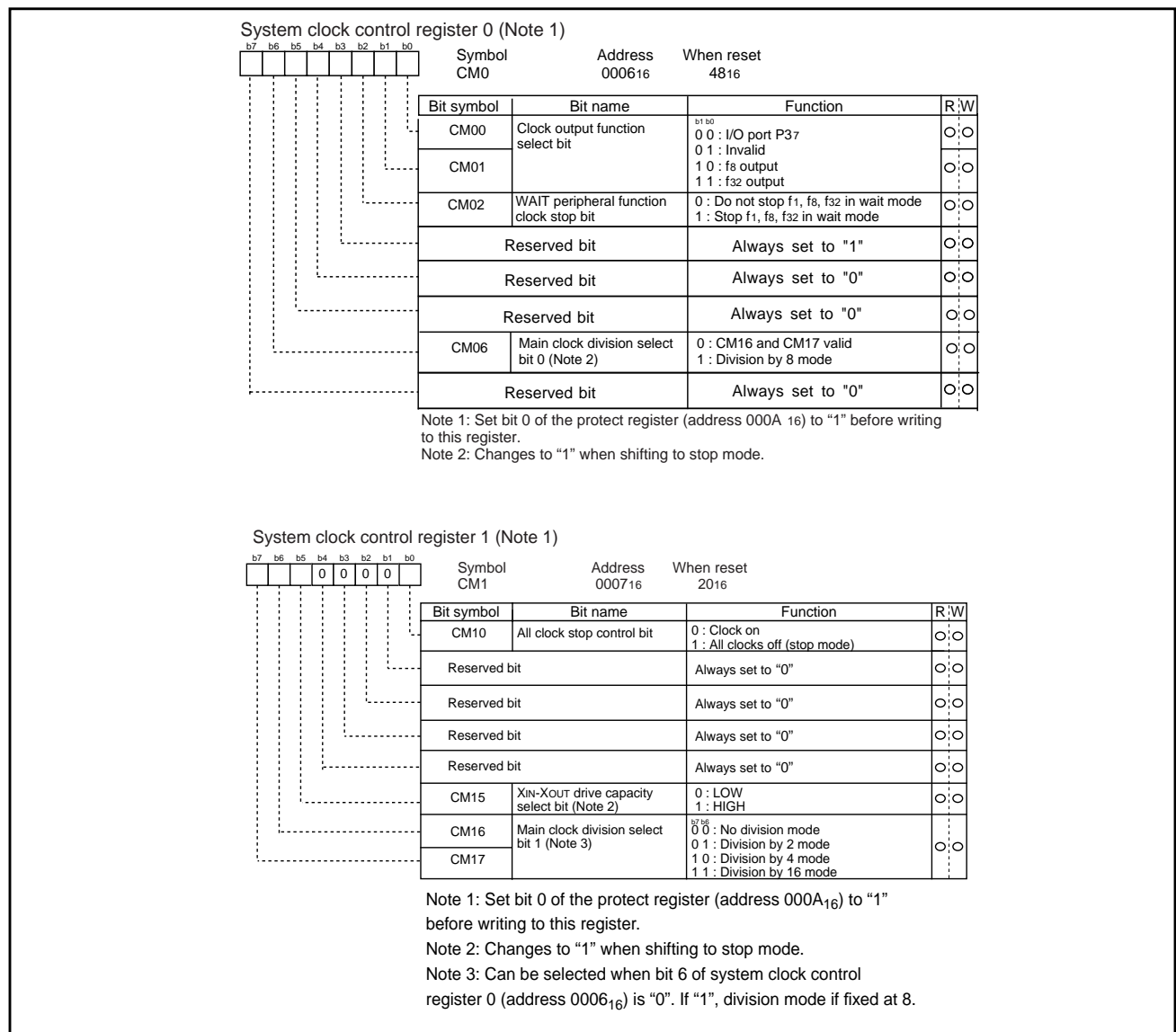


Figure 1.13: System clock control registers 0 and 1

Stop Mode

2.9 Stop Mode

Writing "1" to the all-clock stop control bit (bit 0 at address 0007₁₆) stops all oscillation and the microcomputer enters stop mode. In stop mode, the content of the internal RAM is retained provided that VCC remains above 2V.

Because the oscillation of internal clock Φ , f1 to f32, and fAD stops in stop mode, peripheral functions such as the A-D converter and watchdog timer do not function. However, timer A operates, provided that the event counter mode is set to an external pulse, and UART_i (i = 0 to 2) functions provided an external clock is selected. Table 1.5 shows the status of the ports in stop mode.

Stop mode is cancelled by a hardware reset or interrupt. If an interrupt is to be used to cancel stop mode, that interrupt must first have been enabled. The I flag must also be set prior to stopping for an interrupt to cancel it. After coming out of stop mode, it is recommended that five "NOP" instructions be executed to clear the instruction queue.

When shifting to stop mode, the main clock division select bit 0 (bit 6 at 0006₁₆) is set to "1".

Table 1.5: Port status during stop mode

Pin	Single-chip mode
Port	Retains status before stop mode
CLKOUT	Retains status before stop mode

2.10 Wait Mode

When a WAIT instruction is executed, the internal clock Φ stops and the microcomputer enters the wait mode. In this mode, oscillation continues but the internal clock Φ and watchdog timer stop. Writing "1" to the WAIT peripheral function clock stop bit and executing a WAIT instruction stops the clock being supplied to the internal peripheral functions, allowing power dissipation to be reduced. Table 1.6 shows the status of the ports in wait mode.

Wait mode is cancelled by a hardware reset or interrupt. If an interrupt is used to cancel wait mode, the microcomputer restarts using as internal clock Φ the clock that had been selected when the WAIT instruction was executed

Table 1.6: Port status during wait mode

Pin	Single-chip mode
Port	Retains status before stop mode
CLKout	Does not stop when the WAIT peripheral function clock stop bit is "0" When the WAIT peripheral function clock stop bit is "1", the status immediately prior to entering wait mode is maintained.

2.11 Status Transition Of the Internal Clock Φ

Power dissipation can be reduced and low-voltage operation achieved by changing the count source for internal clock Φ . Table 1.7 shows the operating modes corresponding to the settings of system clock control registers 0 and 1.

After a reset, operation defaults to division by 8 mode. When shifting to stop mode, the main clock division select bit 0 (bit 6 at address 0006₁₆) is set to "1". The following shows the operational modes of internal clock

2.11.1 Division by 2 mode

The main clock is divided by 2 to obtain the internal clock Φ .

Power Control

2.11.2 Division by 4 mode

The main clock is divided by 4 to obtain the internal clock Φ .

2.11.3 Division by 8 mode

The main clock is divided by 8 to obtain the internal clock Φ . Note that oscillation of the main clock must have stabilized before transferring from this mode to another mode.

2.11.4 Division by 16 mode

The main clock is divided by 16 to obtain the internal clock Φ .

2.11.5 No-division mode

The main clock is used as internal clock.

Table 1.7: Operating modes dictated by settings of system clock control registers 0 and 1

CM17	CM16	CM06	Operating mode of internal clock
0	1	0	Division by 2 mode
1	0	0	Division by 4 mode
Invalid	Invalid	1	Division by 8 mode
1	1	0	Division by 16 mode
0	0	0	No-division mode

2.12 Power Control

The following is a description of the three available power control modes:

2.12.0.1 Normal Operation Mode

- High-speed mode

Divide-by-1 frequency of the main clock become the internal clock Φ . The CPU operates with the internal clock selected. Each peripheral function operates according to its assigned clock.

- Medium-speed mode

Divide-by-2, divide-by-4, divide-by-8, or divide-by-16 frequency of the main clock becomes the internal clock Φ . The CPU operates according to the internal clock selected. Each peripheral function operates according to its assigned clock.

2.12.0.2 Wait mode

The CPU operation is stopped. The oscillators do not stop.

2.12.0.3 Stop Mode

All oscillators stop. The CPU and all built-in peripheral functions stop. Of the three modes listed, this mode is the most effective in decreasing power consumption.

Protection

2.13 Protection

The protection function is provided so that the values in important registers cannot be changed in the event that the program runs out of control. Figure 1.14 shows the protect register. The values in the processor mode register 0 (address 0004₁₆), processor mode register 1 (address 0005₁₆), system clock control register 0 (address 0006₁₆), system clock control register 1 (address 0007₁₆) and frequency synthesizer registers can only be changed when the respective bit in the protect register is set to "1".

The system clock control registers 0 and 1 write-enable bit (bit 0 at 000A₁₆) and processor mode register 0 and 1 write-enable bit (bit 1 at 000A₁₆) do not automatically return to "0" after a value has been written to an address. The program must therefore be written to return these bits to "0".

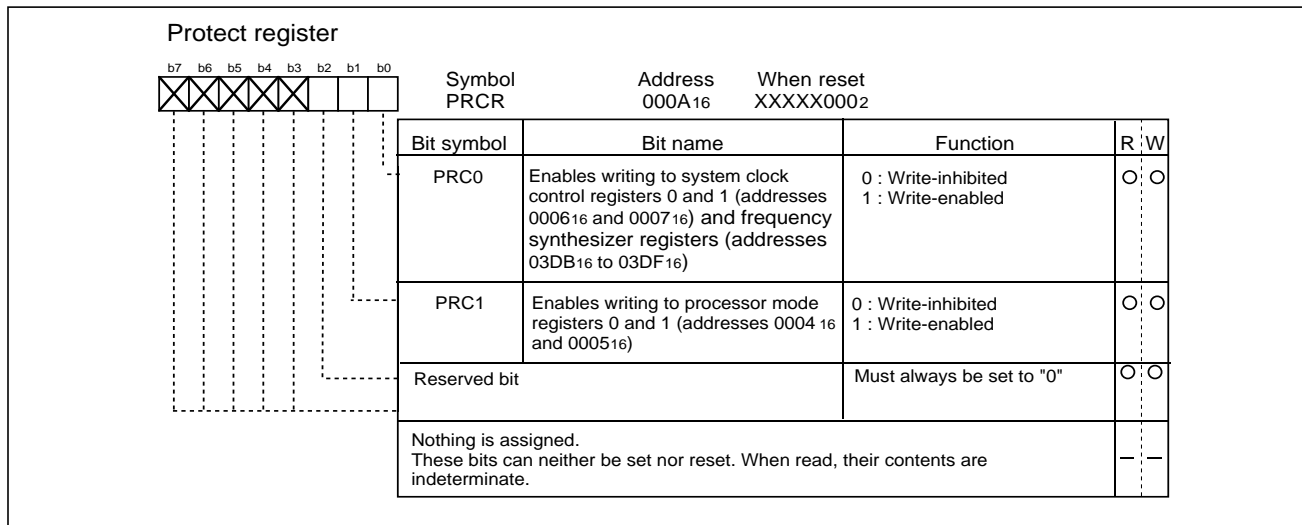


Figure 1.14: Protect register

Interrupts

2.14 Interrupts

Table 1.8 and Table 1.9 show the interrupt sources and vector table addresses. When an interrupt is received, the program is executed from the address shown by the respective interrupt vector.

The vector table addresses for the interrupts in Table 7 are fixed (interrupt vector addresses). These interrupts are not affected by the interrupt enable flag (I flag) (non-maskable interrupts).

The vector table addresses for the interrupts in Table 8 are variable, being determined as relative to the fixed address in the interrupt table register (INTB). These interrupts can be enabled or disabled using the interrupt enable flag (I flag) (maskable interrupts). Sixty four vectors can be set in the interrupt table register (INTB). Any of software interrupts 0 to 63 can be assigned to each vector. By using the INT instruction to specify a software interrupt number, the program can be executed starting at the address indicated by the respective vector. The BRK instruction interrupt has interrupt vectors in both the fixed vector address and variable vector address. When the contents of FFFE4₁₆ through FFFE7₁₆ are all "FF₁₆", the program is executed from the address shown in the BRK instruction interrupt vector in the variable vector address.

Specify the starting address of the interrupt program in the interrupt vector. Figure 1.15 shows the format for specifying the address.

Table 1.8: Interrupt vectors (fixed interrupt vector addresses)

Interrupt source	Vector table addresses Address(L) to Address(H)	Remarks
Undefined instruction	FFFDC ₁₆ to FFFDF ₁₆	Interrupt on UND instruction
Overflow	FFFE0 ₁₆ to FFFE3 ₁₆	Interrupt on INTO instruction
BRK instruction	FFFE4 ₁₆ to FFFE7 ₁₆	If the vector is filled with FF ₁₆ , program execution starts from the address shown by the vector in the variable vector table
Address Match	FFFE8 ₁₆ to FFFEB ₁₆	There is an address-matching interrupt enable bit
Single Step (Note)	FFFE _C ₁₆ to FFFE _F ₁₆	Do not use
Watchdog timer	FFFF0 ₁₆ to FFF3 ₁₆	
\overline{DBC} (Note)	FFFF4 ₁₆ to FFFF7 ₁₆	Do not use
NMI	FFFF8 ₁₆ to FFFFB ₁₆	External interrupt by NMI pin
Reset	FFFFC ₁₆ to FFFFF ₁₆	

Note: Interrupts used for debugging purposes only

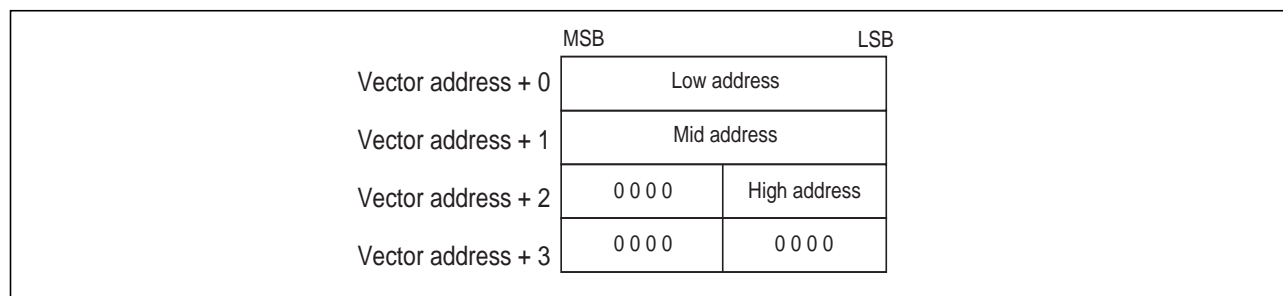


Figure 1.15: Format for specifying interrupt vector addresses

Interrupts

Table 1.9: Interrupt vectors (variable interrupt vector addresses)

Software interrupt number	Vector table addresses Address(L) to Address(H)	Interrupt source	Remarks
Software interrupt number 0	+0 to +3 (Note 1)	BRK instruction	Cannot be masked by I flag
Software interrupt number 4	+16 to +19	USB Suspend	
Software interrupt number 6	+24 to +27	USB Resume	
Software interrupt number 7	+28 to +31	USB Start of Frame	
Software interrupt number 10	+40 to +43	Bus collision detection	
Software interrupt number 11	+44 to +47	DMA0	
Software interrupt number 12	+48 to +51	DMA1	
Software interrupt number 13	+52 to +55	Key input interrupt	
Software interrupt number 14	+56 to +59	A-D	
Software interrupt number 15	+60 to +63	UART2 transmit	
Software interrupt number 16	+64 to +67	UART2 receive	
Software interrupt number 17	+68 to +71	UART0 transmit	
Software interrupt number 18	+72 to +75	UART0 receive	
Software interrupt number 19	+76 to +79	UART1 transmit	
Software interrupt number 20	+80 to +83	UART1 receive	
Software interrupt number 21	+84 to +87	Timer A0	
Software interrupt number 22	+88 to +91	Timer A1	
Software interrupt number 23	+92 to +95	Timer A2	
Software interrupt number 24	+96 to +99	Timer A3	
Software interrupt number 25	+100 to +103	Timer A4	
Software interrupt number 26	+104 to +107	Timer B0	
Software interrupt number 27	+108 to +111	Timer B1	
Software interrupt number 28	+112 to +115	USB Reset	
Software interrupt number 29	+116 to +119	INT0	
Software interrupt number 30	+120 to +123	INT1	
Software interrupt number 31	+124 to +127	USB Function	
Software interrupt number 32 to Software interrupt number 63	+252 to +255	Software interrupt	Cannot be masked by I flag

Note 1: Address relative to address in interrupt table base address register (INTB)

Interrupts

2.14.1 Interrupt control registers

Peripheral I/O interrupts have their own interrupt control registers. Table 1.10 shows the addresses of the interrupt control registers. Figure 1.16 shows the interrupt control registers.

The interrupt request bit is set by hardware to “0” when an interrupt request is received. The interrupt request bit can also be set by software to “0”. (Do not set to “1”.)

$\overline{INT}0$ and $\overline{INT}1$ are triggered by the edges of external inputs. The edge polarity is selected using the polarity select bit. (Other interrupts are described elsewhere.)

An interrupt must first be enabled before it can be used to cancel stop mode.

Table 1.10: Addresses in interrupt control register

Interrupt control register	Symbol name	Address	Interrupt control register	Symbol name	Address
USB Suspend Interrupt	SUSPIC	0044 ₁₆	UART1 receive	S1RIC	0054 ₁₆
USB Resume interrupt	RSMIC	0046 ₁₆	Timer A0	TA0IC	0055 ₁₆
USB Start Of Frame	SOFIC	0047 ₁₆	Timer A1	TA1IC	0056 ₁₆
Bus collision detection	BCNIC	004A ₁₆	Timer A2	TA2IC	0057 ₁₆
DMA0	DM0IC	004B ₁₆	Timer A3	TA3IC	0058 ₁₆
DMA1	DM1IC	004C ₁₆	Timer A4	TA4IC	0059 ₁₆
Key input interrupt	KUPIC	004D ₁₆	Timer B0	TB0IC	005A ₁₆
A-D	ADIC	004E ₁₆	Timer B1	TB1IC	005B ₁₆
UART2 transmit	S2TIC	004F ₁₆	USB Reset	RSTIC	005C ₁₆
UART2 receive	S2RIC	0050 ₁₆	INT0	INT0IC	005D ₁₆
UART0 transmit	S0TIC	0051 ₁₆	INT1	INT1IC	005E ₁₆
UART0 receive	S0RIC	0052 ₁₆	USB Function	USBFIC	005F ₁₆
UART1 transmit	S1TIC	0053 ₁₆			

Interrupts

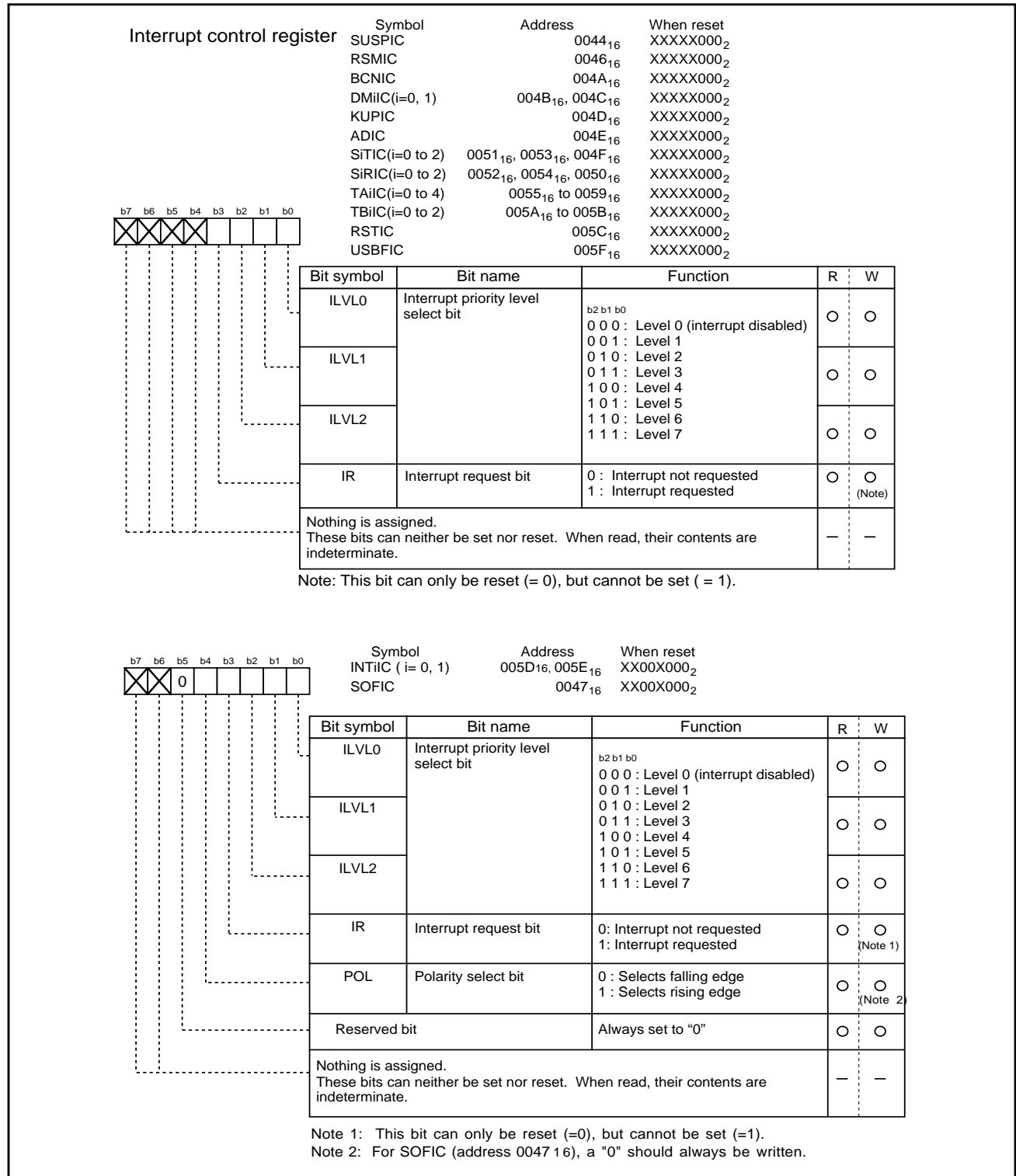


Figure 1.16: Interrupt control registers



Interrupts

2.14.2 Interrupt priority

The order of priority when two or more interrupts are generated simultaneously is determined by both hardware and software.

The interrupt priority levels determined by hardware are reset > $\overline{\text{NMI}}$ > $\overline{\text{DBC}}$ > watchdog timer > peripheral I/O interrupts > single-step > address matching interrupt.

The interrupt priority levels determined by software are set in the interrupt control registers.

Figure 1.17 shows the circuit that judges the interrupt hardware priority level. When two or more interrupts are generated simultaneously, the interrupt with the higher software priority is selected. However, if the interrupts have the same software priority level, the interrupt is selected according to the hardware priority set in the circuit.

The selected interrupt is accepted only when the priority level is higher than the processor interrupt priority level (IPL) in the flag register (FLG) and the interrupt enable flag (I flag) is "1". Note that the reset, $\overline{\text{NMI}}$, $\overline{\text{DBC}}$, watchdog timer, single-step, address-match, BRK instruction, overflow, and undefined instruction interrupts are accepted regardless of the interrupt enable flag (I flag).

Interrupts

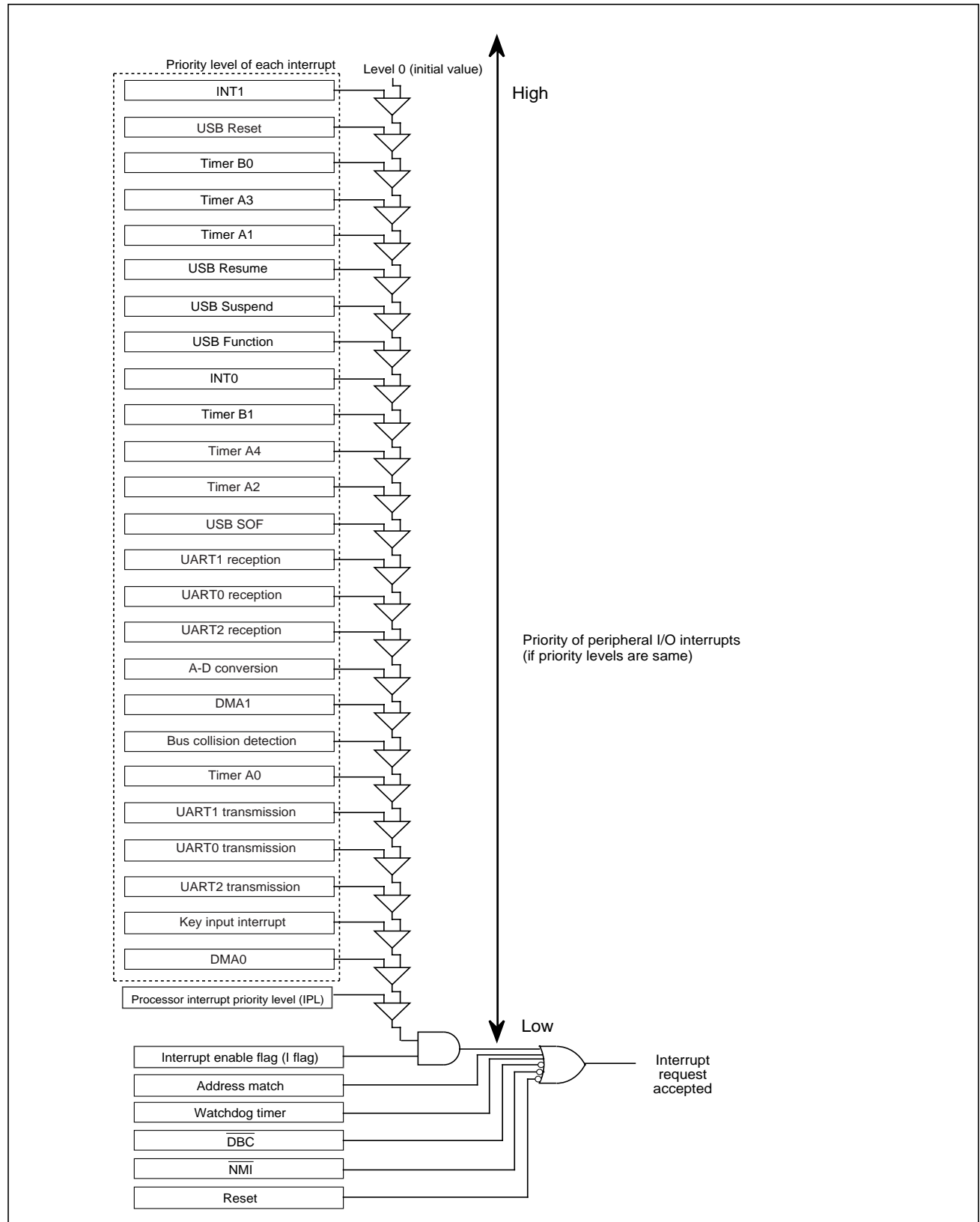


Figure 1.17: Interrupt resolution circuit

NMI Interrupt

2.14.3 Flag changes

When an interrupt request is received, the stack pointer select flag (U flag) changes to “0” and the flag register (FLG) and program counter (PC) are saved to the stack area indicated by the interrupt stack pointer (ISP). Thereafter, the interrupt enable flag (I flag) and debug flag (D flag) change to “0” and the processor interrupt priority level (IPL) at the flag register (FLG) is replaced by the priority level of the received interrupt. However, when interrupt requests are received for software interrupts 32 to 63, the flag register (FLG) and program counter (PC) are saved to the stack shown by the stack pointer select flag (U flag) at the time the interrupt was received. The stack pointer select flag (U flag) does not change. The value of the processor interrupt priority level (IPL) in the flag register (FLG) differs in the case of reset, $\overline{\text{NMI}}$, $\overline{\text{DBC}}$, watchdog timer, single-step, address-match, BRK instruction, overflow, and undefined instruction interrupts. Table 1.11 shows how the IPL changes when interrupt requests are received.

Table 1.11: Change of IPL state when interrupt request are accepted

Interrupt	Change of IPL
Reset	Level 0 (“000 ₂), is set
$\overline{\text{NMI}}$	Level 7 (“111 ₂), is set
$\overline{\text{DBC}}$	Does not change
Watchdog timer	Level 7 (“111 ₂), is set
Single step	Does not change
Address match	Does not change
Software interrupt	Does not change

2.13 $\overline{\text{NMI}}$ Interrupt

An $\overline{\text{NMI}}$ interrupt is generated when the input to the P85/ $\overline{\text{NMI}}$ pin changes from “H” to “L”. The $\overline{\text{NMI}}$ interrupt is a non-maskable external interrupt. The pin level can be checked in the Port P85 register (bit 5 at address 03F0₁₆).

This pin cannot be used as a normal port input.

2.13.1 Notes:

- (1) When not intending to use the $\overline{\text{NMI}}$ function, be sure to connect the $\overline{\text{NMI}}$ pin to VCC. Because the $\overline{\text{NMI}}$ interrupt is non-maskable, it cannot be disabled.
- (2) When the $\overline{\text{NMI}}$ pin input is “L”, do not set the microcomputer in stop mode or wait mode. The $\overline{\text{NMI}}$ interrupt is triggered by the falling edge, so the “L” level does not need to be maintained longer than necessary.

Key-Input Interrupt

2.14 Key-Input Interrupt

If the direction register of any of pin of Port0 or Port1 is set for input and a falling edge is input to that port, a key-input interrupt is generated. A key-input interrupt can also be used as a key-on wakeup function for cancelling the wait mode or stop mode. Figure 1.18 shows the block diagram of the key-input interrupt.

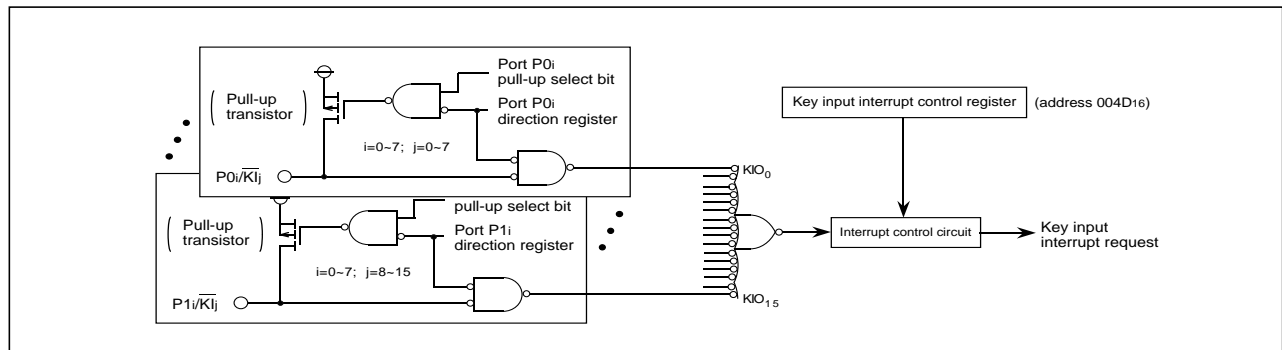


Figure 1.18: Block diagram of key input interrupt

2.14.1 Enabling/disabling the key-input interrupt

The key-input interrupt can be enabled and disabled using the key-input interrupt register (004D₁₆). The key-input interrupt is affected by the interrupt priority level (IPL) and the interrupt enable flag (I flag).

2.14.2 Occurrence timing of the key-input interrupt

With key-input interrupt acceptance enabled, ports P0 and P1, which are set to input, become key-input interrupt pins ($\overline{KI0}$ through $\overline{KI15}$). A key-input interrupt occurs when a falling edge is input to a key-input interrupt pin. At this moment, the level of other key-input interrupt pins must be "H". No interrupt occurs when the level of any other key-input interrupt pins is "L".

2.14.3 How to determine a key-input interrupt

A key-input interrupt occurs when a falling edge is input to one of 16 pins, but each pin has the same vector address. Therefore, read the input level of ports P0 and P1 in the key-input interrupt routine to determine the interrupted pin.

Key-Input Interrupt

2.14.4 Registers related to the key-input interrupt

Figure 1.19 shows the memory map of key-input interrupt-related registers

Key-input interrupt control register (KUPIC)	04D ₁₆
Port 0 (P0)	3E0 ₁₆
Port 1 (P1)	3E1 ₁₆
Port 0 direction register	3E2 ₁₆
Port 1 direction register	3E3 ₁₆
Pull-up control register 0	3FC ₁₆
Pull-up control register 1	3FD ₁₆

Figure 1.19: Memory Map of key input interrupt related registers

Address Match Interrupt

2.15 Address Match Interrupt

An address match interrupt is generated when the address match interrupt address register contents match the program counter value. Two address match interrupts can be set, each of which can be enabled and disabled by an address match interrupt enable bit. Address match interrupts are not affected by the interrupt enable flag (I flag) and processor interrupt priority level (IPL).

Figure 1.20 shows the address match interrupt-related registers.

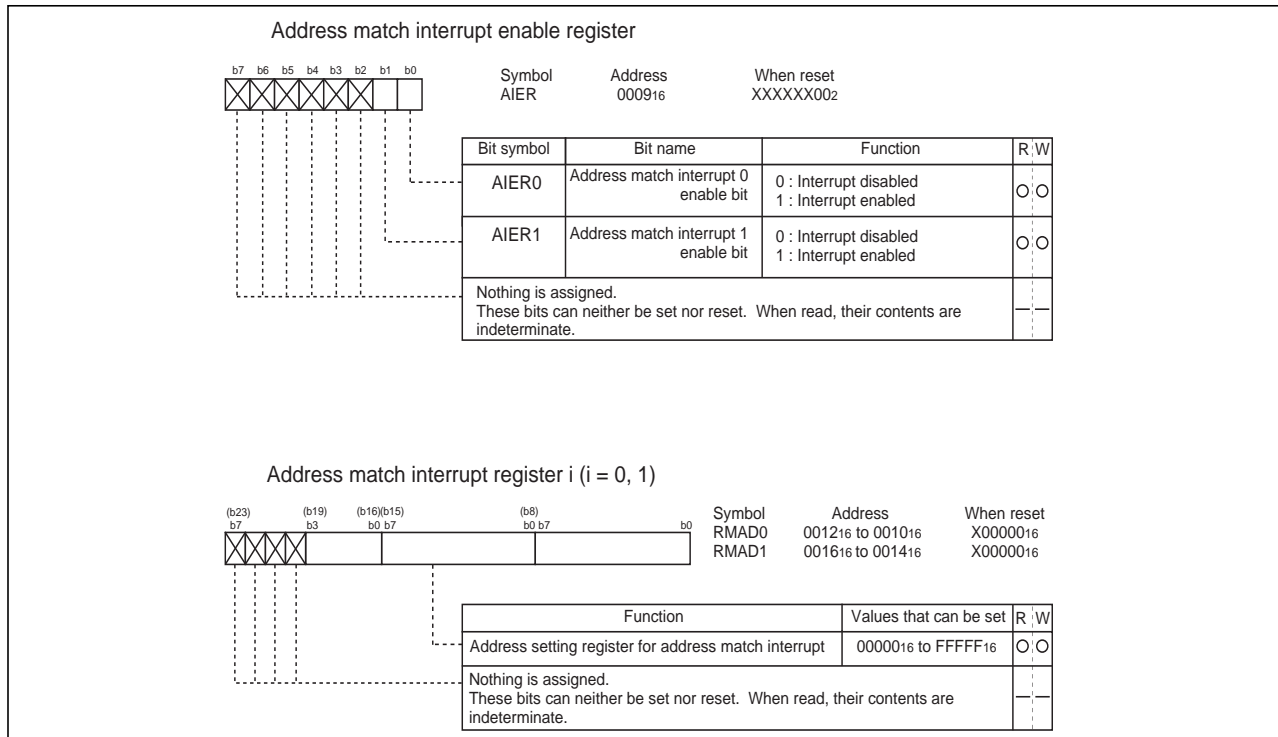


Figure 1.20: Address match interrupt-related registers



Watchdog Timer

2.16 Watchdog Timer

The watchdog timer has the function of detecting when the program is out of control. The watchdog timer is 39a 15-bit counter that decrements using the clock derived by dividing the internal clock Φ using the prescaler. A watchdog timer interrupt is generated when an underflow occurs in the watchdog timer. Bit 7 of the watchdog timer control register (address 000F₁₆) selects the prescaler division ratio (by 16 or 128). Table 1.12 shows the periodic table for the watchdog timer.

Table 1.12: Watchdog timer periodic table (f(X_{IN})=10MHz)

CM06	CM17	CM16	Internal clock Φ	WDC7	Period
0	0	0	10MHz	0	Approx. 52.4ms
				1	Approx. 419.2ms
0	0	1	5MHz	0	Approx. 104.9ms
				1	Approx. 838.8ms
0	1	0	2.5MHz	0	Approx. 209.7ms
				1	Approx. 1.68s
0	1	1	0.625MHz	0	Approx. 838.8ms
				1	Approx. 6.71s
1	Invalid	Invalid	1.25MHz	0	Approx. 419.2ms
				1	Approx. 3.35s

The watchdog timer is initialized by writing to the watchdog timer start register (address 000E₁₆) and when a watchdog timer interrupt request is generated. The prescaler is initialized only when the microcomputer is reset. After a reset is cancelled, the watchdog timer and prescaler are both stopped. The count is started by writing to the watchdog timer start register (address 000E₁₆).

Figure 1.21 shows the block diagram of the watchdog timer. Figure 1.22 shows the watchdog timer-related registers.

Watchdog Timer

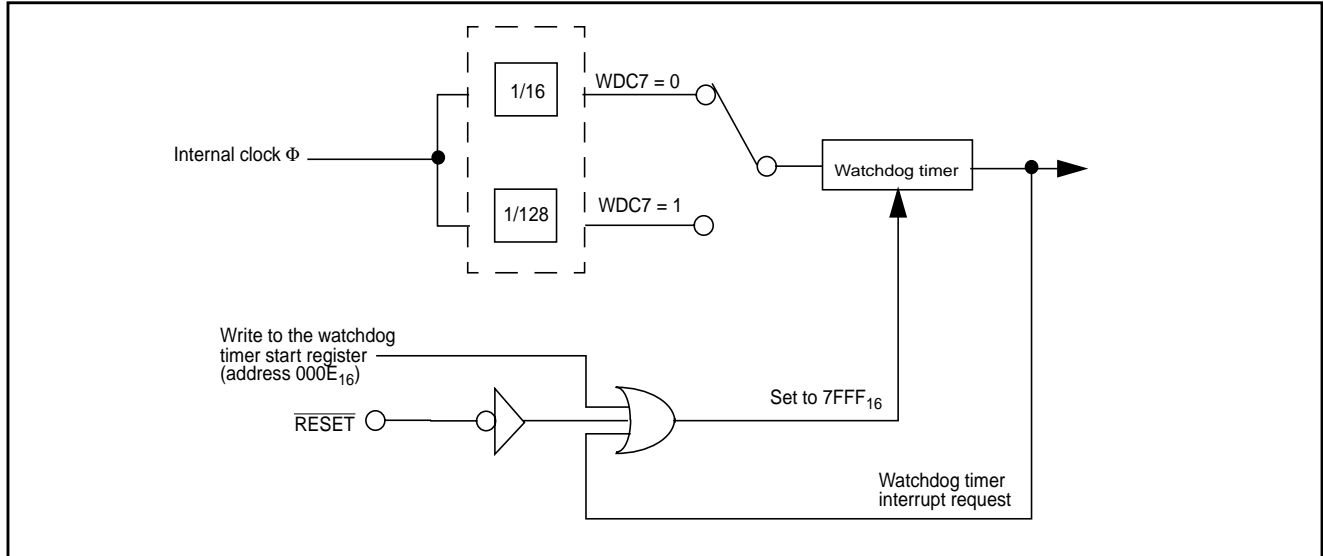


Figure 1.21: Block diagram of watchdog timer

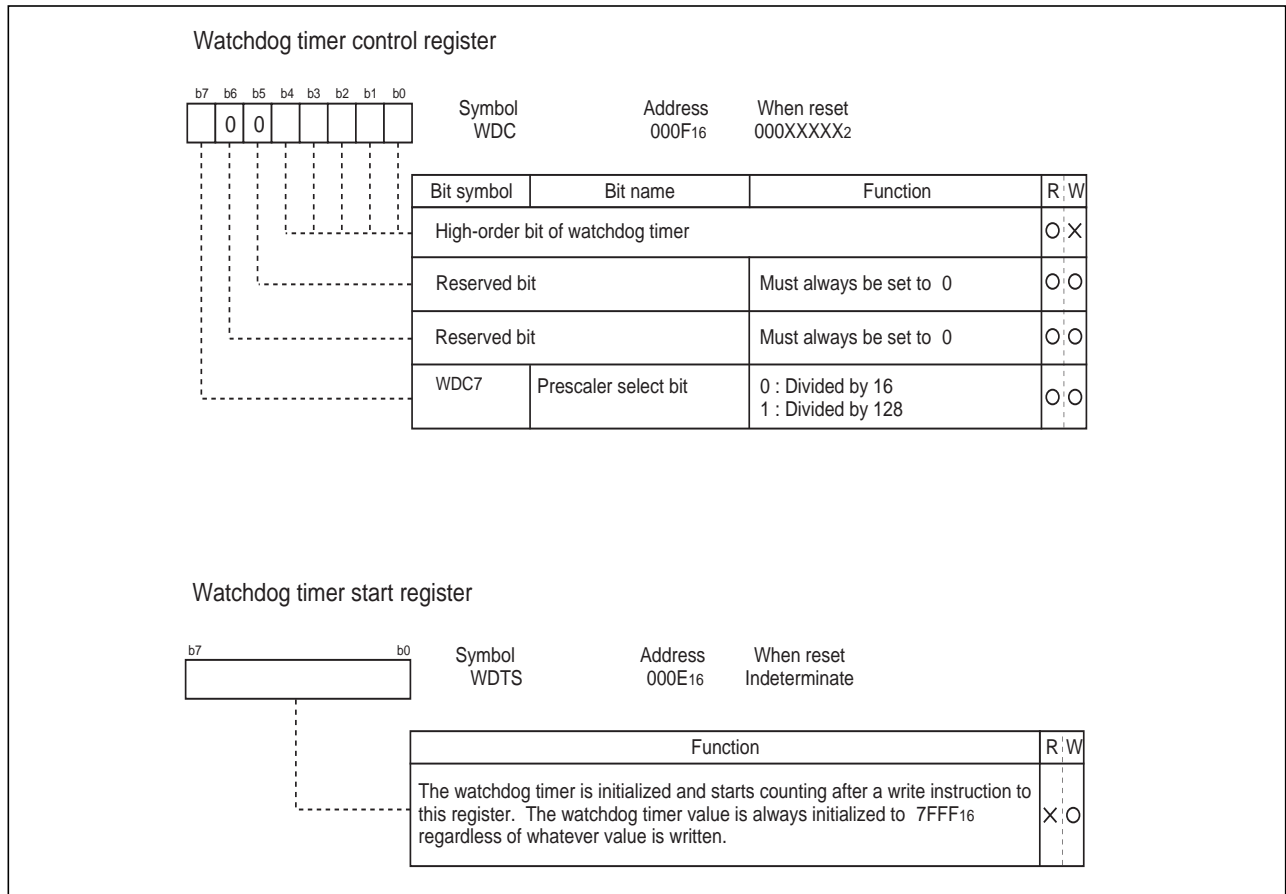


Figure 1.22: Watchdog timer control and start registers

Frequency Synthesizer Circuit

2.17 Frequency Synthesizer Circuit

The Frequency Synthesizer Circuit generates a 48MHz clock needed by the USB block and a clock f_{SYN} that are both a multiple of the external input reference clock $f(Xin)$. A block diagram of the circuit is shown in Figure 1.23.

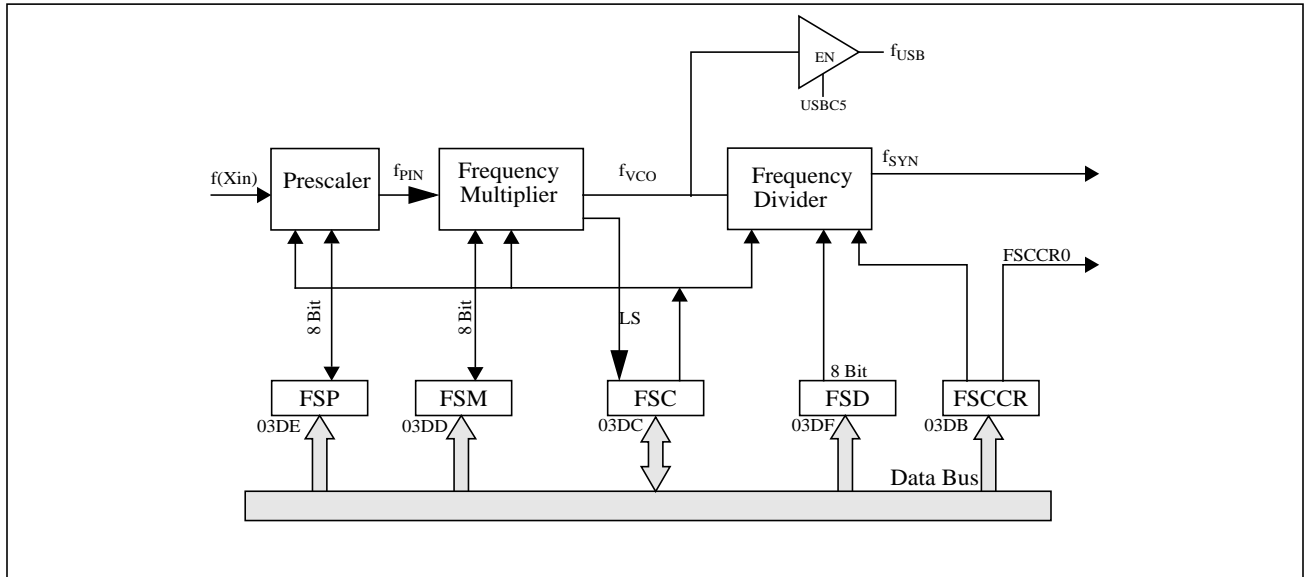


Figure 1.23: Frequency Synthesizer Circuit

The frequency synthesizer consists of a prescaler, frequency multiplier macro, a frequency divider macro, and five registers, namely FSP, FSM, FSC, FSD, and FSCCR. Clock $f(Xin)$ is prescaled down using FSP to generate f_{PIN} . f_{PIN} is multiplied using FSM to generate an f_{VCO} clock which is then divided using FSD to produce the clock f_{SYN} . The f_{VCO} clock is optimized for 48 MHz operation and is buffered and sent out of the frequency synthesizer block as signal f_{USB} . This signal is used by the USB block.

2.17.1 Prescaler

Clock f_{PIN} is a divided down version of clock $f(Xin)$ (see Figure 1.24). The relationship between f_{PIN} and the clock input to the prescaler $f(Xin)$ is as follows:

- $f_{PIN} = f(Xin) / 2(n+1)$ where n is a decimal number between 0 and 254.
 Setting FSP to 255 disables the prescaler and $f_{PIN} = f(Xin)$.
- Note: $f(Xin)$ frequency below 1 MHz is not recommended.

MSB 7	Bit 7	Bit 6	Bit 5 ₂	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	LSB 0	Address: 03DE ₁₆ Access: R/W Reset: FF ₁₆																									
<table border="1"> <thead> <tr> <th rowspan="2">f_{PIN}</th> <th colspan="2">FSP</th> <th rowspan="2">$f(Xin)$</th> </tr> <tr> <th>Dec(n)</th> <th>Hex(n)</th> </tr> </thead> <tbody> <tr> <td>12 MHz</td> <td>255</td> <td>FF</td> <td>12.00 MHz</td> </tr> <tr> <td>1 MHz</td> <td>5</td> <td>05</td> <td>12.00 MHz</td> </tr> <tr> <td>2 MHz</td> <td>2</td> <td>02</td> <td>12.00 MHz</td> </tr> <tr> <td>3 MHz</td> <td>1</td> <td>01</td> <td>12.00 MHz</td> </tr> <tr> <td>6 MHz</td> <td>0</td> <td>00</td> <td>12.00 MHz</td> </tr> </tbody> </table>										f_{PIN}	FSP		$f(Xin)$	Dec(n)	Hex(n)	12 MHz	255	FF	12.00 MHz	1 MHz	5	05	12.00 MHz	2 MHz	2	02	12.00 MHz	3 MHz	1	01	12.00 MHz	6 MHz	0	00	12.00 MHz
f_{PIN}	FSP		$f(Xin)$																																
	Dec(n)	Hex(n)																																	
12 MHz	255	FF	12.00 MHz																																
1 MHz	5	05	12.00 MHz																																
2 MHz	2	02	12.00 MHz																																
3 MHz	1	01	12.00 MHz																																
6 MHz	0	00	12.00 MHz																																
$f(Xin)/2(n+1) = f_{PIN}$																																			

Figure 1.24: Frequency Synthesizer Prescaler Register (FSP)

Frequency Synthesizer Circuit

2.17.2 Multiplier

Clock f_{VCO} is a multiplied up version of clock f_{PIN} (See Figure 1.25). The relationship between f_{VCO} and the clock input to the multiplier (f_{PIN}) from the prescaler is as follows:

- $f_{VCO} = f_{PIN} \times 2(n+1)$ where n is the decimal equivalent of the value loaded in FSM.
 Setting FSM to 255 disables the multiplier and $f_{VCO} = f_{PIN}$.

Note 1: n must be chosen such that f_{VCO} equals 48 MHz.

Note 2: Minimum f_{PIN} is 1 MHz.

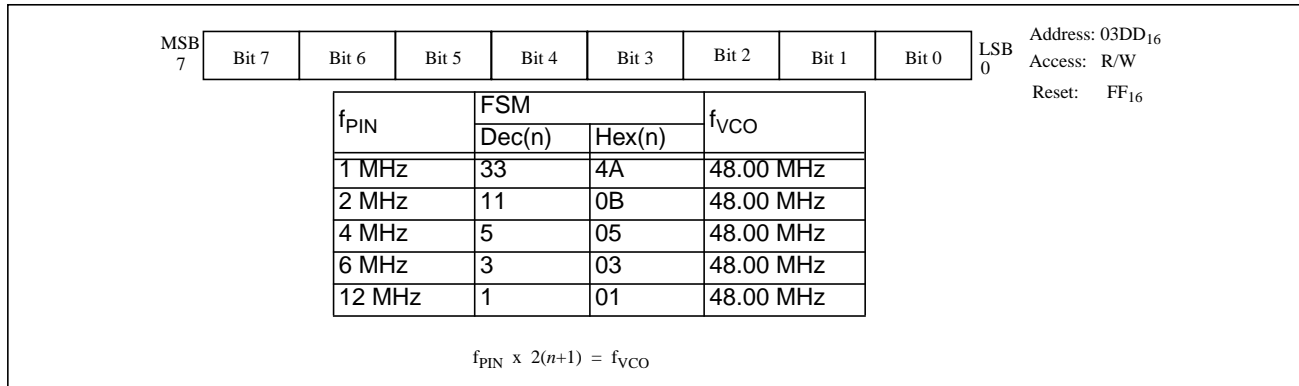


Figure 1.25: Frequency Synthesizer Multiply Register (FSM)

2.17.3 Divider

Clock f_{SYN} is a divided down version of clock f_{VCO} (See Figure 1.26). The relationship between f_{SYN} and the clock input to the divider (f_{VCO}) from the multiplier is as follows:

- $f_{SYN} = f_{VCO} / 2(m+1)$ where m is the decimal equivalent of the value loaded in FSD.
 Setting FSD to 255 disables the divider and $f_{SYN} = f_{VCO}$.

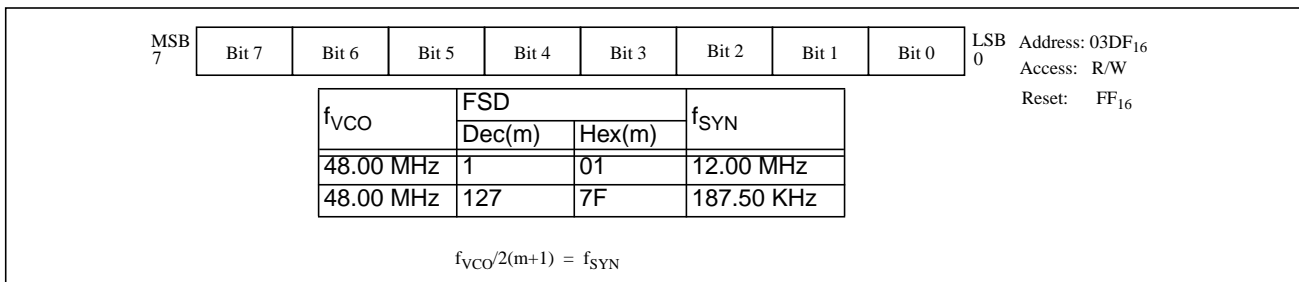


Figure 1.26: Frequency Synthesizer Divide Register (FSD)

Frequency Synthesizer Circuit

The FSC0 bit in the FSC Control Register enables the frequency synthesizer block. When disabled (FSC0 = "0"), f_{VCO} is held at either a high or low state. When the frequency synthesizer control bit is active (FSC0 = "1"), a lock status (LS = "1") indicates that f_{SYN} and f_{VCO} are the correct frequency. The LS and FSC0 control bits in the FSC Control register are shown in Figure 1.27.

When using the frequency synthesizer, a low-pass filter must be connected to the LPF pin.

Once the frequency synthesizer is enabled, a delay of 2-5ms is recommended before the output of the frequency synthesizer is used. This is done to allow the output to stabilize. It is also recommended that none of the registers be modified once the frequency synthesizer is enabled as it will cause the output to be temporarily (2-5ms) unstable. The MCU clock source is selected via the Frequency Synthesizer Clock Control register (FSCCR). See Figure 1.28.

Note: None of the registers must be written to once the frequency synthesizer is enabled and used as the system clock source (FSCCR register, address 03DB₁₆, bit '0' set to '1') because it will cause the output of the PLL to freeze. Switch system back to $f(X_{IN})$ and disable before modifying PLL registers.

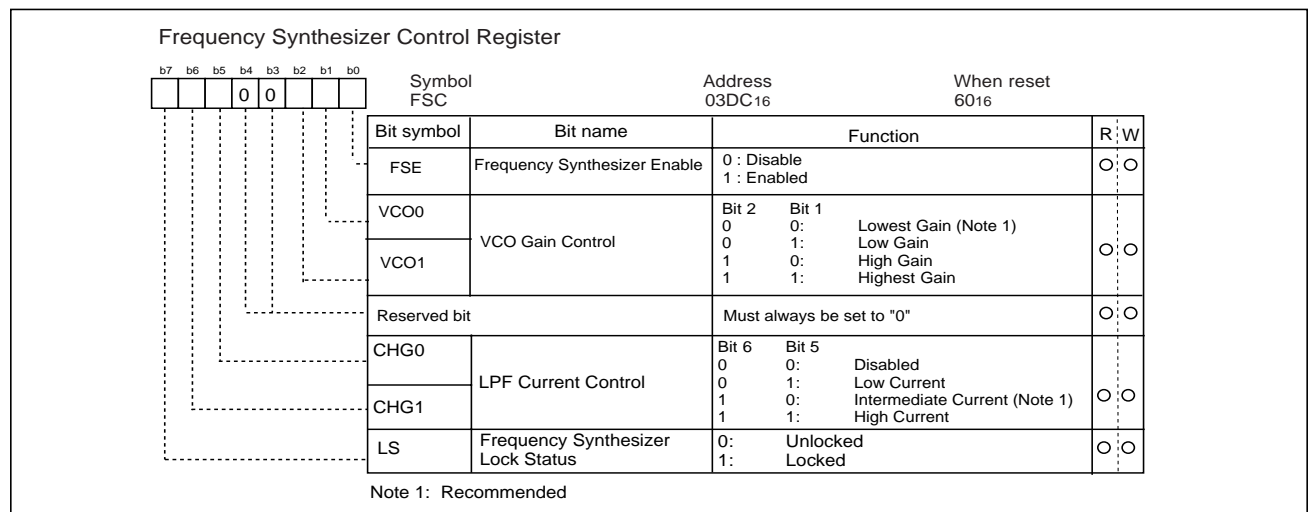


Figure 1.27: Frequency Synthesizer Control Register (FSC)

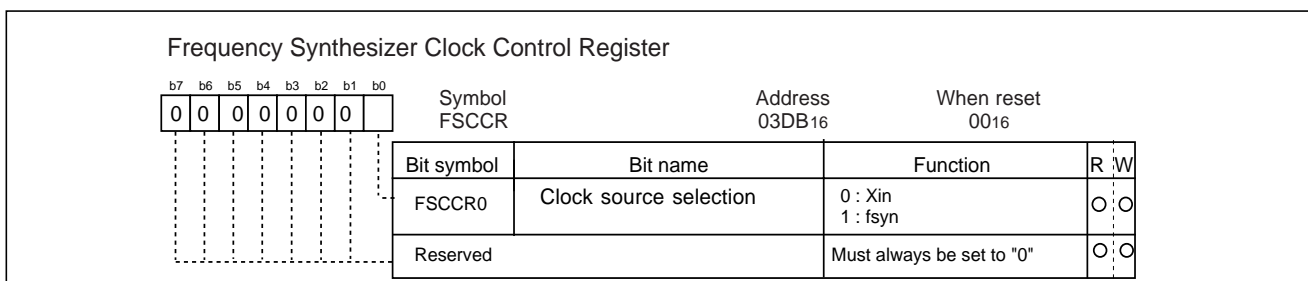


Figure 1.28: Frequency Synthesizer Clock Control Register (FSCCR)



2.18 Universal Serial Bus

The Universal Serial Bus (USB) has the following features:

- Complete USB Specification (version 1.1) Compatibility
- Error-handling capabilities
- FIFOs:
 - Endpoint 0: IN/OUT 32-byte
 - Endpoint 1: IN 128-byte OUT 128-byte
 - Endpoint 2: IN 32-byte OUT 32-byte
 - Endpoint 3: IN 32-byte OUT 32-byte
 - Endpoint 4: IN 32-byte OUT 32-byte
- Nine endpoints - control endpoint (Endpoint 0 - bi-directional) plus four IN and four OUT endpoints
- Complete device configuration
- Support of all device commands
- Supports of full-speed functions
- Support of all USB transfer types:
 - Isochronous
 - Bulk
 - Control
 - Interrupt
- Suspend/Resume operation
- On-chip USB transceiver with voltage converter
- Start-of-frame interrupt and output pin

2.18.1 USB Function Control Unit (USB FCU)

The implementation of the USB by this device is accomplished chiefly through the device's USB Function Control Unit (See Figure 1.29). The Function Control Unit's overall purpose is to handle the USB packet protocol layer. The Function Control Unit notifies the MCU that a valid token has been received. When this occurs, the data portion of the token is routed to the appropriate FIFO. The MCU transfers the data to, or from, the host by interacting with that endpoint's FIFO and CSR register.

The USB Function Control Unit is composed of five sections:

- Serial Interface Engine (SIE)
- Generic Function Interface (GFI)
- Serial Engine Interface Unit (SIU)
- Microcontroller Interface (MCI)
- USB Transceiver

2.18.1.1 Serial Interface Engine

The SIE interfaces to the USB serial data and handles deserialization/serialization of data, NRZI encoding decoding, clock extraction, CRC generation and checking, bit stuffing, and other items pertaining to the USB protocol such as handling inter-packet time-outs and packet ID (PID) decoding.

Universal Serial Bus

2.18.1.2 Generic Function Interface

The GFI handles all USB standard requests from the host through the control endpoint (endpoint zero), handles Bulk, Isochronous and Interrupt transfers through endpoints 1-4. The GFI handles read pointer reversal for re-transmission the current data set; write pointer reversal for reception of the last data set again and data toggle synchronization.

2.18.1.3 Serial Engine Interface Unit

The SIU block decodes the Address and Endpoint fields from the USB host.

2.18.1.4 Microcontroller Interface

The MCI block handles the Microcontroller interface and performs address decoding and synchronization of control signals.

2.18.1.5 USB Transceiver

The USB transceiver, designed to interface with the physical layer of the USB, is compliant with the USB Specification (version 1.1) for full-speed devices. It consists of two 6-ohm drivers, a receiver, and Schmitt triggers for single-ended receive signals.

The transceiver also includes a voltage converter. The voltage converter can supply 3.0 - 3.6V to the transmitter when the rest of the chip (CPU, USB FCU) operates at 4.15 - 5.25V. To enable the voltage converter, set bit 4 of the USB Control Register (USBC) to a "1". To disable the voltage converter, set bit 4 of the USBC to a "0". Refer to Section 5.4 "USB Transceiver" for more detailed information.

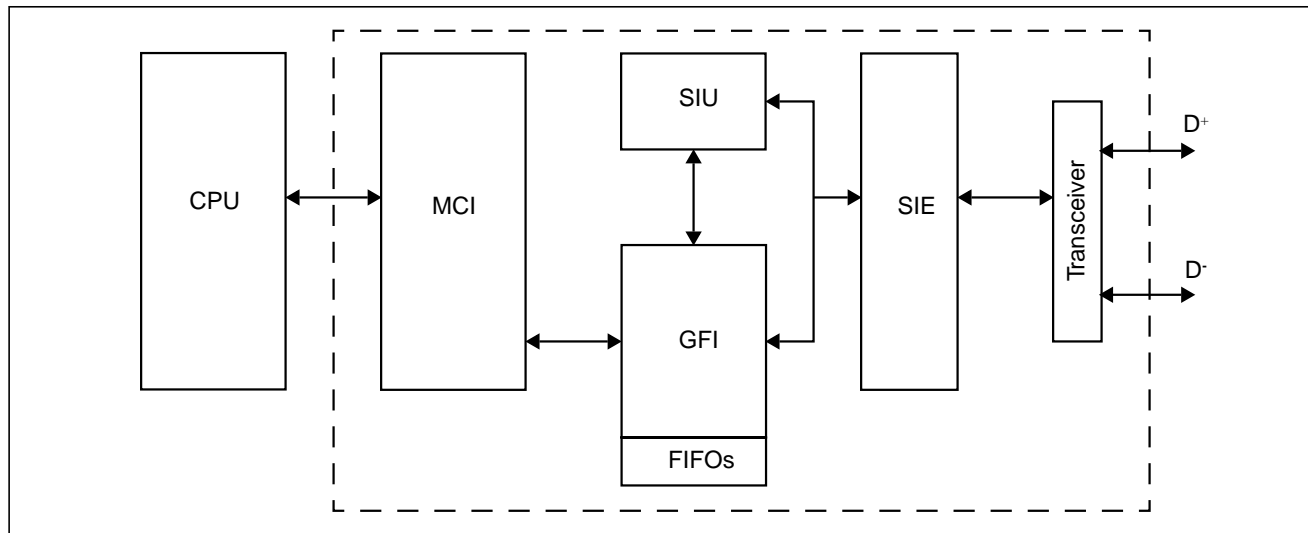


Figure 1.29: USB Function Control Unit Block Diagram

2.18.2 USB Interrupts

There are five USB interrupts in this device:

- USB Function interrupt
- USB Reset interrupt
- USB Suspend interrupt
- USB Resume interrupt
- USB Start-of-Frame (SOF) interrupt.

The first four interrupts are used to control the data flow and USB power. The SOF interrupt is used to monitor the transfer of isochronous (ISO) data. Each of the five USB interrupts is enabled by setting the corresponding bit in the Interrupt Control Register of the Interrupt Control Unit. Because the USB Function Interrupt has multiple interrupt sources, another level of enabling is within the USB Interrupt Registers 1 & 2.



Universal Serial Bus

2.18.2.1 USB Function Interrupt

The USB Function Interrupt can be triggered by 10 sources; many of these may be caused by several different events. Interrupt status flags associated with each source are contained in USBIS1 and USBIS2.

Endpoints 1-4 have two interrupt status flags associated with it to control data transfer or to report a STALL/ UNDER_RUN/OVER RUN condition.

The USB Endpoint x Out Interrupt Status Flag is set when

- USB FCU successfully receives a packet of data OR
- USB FCU sets the FORCE_STALL bit or OVER_RUN bit of the Endpoint x OUT CSR.

The USB Endpoint x In Interrupt Status is set when

- USB FCU successfully sends a packet of data OR
- USB FCU sets the UNDER_RUN bit of the Endpoint x IN CSR.

The USB Endpoint 0 (control endpoint) has one interrupt status bit associated with it to control data transfer or report a STALL condition.

The USB Endpoint 0 Interrupt Status Flag is set when

- USB FCU successfully receives/sends a packet of data
- Sets the SETUP_END bit or the FORCE_STALL bit, OR clears the DATA_END bit in the Endpoint 0 IN CSR.

The Overrun/Underrun Interrupt Status Flag is set when (applicable to endpoints used for isochronous data transfer)

- Overrun condition occurs in an endpoint (CPU is too slow to unload the data from the FIFO), OR
- Underrun condition occurs in an endpoint (CPU is too slow to load the data to the FIFO).

Each endpoint interrupt and overrun/underrun interrupt is enabled by setting the corresponding bit in the USB Interrupt Enable Register 1 and 2.

2.18.2.2 USB Reset Interrupt

The USB Reset Interrupt Status Flag is set when the USB FCU sees a SE0 present on D+/D- for at least 2.5 μ s. When this bit is set, all USB internal registers except INTST13 (bit5 of USBIS2) are reset to their default values. INTST13, the USB reset Interrupt Status Flag, is set to a "1" when the USB Reset is detected.

When the CPU recognizes a USB Reset Interrupt, it needs to re-initialize the USB FCU so that the USB operation can behave properly. It must also clear INTST13 by writing a "1" to this bit to allow a USB Reset Interrupt request to occur the next time a USB Reset is detected.

Register RSTIC contains the USB Reset Interrupt's request bit and its interrupt priority select bits which are used to enable the interrupt and set its software priority level.

2.18.2.3 USB Suspend and Resume Interrupts

The USB Suspend Interrupt is set when the USB FCU does not detect any bus activity on D+/D- (in J-state) for at least 3ms.

The USB Suspend Signaling Interrupt Status Flag (INTST15, bit 7 of USBIS2) is set to a "1" when the USB Suspend is detected. The CPU must clear INTST15 by writing a "1" to this bit to allow a USB Suspend Interrupt request to occur the next time a USB Suspend is detected.

The USB Resume Signaling Interrupt Status Flag is set when a USB FCU is in the suspend state and detects non-idle signaling on the D+/D-.

Register SUSPIC contains the USB Suspend Interrupt's request bit and its interrupt priority select bits which are used to enable the interrupt and set its software priority level.

The USB Resume Interrupt request is set when the USB FCU is in the suspend state and detects non-idle signaling on D+/D-.

The USB Signaling Interrupt Status Flag (INTST14, bit 6 of USBIS2) is set to a "1" when the USB Resume is detected. The CPU must clear INTST14 by writing a "1" to this bit to allow a USB Resume Interrupt request to occur the next time a USB Resume is detected.

Register RSMIC contains the USB Resume Interrupt's request bit and its interrupt priority select bits, which are used to enable the interrupt and set its software priority level.



2.18.2.4 USB SOF Interrupt

The USB SOF (Start-Of-Frame) Interrupt is used to control the transfer of isochronous data. The USB FCU generates a USB SOF Interrupt request when a start-of-frame packet is received.

Register SOFIC contains the USB SOF Interrupt's request bit and its interrupt priority select bits, which are used to enable the interrupt and set its software priority level.

2.18.3 USB Endpoint FIFOs

The USB FCU has an IN (transmit) FIFO and an OUT (receive) FIFO for each endpoint. Each endpoint (except endpoint 0) can be configured to support either single packet mode (in which only a single data packet is allowed to reside in the endpoint's FIFO) or dual packet mode (in which up to two data packets are allowed to reside in the endpoint's FIFO). Dual packet mode provides support for back-to-back transmission or back-to-back reception. The mode is automatically determined by the MAXP value. When $MAXP > 1/2$ of the endpoint's FIFO size, single packet mode is set. When $MAXP \leq 1/2$ of the endpoint's FIFO size, dual packet mode is set.

In the event of a bad transmission/reception, the USB FCU handles all the FIFO read/write pointer reversal and data set management tasks required.

Throughout this specification, the terms "IN FIFO" and "OUT FIFO" usually refer to the FIFOs associated with a specific endpoint.

2.18.3.1 IN (Transmit) FIFOs

The CPU/DMA writes data to the endpoint's IN FIFO location specified by the FIFO write pointer, which automatically increments by "1" after a write. The CPU/DMA should only write data to the IN FIFO when the IN_PKT_RDY bit of the associated IN CSR is a "0".

- **Endpoint 0 IN FIFO Operation:**

The CPU writes a "1" to the IN_PKT_RDY bit of Endpoint 0 CSR after it finishes writing a packet of data to the IN FIFO. The USB FCU clears the IN_PKT_RDY bit after the packet has been successfully transmitted to the host (i.e., ACK is received from the host) or the SETUP_END bit of the IN CSR is set to a "1".

- **Endpoint 1-4 IN FIFO Operation when AUTO_SET (bit 7 of Endpoint x IN CSR) = "0" (disabled):**

MAXP > 1/2 of the IN FIFO size: The CPU writes a "1" to the IN_PKT_RDY bit of the associated IN CSR after the CPU/DMAC finishes writing a packet of data to the IN FIFO. The USB FCU clears the IN_PKT_RDY bit after the packet has been successfully transmitted to the host (which is assumed for isochronous transfers and is concluded when an ACK is received from the host for non-isochronous transfers).

MAXP ≤ 1/2 of the IN FIFO size: The CPU writes a "1" to the IN_PKT_RDY bit of the associated IN CSR after the CPU/DMAC finishes writing a packet of data to the IN FIFO. The USB FCU clears the IN_PKT_RDY bit as soon as the IN FIFO is ready to accept another data packet. (The FIFO can hold up to two data packets at the same time in this configuration for back-to-back transmission.)

- **Endpoint 1-4 IN FIFO Operation when AUTO_SET (bit 7 of Endpoint x IN CSR) = "1" (enabled):**

MAXP > 1/2 of the IN FIFO size: When the number of bytes of data equal to the MAXP (maximum packet size) has been written to the IN FIFO by the CPU/DMAC, the USB FCU sets the IN_PKT_RDY bit of the associated IN CSR to a "1" automatically. The USB FCU clears the IN_PKT_RDY bit after the packet has been successfully transmitted to the host (which is assumed for isochronous transfers and is concluded when an ACK is received from the host for non-isochronous transfers).

MAXP ≤ 1/2 of the IN FIFO size: When the number of bytes of data equal to the MAXP (maximum packet size) has been written to the IN FIFO by the CPU/DMAC, the USB FCU sets the IN_PKT_RDY bit to a "1" automatically. The USB FCU clears the IN_PKT_RDY bit as soon as the IN FIFO is ready to accept another data packet. (The FIFO can hold up to two data packets at the same time in this configuration for back-to-back transmission.)

A software or a hardware flush causes the USB FCU to act as if a packet has been successfully transmitted out to the host. When there is one packet in the IN FIFO, a flush causes the IN FIFO to be empty. When there are two packets in the IN FIFO, a flush causes the older packet to be flushed out from the IN FIFO. A flush also updates the IN FIFO status bits IN_PKT_RDY and TX_NOT_EMPTY of the associated IN CSR.

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The status of endpoint 1-4 IN FIFOs for both of the above cases can be obtained from the IN CSR of the corresponding IN FIFO as shown in Table 1.13 .

Table 1.13: TA FIFO Status

IN_PKT_RDY	TX_NOT_EMPTY	IN FIFO Status
0	0	No data packet in IN FIFO
0	1	One data packet in IN FIFO if MAXP <= 1/2 of the FIFO size./ Invalid when MAXP > 1/2 of the FIFO size
1	0	Invalid
1	1	Two data packets in IN FIFO when MAXP <= 1/2 of the FIFO size One data packet in IN FIFO when MAXP > 1/2 of the FIFO size

2.18.3.2 Out (Receive) FIFOs

The USB FCU writes data to the endpoint's OUT FIFO location specified by the FIFO write pointer, which automatically increments by one after a write. When the USB FCU has successfully received a data packet, it sets the OUT_PKT_RDY bit of the corresponding OUT CSR to a "1". The CPU/DMAC should only read data from the OUT FIFO when the OUT_PKT_RDY bit of the OUT CSR is a "1".

• **Endpoint 0 OUT FIFO Operation:**

The USB FCU sets the OUT_PKT_RDY bit to a "1" after it has successfully received a packet of data from the host. The CPU sets bit SERVICED_OUT_PKT_RDY to a "1" to clear the OUT_PKT_RDY bit after the packet of data has been unloaded from the OUT FIFO by the CPU.

• **Endpoint 1-4 OUT FIFO Operation when AUTO_CLR (bit 7 of Endpoint x OUT CSR) = "0" (disabled):**

MAXP > 1/2 of the OUT FIFO size: The USB FCU sets the OUT_PKT_RDY bit of the associated IN CSR to a "1" after it has successfully received a packet of data from the host. The CPU writes a "0" to the OUT_PKT_RDY bit after the packet of data has been unloaded from the OUT FIFO by the CPU/DMAC.

MAXP <= 1/2 of the OUT FIFO size: The USB FCU sets the OUT_PKT_RDY bit of the associated IN CSR to a "1" after it has successfully received a packet of data from the host. The CPU writes a "0" to the OUT_PKT_RDY bit after the packet of data has been unloaded from the OUT FIFO by the CPU/DMAC. If another packet is in the OUT FIFO, the OUT_PKT_RDY bit will be set to a "1" again almost immediately (such that it may appear that the OUT_PKT_RDY bit remains a "1"). In this configuration, the FIFO can store up to two data packets at the same time for back-to-back reception.

• **Endpoint 1-4 OUT FIFO Operation when AUTO_CLR (bit 7 of Endpoint x OUT CSR) = "1" (enabled):**

MAXP > 1/2 of the OUT FIFO size: The USB FCU sets the OUT_PKT_RDY bit of the associated IN CSR to a "1" after it has successfully received a packet of data from the host. The USB FCU clears the OUT_PKT_RDY bit to a "0" automatically when the number of bytes of data equal to the MAXP (maximum packet size) has been unloaded from the OUT FIFO by the CPU/DMAC.

MAXP <= 1/2 of the OUT FIFO size: The USB FCU sets the OUT_PKT_RDY bit of the associated IN CSR to a "1" after it has successfully received a packet of data from the host. The USB FCU clears the OUT_PKT_RDY bit to a "0" automatically when the number of bytes of data equal to the MAXP (maximum packet size) has been unloaded from the OUT FIFO by the CPU/DMAC. If another packet is in the OUT FIFO, the OUT_PKT_RDY bit will be set to a "1" again almost immediately (such that it may appear that the OUT_PKT_RDY bit remains a "1"). In this configuration, the FIFO can store up to two data packets at the same time for back-to-back reception.

A software flush causes the USB FCU to act as if a packet has been unloaded from the OUT FIFO. If there is one packet in the OUT FIFO, a flush will cause the OUT FIFO to be empty. If there are two packets in the OUT FIFO, a flush will cause the older packet to be flushed out from the OUT FIFO.

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2.18.3.3 Interrupt Endpoints:

Any endpoint can be used for interrupt transfers. For normal interrupt transfers, the interrupt transactions behave the same as bulk transactions, i.e., no special setting is required. The IN endpoints may also be used to communicate rate feedback information for certain types of isochronous functions. This is done by setting the INTPT bit in the IN CSR register of the corresponding endpoint.

The following outlines the operation sequence for an IN endpoint used to communicate rate feedback information:

1. Set MAXP > 1/2 of the endpoint's FIFO size;
2. Set INTPT bit of the IN CSR;
3. Flush the old data in the FIFO;
4. Load interrupt status information and set IN_PKT_RDY bit in the IN CSR;
5. Repeat steps 3 & 4 for all subsequent interrupt status updates.

2.18.4 USB Special Function Registers

The MCU controls USB operation through the use of special function registers (SFR). This section describes each USB related SFR. Some USB special function registers have a mix of read/write, read only, and write only register bits. Additionally, the bits may be configured to allow the user to write only a "0" or a "1" to individual bits.

- When accessing these registers, writing a "0" to a register that can only be set to a "1" by the CPU has no effect on that register bit.
- Writing a "1" to a register that can only be set to a "0" by the CPU has not effect on that register bit.

Each figure and description of the special function registers details this operation.

All USB Special Function Registers, with the exception of USB Attach/Detach (001F₁₆) and USB control (000C₁₆) must use byte access. Work access is prohibited for USB internal registers (0300₁₆ - 033C₁₆).

The contents of all USB Special Functions Registers, including USB Attach/Detach and USB Control, are preserved on a software reset.

2.18.4.1 USB Attach/Detach Register

The USB Attach / Detach Register is shown in Figure 1.30. The register is used to attach and detach the USB function from a USB host without physically disconnecting the USB cable. This functionality is enabled by setting P83_SECOND to a "1". Doing this forces P83 to operate as a pull-up for D+ (through an external 1.5k ohm resistor). The port driver is tri-stated and a "1" is always read from the port bit in this mode. When the ATTACH/DETACH bit is a "1" (and P83_SECOND is a "1"), P83 is driven with the voltage on EXTCAP, causing D+ to be pulled up and the host to detect an attach. When the ATTACH/DETACH bit is a "0" (and P83_SECOND is a "1"), P83 is tri-stated, causing D+ to be pulled down (through the cable and 15k ohm resistor on the host/hub side) and a detach to be registered by the host. A 1.5k ohm pull-up resistor must be connected externally from P83 to D+ when this functionality is used. When it is not used, the 1.5k ohm resistor should be placed between EXTCAP and D+.

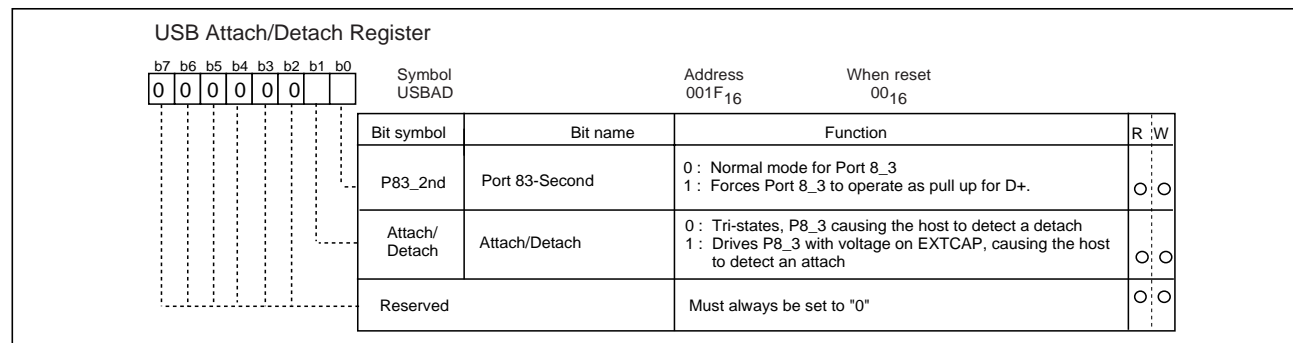


Figure 1.30: USB Attach/Detach Register

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2.18.4.2 USB Control Register

The USB Control Register, shown in Figure 1.31, is used to control the USB FCU. This register is not reset by a USB reset signaling. After the USB is enabled (USBC7 set to "1"), a minimum delay of 250ns (three 12 MHz clock periods) is needed before performing any other USB register read/write operations.

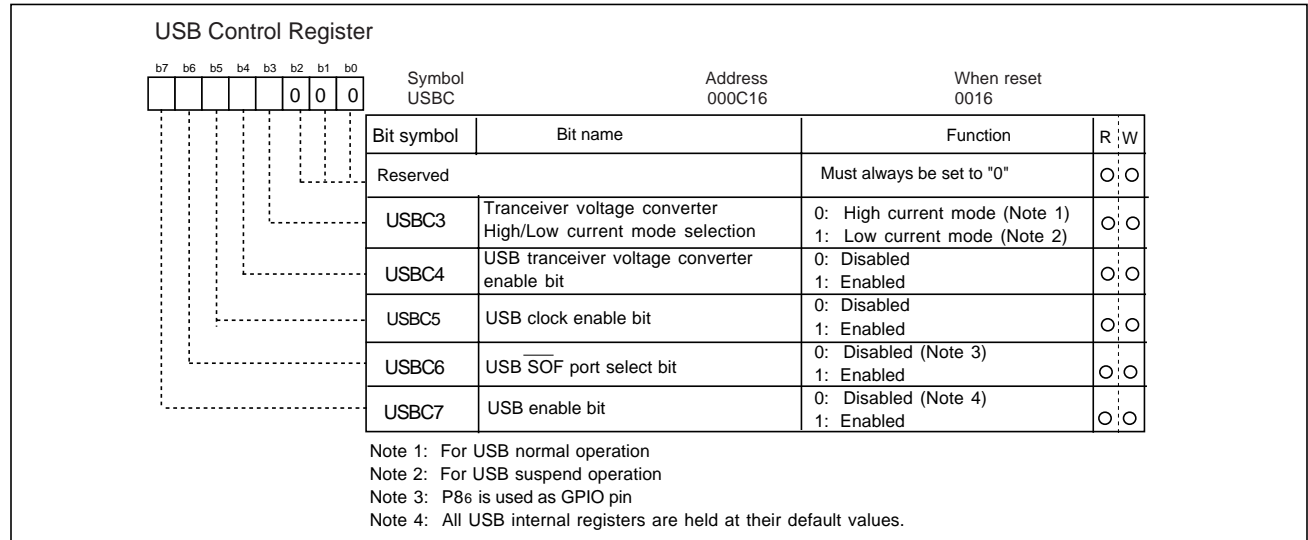


Figure 1.31: USB Control Register

2.18.4.3 USB Function Address Register

The USB Function Address Register, shown in Figure 1.32, maintains the 7-bit USB address assigned by the host. The USB FCU uses this register value to decode USB token packet addresses. At reset, when the device is not yet configured, the value is 00 $_{16}$. For the procedures on how to update this register, refer to Application Notes USB Consecutive Set Address.

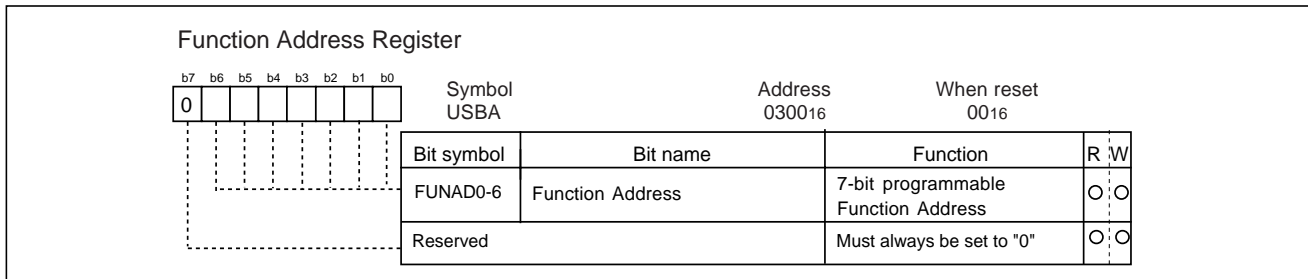


Figure 1.32: USB Function Address Register

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2.18.4.4 The USB Power Management Register

The USB Power Management Register, shown in Figure 1.33, is used for power management in the USB FCU.

• **SUSPEND Detection Flag:**

When the USB FCU does not detect any bus activity on D+/D- for at least 3ms (and D+/D- are in the J-state), it sets the Suspend Detection Flag and generates an interrupt. This bit is cleared when signaling from the host is detected on D+/D- (which sets the Resume Detection Flag and generates an interrupt), or the Remote Wake-up Bit is set and then cleared by the CPU. If the USB clock was disabled during the suspend state, the SUSPEND Detection Flag is not cleared until after the USB clock is re-enabled.

• **RESUME Detection Flag:**

When the USB FCU is in the suspend state and detects activity on D+/D- from the host, it sets the Resume Detection Flag and generates an interrupt. The CPU writes a "1" to INTST14 (bit 6 of USB Interrupt Status Register 2) to clear this flag.

• **WAKEUP Control Bit:**

The CPU writes a "1" to the WAKEUP Control Bit for remote wake-up. While this bit is set and the USB FCU is in suspend mode, resume signaling is sent to the host. The CPU must keep this bit set for a minimum of 10ms and a maximum of 15ms before writing a "0" to this bit.

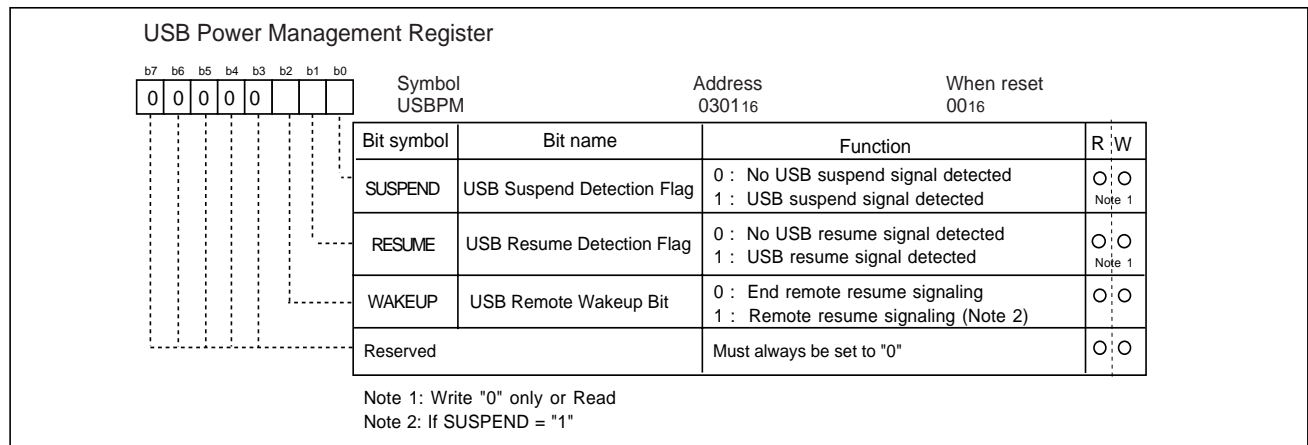


Figure 1.33: USB Power Management Register

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2.18.4.5 USB Interrupt Status Registers 1 and 2

USB Interrupt Status Registers 1 and 2, shown in Figure 1.34 and Figure 1.35, are used to indicate the condition that caused a USB function interrupt and USB Reset, Suspend and Resume Interrupts to the CPU. A "1" indicates the corresponding condition caused an interrupt. The USB Interrupt Status Register bits can be cleared by writing a "1" to the corresponding bit.

INTST0 is set to a "1" by the USB FCU when (in Endpoint 0 CSR):

- A packet of data is successfully received (EP0CSR0 - OUT_PKT_RDY is set by the USB FCU)
- A packet of data is successfully sent (EP0CSR - IN_PKT_RDY is cleared by the USB FCU)
- EP0CSR3 (DATA_END) bit is cleared by the USB FCU
- EP0CSR4 (FORCE_STALL) bit is set by the USB FCU
- EP0CSR5 (SETUP_END) bit is set by the USB FCU

INTST2, INTST4, INTST6 or INTST8 is set to a "1" by the USB FCU when (in Endpoint x IN CSR):

- A packet of data is successfully sent (INXCSR0 - IN_PKT_RDY is cleared by the USB FCU)
- INXCSR1 (UNDER_RUN) bit is set by the USB FCU

INTST3, INTST5, INTST7 or INTST9 is set to a "1" by the USB FCU when (in Endpoint xOUT CSR):

- A packet of data is successfully received (OUTXCSR0 - OUT_PKT_RDY is set by the USB FCU)
- OUTXCSR1 (OVER_RUN) bit is set by the USB FCU
- OUTXCSR4 (FORCE_STALL) bit is set by the USB FCU

INTST12 is set to a "1" by the USB FCU when an overrun or underrun condition occurs in any of the endpoints.

INTST13 is set to a "1" by the USB FCU when a USB reset signaling from the host is received. All internal register bits except this bit are reset to their default values when the USB reset is received.

INTST14 is set to a "1" by the USB FCU when the USB FCU is in the suspend state and non-idle signaling is received from D+/D-.

INTST15 is set to a "1" by the USB FCU when D+/D- are in the idle state for more than 3ms.

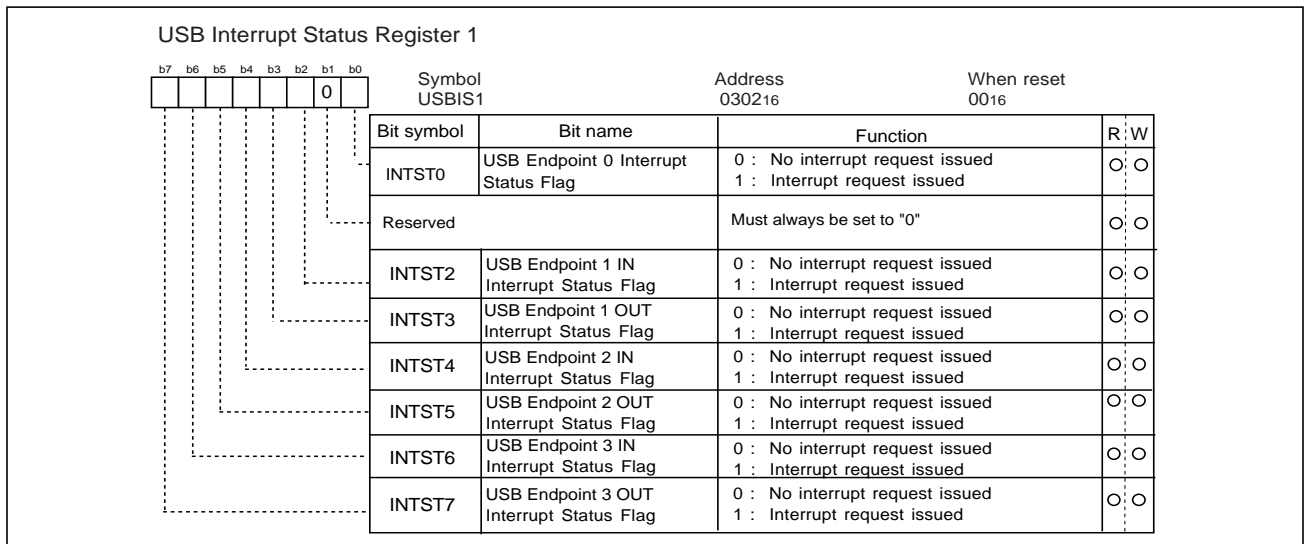


Figure 1.34: USB Interrupt Status Register 1

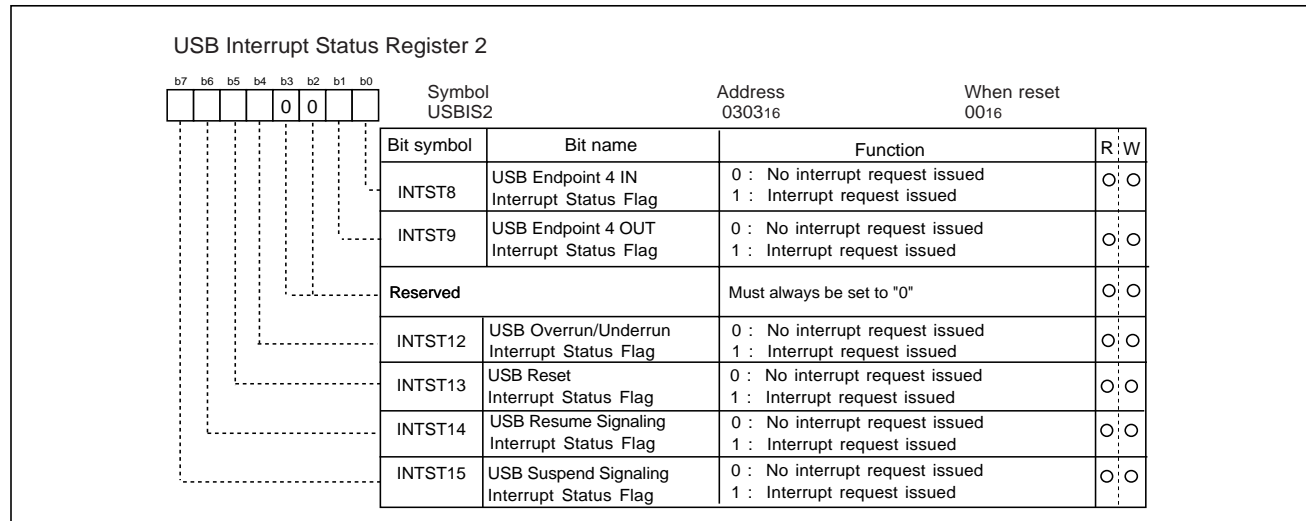


Figure 1.35: USB Interrupt Status Register 2

2.18.4.6 Clearing of the USB Interrupt Status Registers

The USB Interrupt Status Register 1 and 2 are used to indicate pending interrupts for a given source. The USB FCU sets the interrupt status bits. The CPU writes a "1" to each status bit to clear it.

Because the USB Function Interrupt has multiple sources that can generate an interrupt, it is recommended that the user first read the two status registers and store them in variables then write back the same value for clearing all the existing interrupts that were pending when the status registers were read. This procedure prevents any interrupt that occurs after the status registers are read from being cleared by the 'write-back' operation. The CPU must read, then write both status registers, writing to status register 1 first and status register 2 second to guarantee proper operation. The upper three bits of the value written back to USBIS2 should always be "000" to prevent any of the USB Reset, Suspend and Resume Status Flags from being cleared.

The USB Reset, Suspend and Resume Status Flags are contained in USBIS2 along with the USB Endpoint 4 In/Out Interrupt Status Flags and the USB Overrun/Underrun Interrupts Status Flag. Because the flags are not all sources for the same interrupt, use caution when clearing one or more of the flags to avoid inadvertently clearing other flags. The Reset, Suspend and Resume Status Flags should be cleared individually by writing a byte value with a "1" only at the position corresponding to the flag to be cleared. The USB Endpoint 4 In/Out Interrupt status Flags and the USB Overrun/Underrun Interrupt Status Flag should be cleared as described in the preceding paragraph because they are sourced for the USB Function Interrupt.

"Read-modify-write" instructions, such as "BCLR" and "BSET", should not be used to clear any of the interrupt status bits in USBIS1 or USBIS2. Using these instructions could cause pending interrupts to be cleared without the firmware's knowledge.

2.18.4.7 The USB Function Interrupt Enable Registers 1 and 2

The USB Function Interrupt Enable Registers 1 and 2, shown in Figure 1.36 and Figure 1.37, are used to enable the corresponding interrupt status conditions that can generate a USB Function Interrupt. When the bit to a corresponding interrupt condition is "0", that condition does not generate a USB function interrupt. When the bit is a "1", that condition can generate a USB function interrupt. At reset, all USB function interrupt status conditions are enabled.

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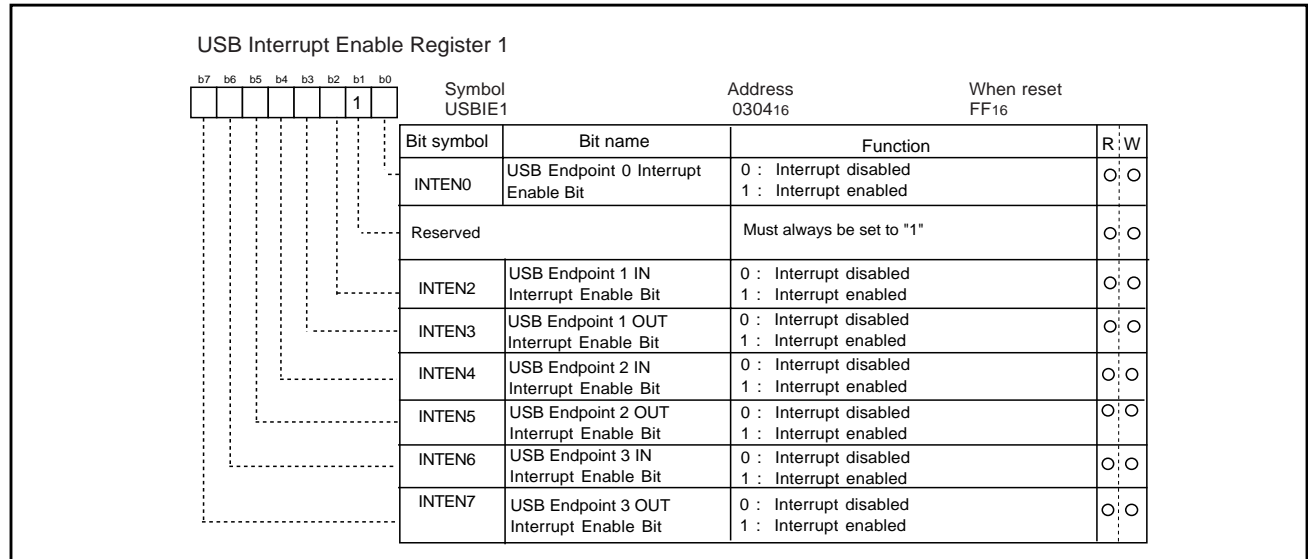


Figure 1.36: USB Interrupt Enable Register 1

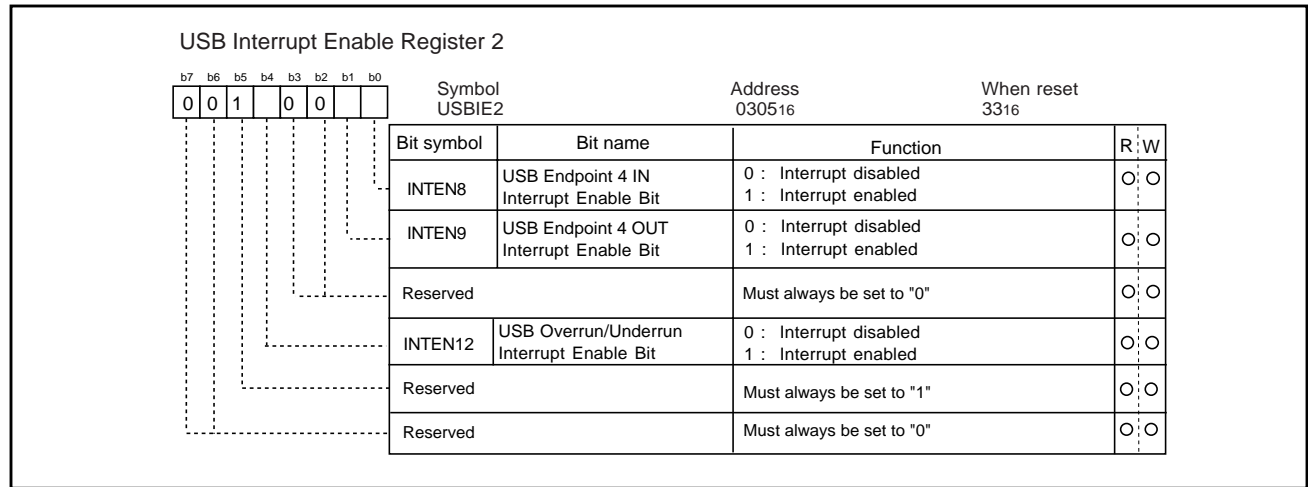


Figure 1.37: USB Interrupt Enable Register 2

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2.18.4.8 USB Frame Number Registers

The USB Frame Number Low Register, shown in Figure 1.38, contains the lower 8 bits of the 11-bit frame number received from the host. The USB Frame Number High Register, shown in Figure 1.39 contains the upper 3 bits of the 11-bit frame number received from the host.

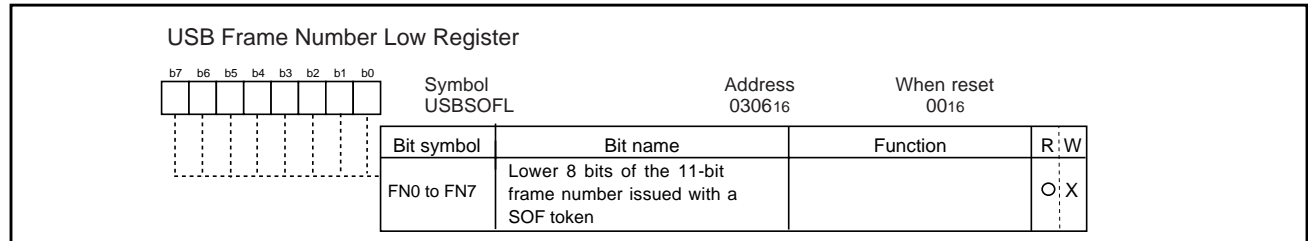


Figure 1.38: USB Frame Number Low Register

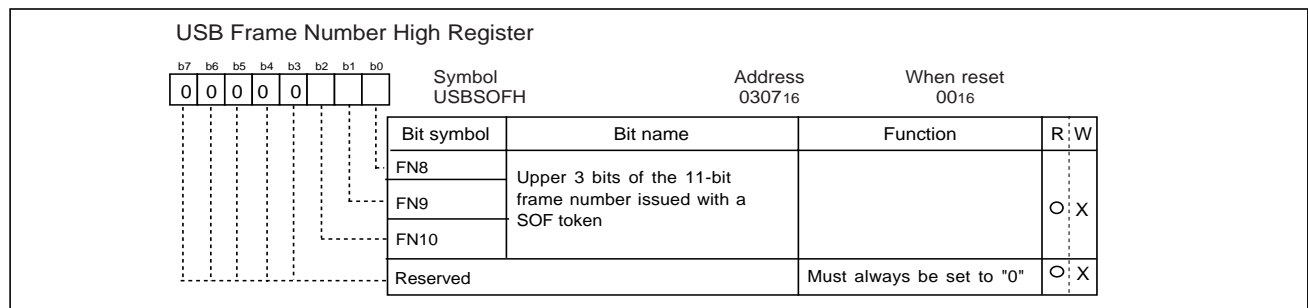


Figure 1.39: USB Frame Number High Register

2.18.4.9 USB ISO Control Register

The USB ISO Control Register, shown in Figure 1.40, contains two global bits, ISO_UPD and AUTO_FL for controlling endpoints 1-4 isochronous data transfer.

When ISO_UPD = "0", a data packet in an endpoint's IN FIFO is always 'ready to transmit' upon receiving the next IN_TOKEN from the host (with matched address and endpoint number) if the endpoint's IN_PKT_RDY is set.

When ISO_UPD = "1" and the ISO/TOGGLE_INIT bit of the corresponding endpoint's IN CSR is set, the internal 'ready to transmit' signal to the transmit control logic is not activated when the endpoint's IN_PKT_RDY is set. Instead, it is activated when the next SOF is received, this way, the data loaded in frame n is transmitted out in frame n+1. The ISO_UPD bit is a global bit for endpoints 1-4 and works with isochronous pipes only.

When AUTO_FL = "1", ISO_UPD = "1", a particular IN endpoint's ISO/TOGGLE_INIT bit is set, and the IN endpoint's IN_PKT_RDY = "1", the USB FCU detects a SOF packet and the USB FCU automatically flushes the oldest packet from the IN FIFO. In this case, IN_PKT_RDY = "1", indicates that two data packets are in the IN FIFO. Because double buffering is a requirement for ISO transfer, MAXP must be set to less than or equal to 1/2 of the FIFO size.

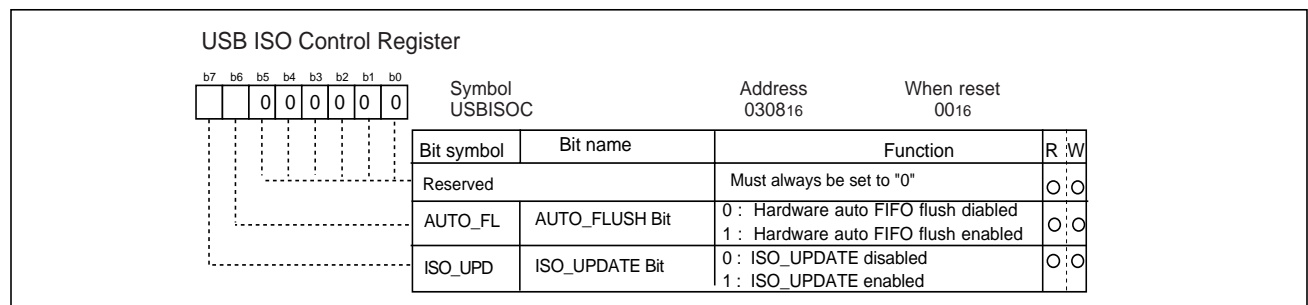


Figure 1.40: USB ISO Control Register

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2.18.4.10 USB DMAx Request Registers

The USB DMAx Request Registers, shown in Figure 1.41 and Figure 1.42, are used to select which USB Endpoint x FIFO read/write requests are selected as the DMAC channel 0 or channel 1 request source. The USB DMA0 (DMA1) Request Register should have only one bit set at any given time. When multiple bits are set, no request is selected.

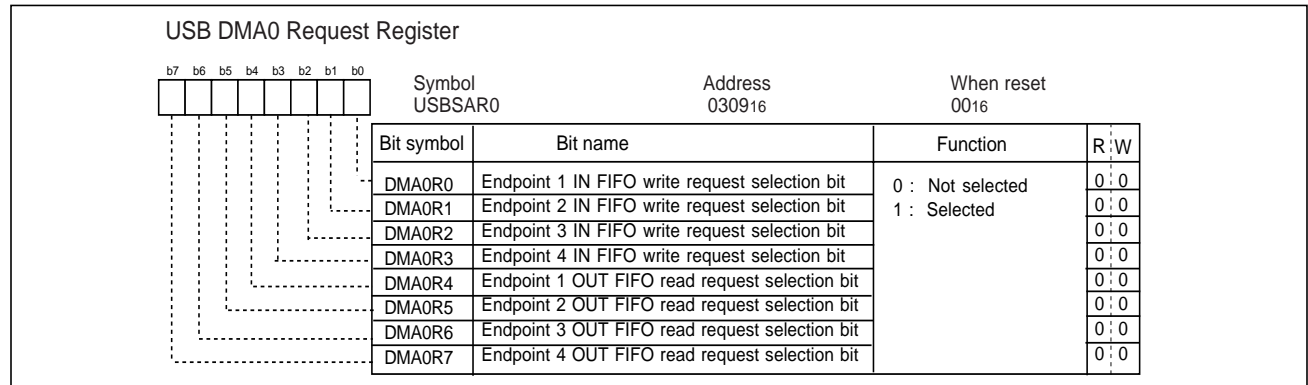


Figure 1.41: USB DMA0 Request Register

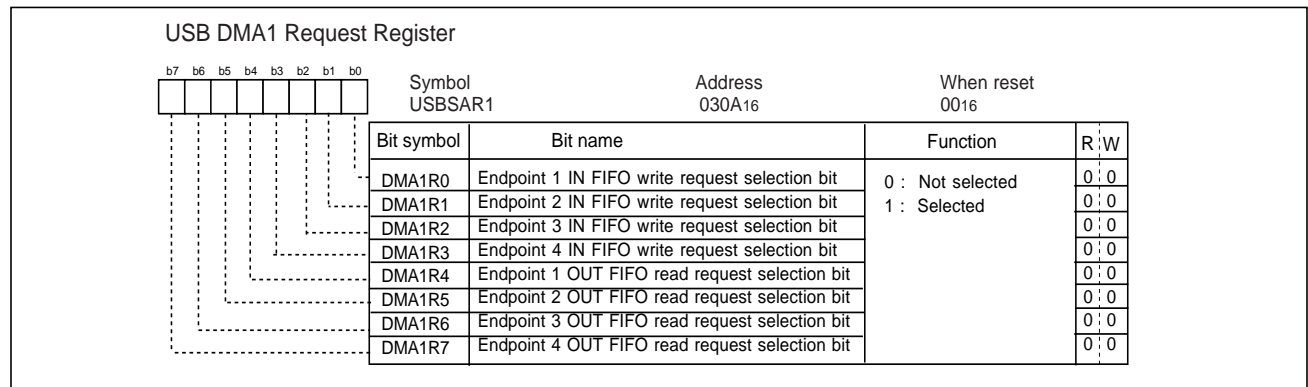


Figure 1.42: USB DMA1 Request Register

2.18.4.11 USB Endpoint Enable Register

The USB Endpoint Enable Register, shown in Figure 1.43, is used to enable/disable an individual endpoint. Endpoint 0 is always enabled and cannot be disabled by firmware. All endpoints are enabled after reset.

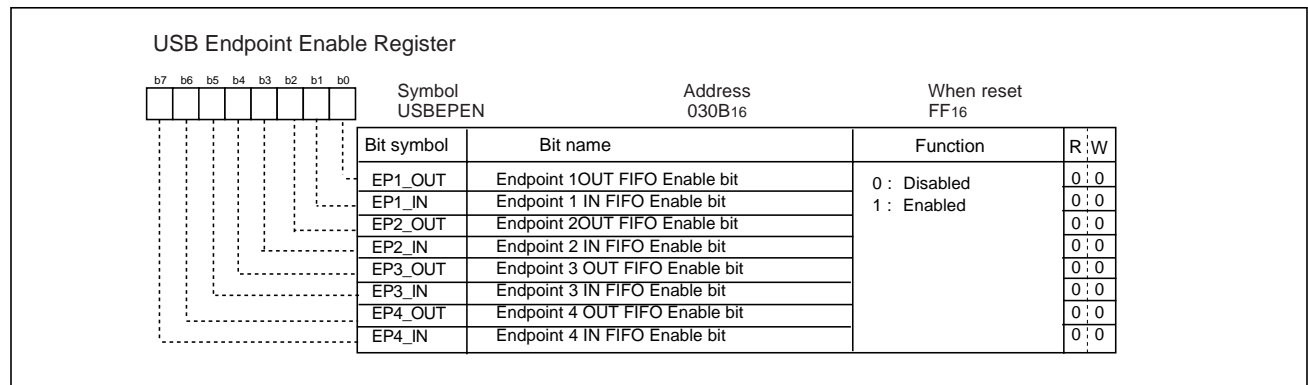


Figure 1.43: USB Endpoint Enable Register



2.18.4.12 Endpoint 0 CSR (Control and Status Register)

The Endpoint 0 CSR (Control and Status Register), shown in Figure 1.44 contains the control and status information of Endpoint 0.

• **EP0CSR0 (OUT_PKT_RDY):**

The USB FCU sets this bit to a “1” after it receives a valid SETUP/OUT token from the host. The CPU clears this bit after unloading the packet from the FIFO by writing a “1” to EP0CSR6. The CPU should not clear the OUT_PKT_RDY bit before it finishes decoding the host request. When EP0CSR2 (SEND_STALL) needs to be set (because the CPU decodes an invalid or unsupported request) a “1” should be written to EP0CSR6 and EP0CSR2 at the same time using the same instruction.

• **EP0CSR1 (IN_PKT_RDY):**

The CPU writes a “1” to this bit after it finishes writing a packet of data to the endpoint 0 FIFO. The USB FCU clears this bit after the packet is successfully transmitted to the host, or the EP0CSR5 (SETUP_END) bit is set.

• **EP0CSR2 (SEND_STALL):**

The CPU writes a “1” to this bit when it decodes an invalid or unsupported standard device request from the host. When the OUT-PKT_RDY bit is a “1” at the time the CPU wants to set the SEND_STALL bit to a “1”, the CPU must also set SERVICED_OUT_PKT_RDY to a “1” to clear the OUT-PKT_RDY at the same time as setting the SEND_STALL bit. The USB FCU returns a STALL handshake for all subsequent IN/OUT transactions (during control transfer data or status stages) while this bit is set. The CPU writes a “0” to clear it after it receives a new SETUP packet. It is up to the firmware to decide what SETUP packet should lead the clearing of the SEND_STALL bit.

• **EP0CSR3 (DATA_END):**

The CPU writes a “1” to this bit when it writes (IN data phase) or reads (OUT data phase) the last packet of data to or from the FIFO. The CPU sets this bit at the same time as it sets the last IN_PKT_RDY bit or sets the last SERVICED_OUT_PKT_RDY bit. This bit indicates to the USB FCU that the specific amount of data in the setup phase is transferred. The USB FCU advances to the status phase once this bit is set. When the status phase completes, the USB FCU clears this bit. When this bit is set to a “1”, and the host requests or sends more data, the USB FCU returns a STALL handshake and terminates the current control transfer.

• **EP0CSR4 (FORCE_STALL):**

The USB FCU sets this bit to a “1” to report an error status when one of the following occur:

- Host sends an IN token in the absence of a SETUP stage
- Host sends a bad data toggle in the STATUS stage, (i.e. DATA0 is used)
- Host sends a bad data toggle in the SETUP stage, (i.e. DATA1 is used)
- Host request more data than specified in the SETUP state, (i.e. IN token comes after DATA_END bit is set)
- Host sends more data than specified in the SETUP state, (i.e. OUT token comes after DATA_END bit is set)
- Host sends larger data packet than MAXP size

All of the conditions stated (except bad data toggle in the SETUP stage) cause the device to send a STALL handshake for the current IN/OUT transaction. For the bad data toggle in the SETUP state, the device sends ACK for the SETUP stage and then sends STALL for the next IN/OUT transaction. A STALL handshake caused by the above listed conditions lasts for one transaction and terminates the ongoing control transfer. Any packet after the STALL handshake will be seen as the beginning of a new control transfer.

The CPU writes a “0” to clear the FORCE_STALL status bit.

• **EP0CSR5 (SETUP_END):**

The USB FCU sets this bit to a “1” if a control transfer has ended before the specific length of data is transferred during the data phase (status phase starts before DATA_END bit is set) or a control transfer has ended before a new SETUP has arrived and before successfully completing the status phase. The CPU clears this bit by writing a “1” to IN0CSR7. Once the CPU detects the SETUP_END bit as set, it should stop accessing the FIFO to service the previous setup transaction. If the SETUP_END is caused by the reception of the SETUP packet prior to the end of the current control transfer, the OUT_PKT_RDY bit is set once the reception of the SETUP packet has completed (without errors). After the OUT_PKT_RDY bit is set, the new SETUP packet

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data will be in the FIFO. For this case, because the SETUP_END bit is set near the beginning of the packet when the SETUP PID is encountered and the OUT_PKT_RDY bit is set at the end of the packet, the value read from EP0IN_CSR in the USB functional interrupt routine may only show that the SETUP_END bit as "1" instead of both the SETUP_END and OUT_PKT_RDY bits.

• **EP0CSR6 and EP0CSR7:**

These bits are used to clear EP0CSR0 and EP0CSR5 respectively. Writing a "1" to these bits clears the corresponding register bit.

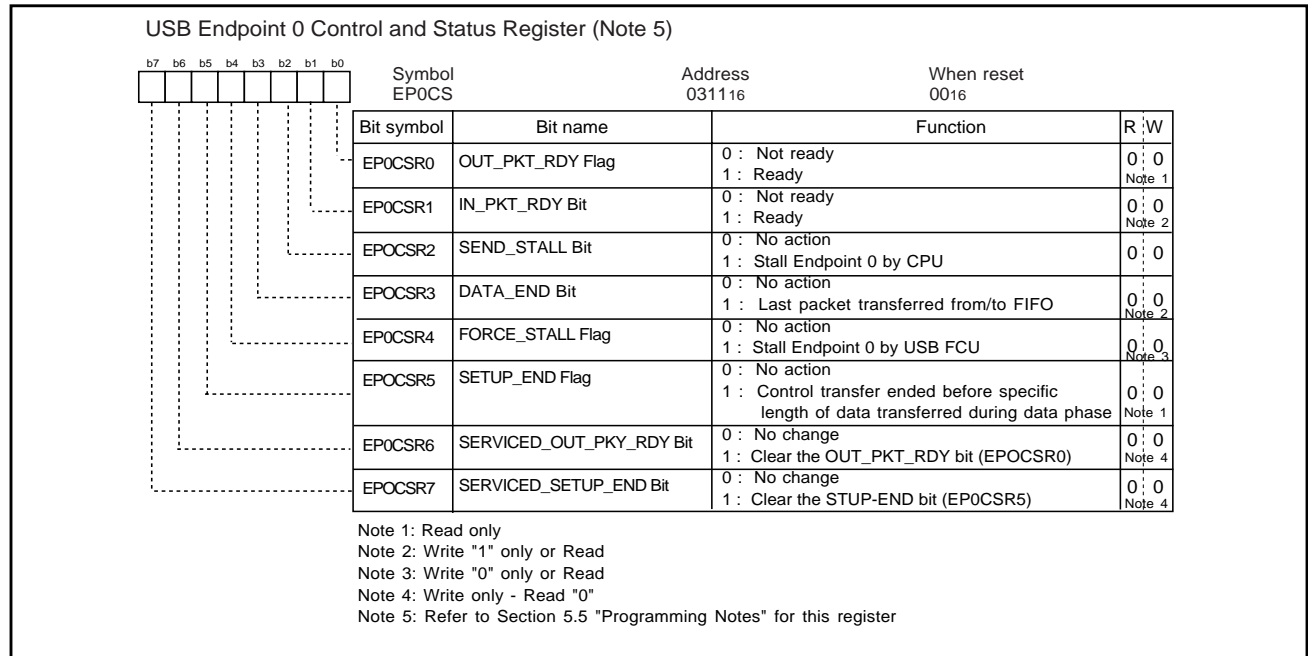


Figure 1.44: USB Endpoint 0 CSR

2.18.4.13 USB Endpoint 0 MAXP Register

The USB Endpoint 0 MAXP Register, shown in Figure 1.45, indicates the maximum packet size (MAXP) of Endpoint 0 IN/OUT packet. The default value for Endpoint 0 MAXP is 8 bytes.

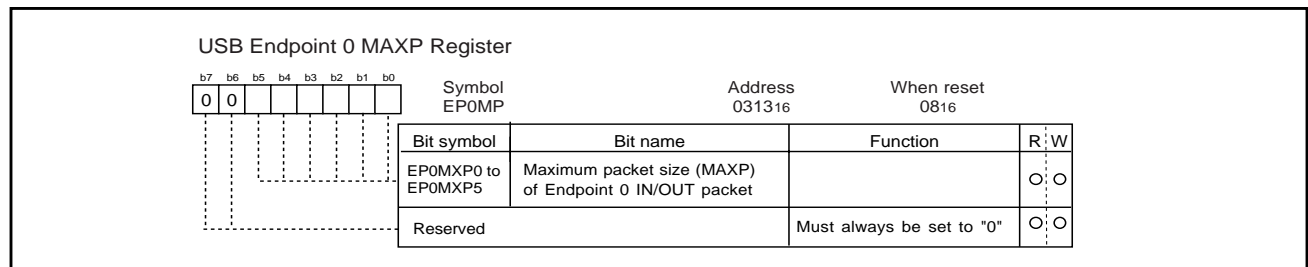


Figure 1.45: USB Endpoint 0 MAXP

2.18.4.14 USB Endpoint 0 OUT WRT CNT Register

The USB Endpoint 0 OUT WRT CNT Register, shown in Figure 1.46, contains the number of bytes of the current data set in the OUT FIFO. The USB FCU sets the value in the Write Count Register after having successfully received a packet of data from the host. The CPU reads the register to determine the number of bytes to be read from the FIFO.

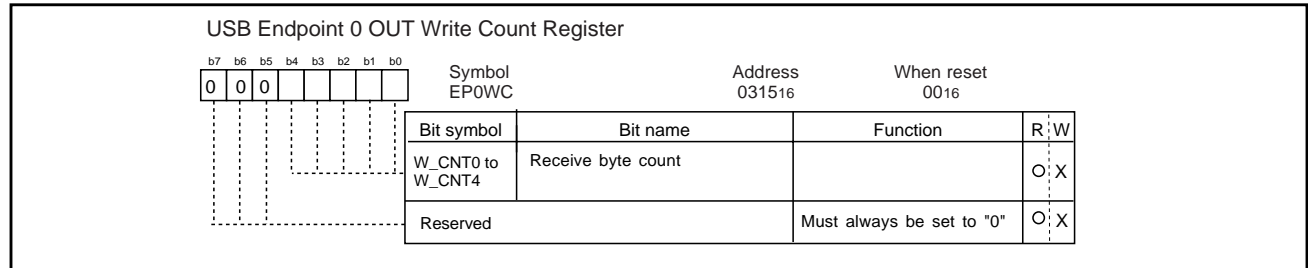


Figure 1.46: USB Endpoint 0 OUT WRT CNT

2.18.4.15 USB Endpoint x IN CSR (Control & Status Register)

The USB Endpoint x IN CSR (Control and Status Register), shown in Figure 1.47, contains control and status information of the respective IN endpoint 1-4.

- **INxCSR0 (IN_PKT_RDY) and INxCSR5 (TX_FIFO_NOT_EMPTY):**

These two bits are for IN FIFO status when in read operation (see "IN (Transmit) FIFO" operation for details). The CPU writes a "1" to the INxCSR0 bit to inform the USB FCU that a packet of data is written to the FIFO. The USB FCU updates the pointers up on this bit set. The USB FCU also updates the pointers upon a packet of data successfully sent to the host. When the pointer updates are completed, the IN FIFO status is shown on INxCSR0 and INxCSR5 bits for the CPU to read. The CPU must allow at least one wait state between writing and reading these bits for proper FIFO status.

- **INxCSR1 (UNDER_RUN):**

This bit is used in ISO mode only to indicate to the CPU that a FIFO underrun has occurred. The USB FCU sets this bit to a "1" at the beginning of an IN token if no data packet is in the FIFO. Setting this bit causes the INST12 bit of the Interrupt Status Register 2 to set. The CPU writes a "0" to clear this bit.

- **INxCSR2 (SEND_STALL):**

The CPU writes a "1" to this bit when the endpoint is stalled (transmitter halt). The USB FCU returns a STALL handshake while this bit is set. The CPU writes a "0" to clear this bit.

- **INxCSR3 (ISO/TOGGLE_INIT):**

When the endpoint is used for isochronous data transfer, the CPU sets this bit to a "1" for the entire duration of the isochronous transfer. With the ISO bit set to a "1", the device uses DATA0 as the pid for all packets sent back to the host.

When the endpoint is required to initialize the data toggle, this set/reset of the TOGGLE_INIT bit method assumes that there is no activity IN transaction to the respective endpoint on the bus at the time the initialization process is ongoing. Set/reset of the TOGGLE_INIT bit is performed only when an endpoint experiences a configuration event.

- **INxCSR4 (INTPT):**

The CPU writes a "1" to this bit to initialize this endpoint as a status change endpoint for IN transactions. This bit is set only when the corresponding endpoint is to be used to communicate rate feedback information (see Chapter. IN (Transmit) FIFOs for details).

- **INxCSR5 (TX_FIFO_NOT_EMPTY):**

The USB FCU sets this bit to a "1" when there is at least one data packet in the IN FIFO. This bit, in conjunction with IN_PKT_RDY bit, provides the transmit IN FIFO status information (see "IN (Transmit) FIFO" for details).

- **INxCSR6 (FLUSH):**

Universal Serial Bus

The CPU writes a “1” to this bit to flush the IN FIFO. When there is one packet in the IN FIFO, a flush causes the IN FIFO to be empty. When there are two packets in the IN FIFO, a flush causes the older packet to be flushed out from the IN FIFO. Setting the INXCSR6 (FLUSH) bit during transmission could produce unpredictable results.

• **INXCSR7 (AUTO_SET):**

When the CPU sets this bit to a “1”, the IN_PKT_RDY bit is set automatically by the USB FCU after the number of bytes of data equal to the maximum packet size (MAXP) is written into the IN FIFO (see “IN (Transmit FIFO)” operation for details).

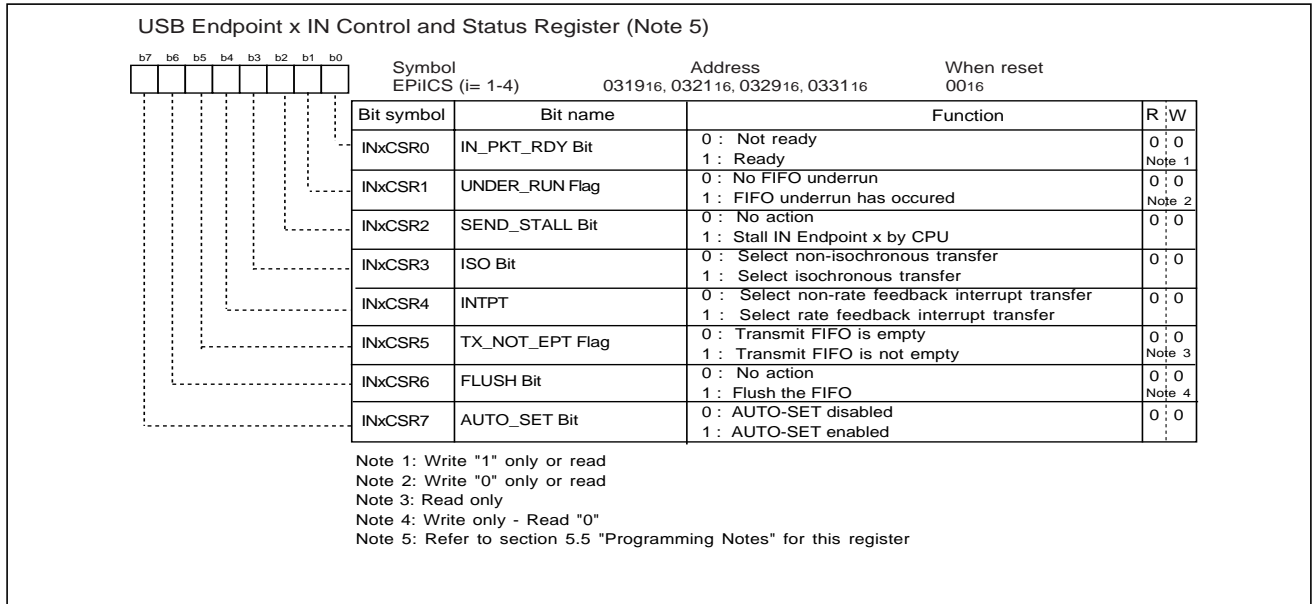


Figure 1.47: USB Endpoint x IN CSR

2.18.4.16 USB Endpoint x OUT Control and Status Register

The USB Endpoint x OUT CSR (Control and Status Register), shown in Figure 1.48 contains control and status information of the respective OUT endpoint 1-4.

• **OUTxCSR0 (OUT_PKT_RDY):**

The OUTxCSR0 bit for the OUT FIFO status (see “OUT (Receive) FIFOs” for details).

The USB FCU sets this bit to a “1” and updates the FIFO pointers after a data packet has been successfully received from the host. The CPU writes a “0” to this bit to inform the USB FCU that a data packet has been unloaded. The USB FCU updates the FIFO pointers when this occurs. The CPU must allow at least one clock cycle between writing and reading bit OUTxCSR0.

• **OUTxCSR1 (OVER_RUN):**

This bit is used in ISO mode only to indicate to the CPU that a FIFO overrun has occurred. The USB FCU sets this bit to a “1” at the beginning of an OUT token when two data packets are already present in the FIFO. Setting this bit causes the INST12 bit of the Interrupt Status Register 2 to set. The CPU writes a “0” to clear OUTXCSR1.

• **OUTxCSR2 (SEND_STALL):**

The CPU writes a “1” to this bit when the endpoint is stalled. The USB FCU returns a STALL handshake while this bit is set. The CPU writes a “0” to clear this bit.

• **OUTxCSR3 (ISO/TOGGLE_INIT):**

When the endpoint is used for isochronous data transfer, the CPU sets this bit to a “1” for the entire duration of the isochronous transfer. With the ISO/TOGGLE_INIT bit set to a “1”, the device accepts either DATA0 or DATA1 for the PID sent by the host.

Universal Serial Bus

When endpoint is required to initialize the data toggle sequence bit (i.e. reset to DATA0 for the next data packet), the CPU sets this bit to a “1” and then resets it to a “0” to initialize the respective endpoint’s data toggle.

Successful initialization of the data toggle sequence bit can only be guaranteed if no active OUT transaction to the respective endpoint is ongoing when the initialization process is taking place. Set/reset of the ISO/TOGGLE_INIT bit should only be performed when an endpoint experiences a configuration event.

• **OUTxCSR4 (FORCE_STALL):**

The USB FCU sets this bit to a “1” when the host sends out a larger data packet than the MAXP size. The USB FCU returns a STALL handshake while this bit is set. The CPU writes a “0” to clear this bit.

• **OUTxCSR5 (DATA_ERR):**

The USB FCU sets this bit to a “1” to indicate that a CRC error or a bit stuffing error was received in an ISO packet. The CPU writes a “0” to clear this bit.

• **OUTxCSR6 (FLUSH):**

The CPU writes a “1” to this to flush the OUT FIFO. When there is one packet in the OUT FIFO, a flush causes the OUT FIFO to be empty. When there are two packets in the OUT FIFO, a flush causes the older packet to be flushed out from the OUT FIFO. Setting the OUTXCSR6 (FLUSH) bit during reception could produce unpredictable results.

• **OUTxCSR7 (AUTO_CLR):**

When the CPU sets this bit to a “1”, the OUT_PKT_RDY bit is cleared automatically by the USB FCU after the number of bytes of data equal to the maximum packet size (MAXP) is unloaded from the OUT FIFO (see “OUT (Receive) FIFO” for details).

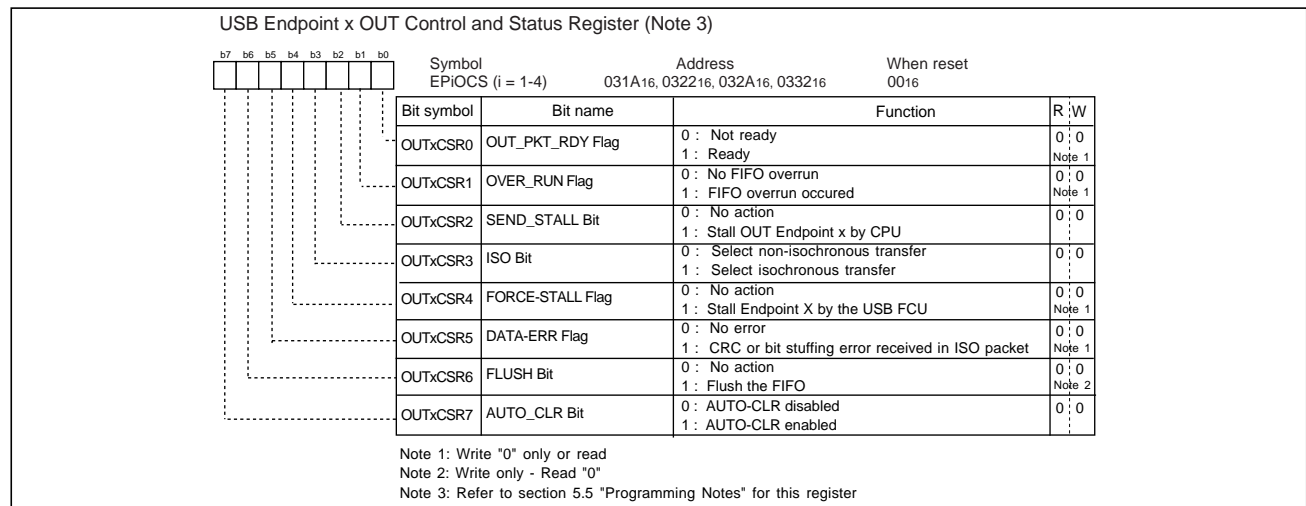


Figure 1.48: USB Endpoint x OUT CSR

2.18.4.17 USB Endpoint x IN MAXP Register

The USB Endpoint x IN MAXP Register, shown in Figure 1.49, indicates the maximum packet size (MAXP) of an Endpoint x IN packet. The default values for Endpoints 1-4 are 0 bytes. The setting of this register also affects the configuration of single/dual packet operation. When MAXP > 1/2 of the FIFO size, single packet mode is set. When MAXP <= 1/2 of the FIFO size, dual packet mode is set.

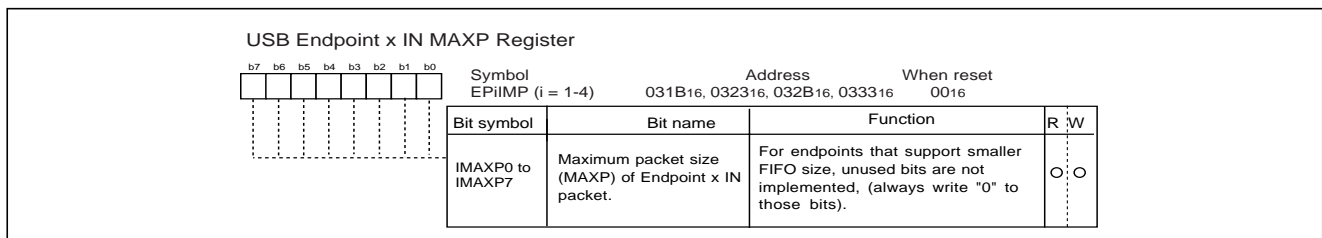


Figure 1.49: USB Endpoint x IN MAXP

Universal Serial Bus

2.18.4.18 USB Endpoint x OUT MAXP Register

The USB Endpoint x OUT MAXP Register, shown in Figure 1.50, indicates the maximum packet size (MAXP) of an Endpoint x OUT packet. The default values for endpoints 1-4 are 0 bytes. The setting of this register also affects the configuration of single/dual packet operation. When MAXP > 1/2 of the FIFO size, single packet is set. When MAXP <= 1/2 of the FIFO size, dual packet mode is set.

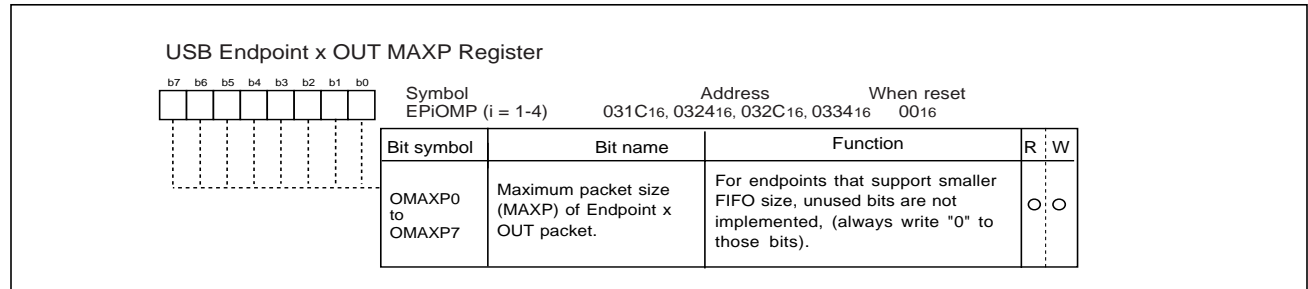


Figure 1.50: USB Endpoint x OUT MAXP

2.18.4.19 USB Endpoint x OUT WRT CNT Register

The USB Endpoint x OUT WRT CNT Register, shown in Figure 1.51, contains the number of bytes of the current data set in the OUT FIFO. The USB FCU sets the value in the Write Count Register after having successfully received a packet of data from the host. The CPU reads the register to determine the number of bytes to be read from the FIFO.

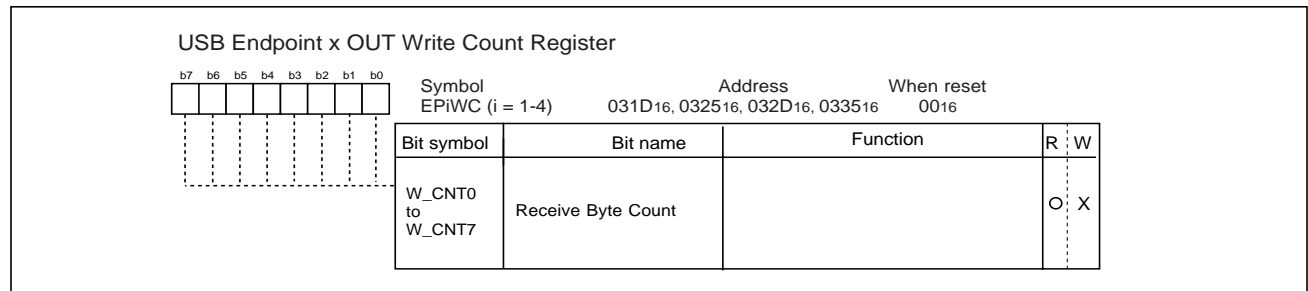


Figure 1.51: USB Endpoint x OUT WRT CNT

2.18.4.20 USB Endpoint x FIFO Register

The USB Endpoint x FIFO Register, shown in Figure 1.52 is the USB IN (transmit) and OUT (receive) FIFO data register. The CPU writes data to this register for the corresponding Endpoint IN FIFO and reads data from this register for the corresponding Endpoint OUT FIFO.

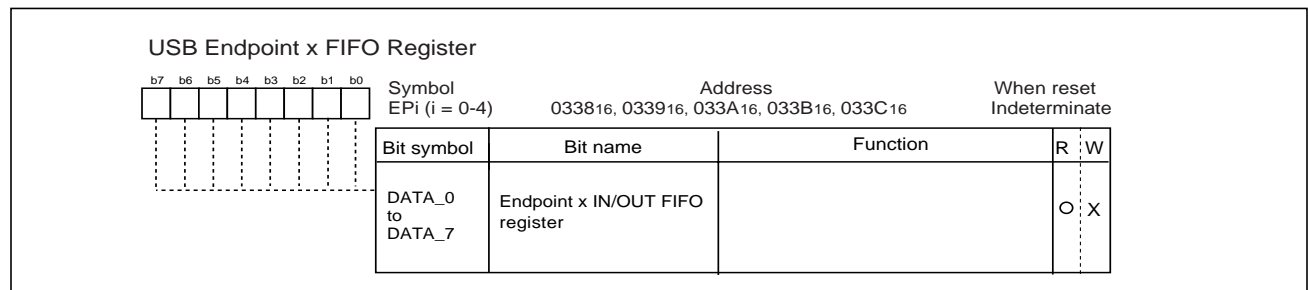


Figure 1.52: USB Endpoint x FIFO Register

DMAC

2.19 DMAC

This microcomputer has two DMAC (direct memory access controller) channels that allow data to be sent to memory without using the CPU. Table 1.14 shows the DMAC specifications. Figure 1.53 shows the block diagram of the DMAC. Figure 1.54, Figure 1.55 and Figure 1.56 show the registers used by the DMAC.

Table 1.14: DMAC specifications

Item	Specification
Number of channels	2 (cycle steal method)
Transfer memory space	<ul style="list-style-type: none"> •From any SFR, RAM, or ROM address to a fixed address •From a fixed address to any SFR or RAM address •From a fixed address to a fixed address (Note that DMA-related registers [0020 ₁₆ to 003F ₁₆] cannot be accessed)
Maximum number of bytes transferred	128K bytes (with 16-bit transfers) or 64K bytes (with 8-bit transfers)
DMA request sources	Falling edge of INT0 or INT1 (INT0 can be selected by DMA0, INT1 by DMA1) Timer A0 to timer A4 Timer B0 to timer B1 UART0 transmission and reception UART1 transmission and reception UART2 transmission and reception A-D conversion complete USB function Software triggers
Channel priority	DMA0 takes precedence if DMA0 and DMA1 requests are generated simultaneously
Transfer unit	8 bits or 16 bits
Transfer address direction	forward/fixed (forward direction cannot be specified for both source and destination simultaneously)
Transfer modes	Single transfer mode The DMA enable bit is cleared and transfer ends when an underflow occurs in the transfer counter. Repeat transfer mode When an underflow occurs in the transfer counter, the value in the transfer counter reload register is loaded into the transfer counter and the DMA transfer is repeated
DMA interrupt request generation timing	When an underflow occurs in the transfer counter
DMA startup	Single transfer mode Transfer starts when the DMA is requested after "1" is written to the DMA enable bit Repeat transfer mode Transfer starts when the DMA is requested after "1" is written to the DMA enable bit or after an underflow occurs in the transfer counter
DMA shutdown	When "0" is written to the DMA enable bit When, in single transfer mode, an underflow occurs in the transfer counter
Forward address pointer and reload timing for transfer counter	When DMA transfer starts, the value of whichever of the source or destination pointer that is set up as the forward pointer is loaded into the forward address pointer. The value in the transfer counter reload register is loaded into the transfer counter.
Writing to register	Registers specified for forward direction transfer are always write-enabled. Registers specified for fixed address transfer are write-enabled when the DMA enable bit is "0".
Reading the register	Can be read at any time. However, when the DMA enable bit is "1", reading the register sets up as the forward register is the same as reading the value of the forward address pointer.

DMAC

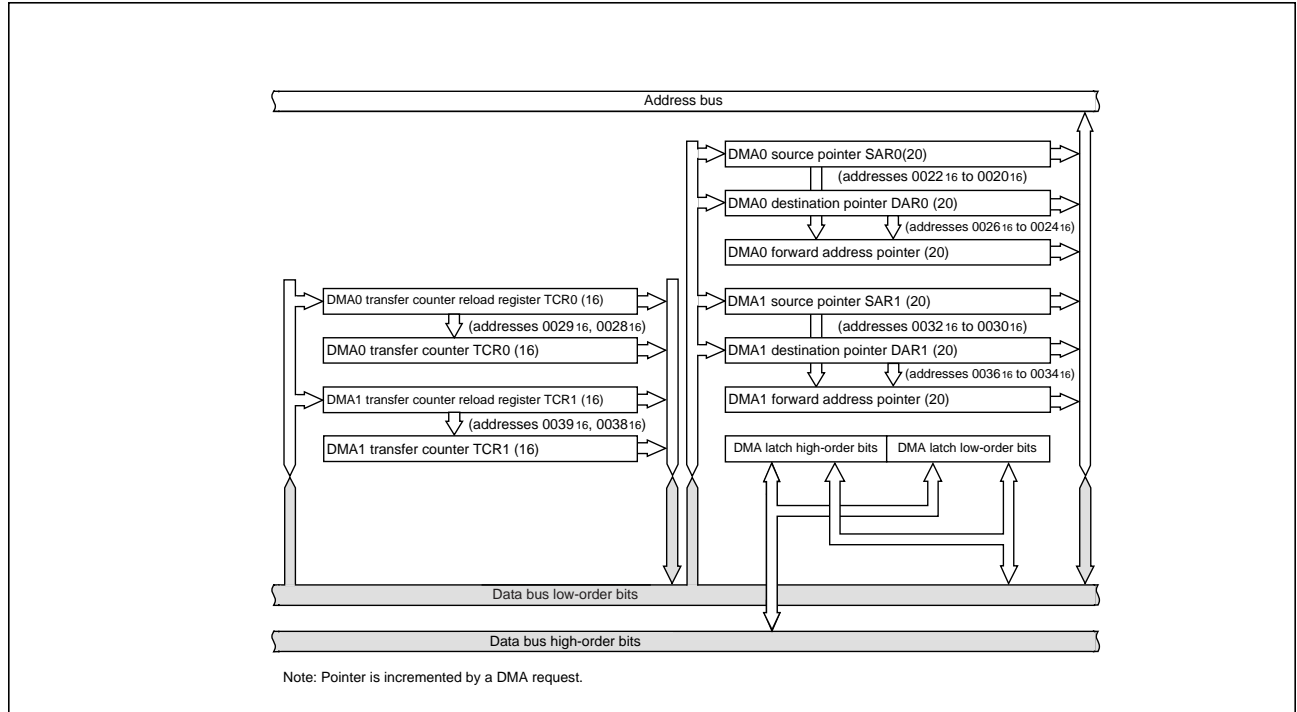


Figure 1.53: Block diagram of DMAC

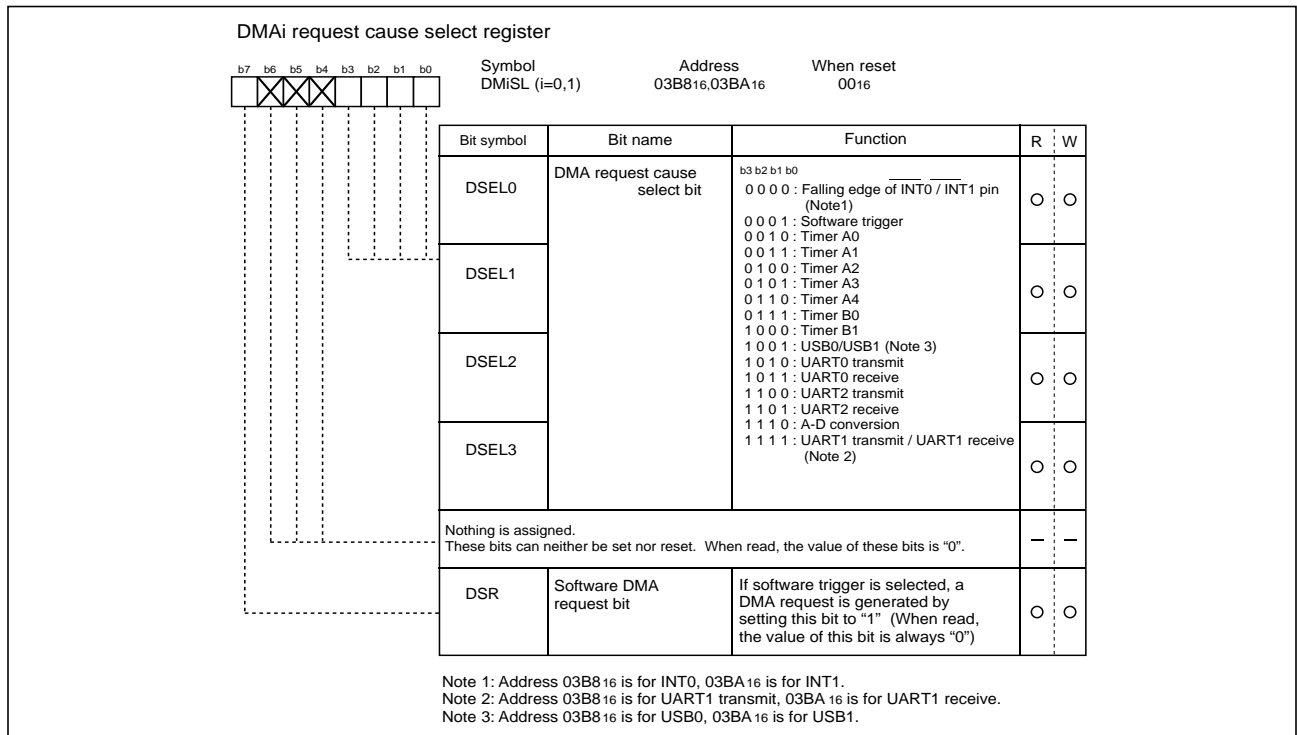


Figure 1.54: DMAC register (1)

DMAC

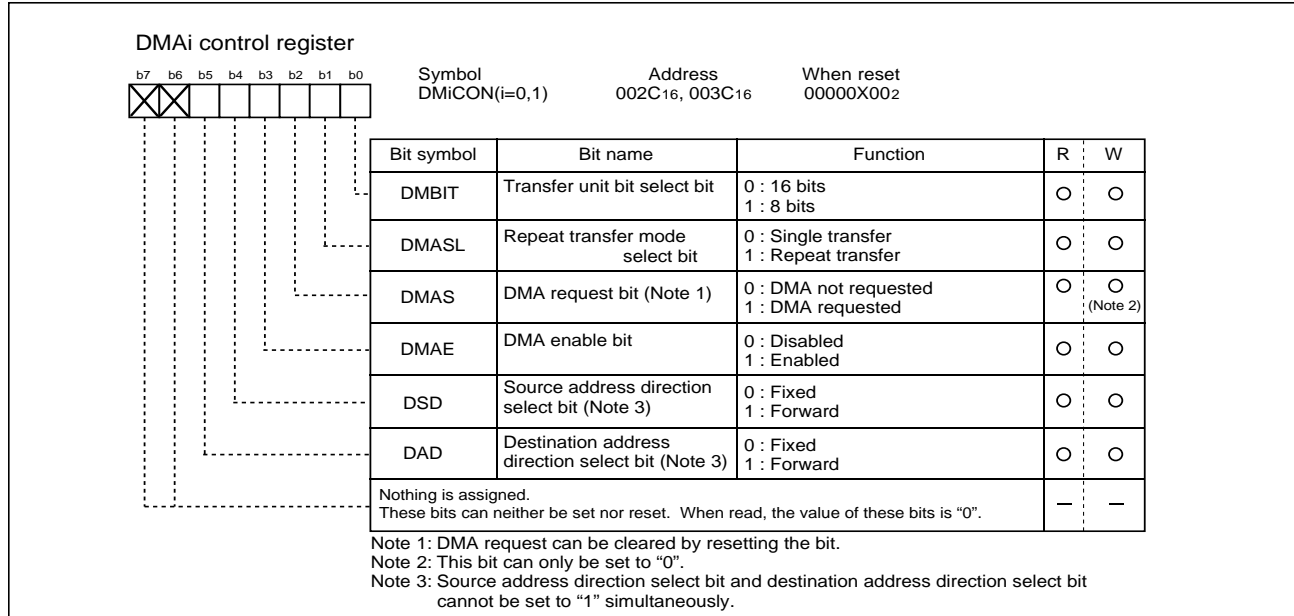


Figure 1.55: DMAC register (2)

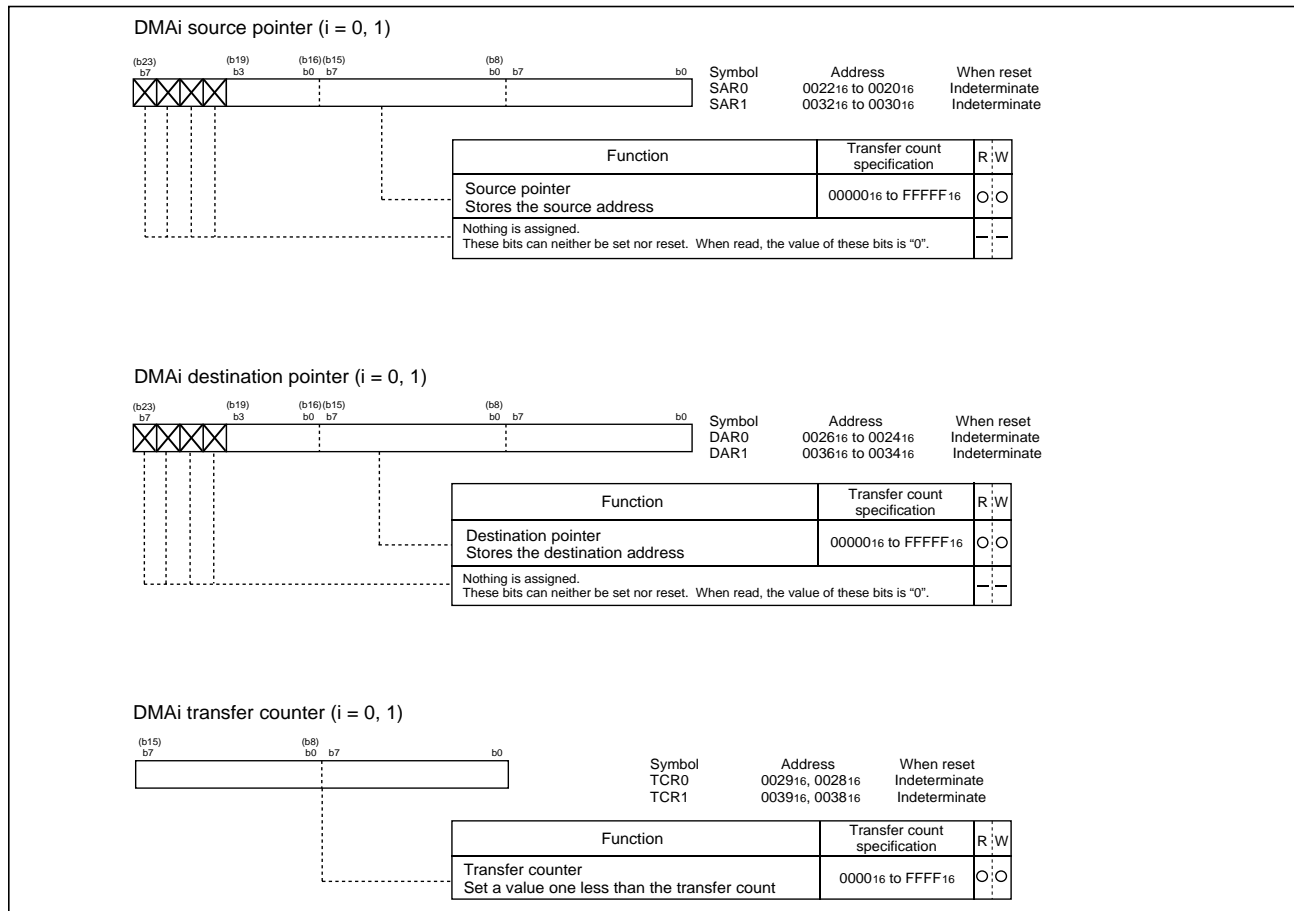


Figure 1.56: DMAC register (3)



DMAC

2.19.1 Transfer cycle

The transfer cycle consists of the bus cycle in which data is read from memory or from the SFR area (source read) and the bus cycle in which the data is written to memory or to the SFR area (destination write). The number of read and write bus cycles depends on the source and destination addresses and the software waits are inserted.

2.19.1.1 Effect of source and destination addresses

When 16-bit data is transferred on a 16-bit data bus, and the source and destination both start at odd addresses, there is one more source read cycle and destination write cycle than when the source and destination both start at even addresses.

2.19.2 DMAC transfer cycles

Any combination of even or odd transfer read and write addresses is possible. Table 1.15 show the number of DMAC transfer cycles. Table 1.16 shows the corresponding coefficient values. Figure 1.57 shows an example of the transfer cycle for a source read.

The number of DMAC transfer cycles can be calculated as follows:

$$\text{Number of transfer cycles per transfer unit} = \text{Number of read cycles} \times j + \text{Number of write cycles} \times k$$

Table 1.15: Number of DMAC transfer cycles

Transfer unit	Access address	Single-chip mode	
		Number of read cycles	Number of write cycles
8-bit transfers (DMBIT="1")	Even	1	1
	Odd	1	1
16-bit transfers (DMBIT="0")	Even	1	1
	Odd	2	2

Table 1.16: Coefficients j,k

Internal memory		
Internal ROM/ RAM No wait	Internal ROM/ RAM with wait	SFR area
1	2	2

DMAC

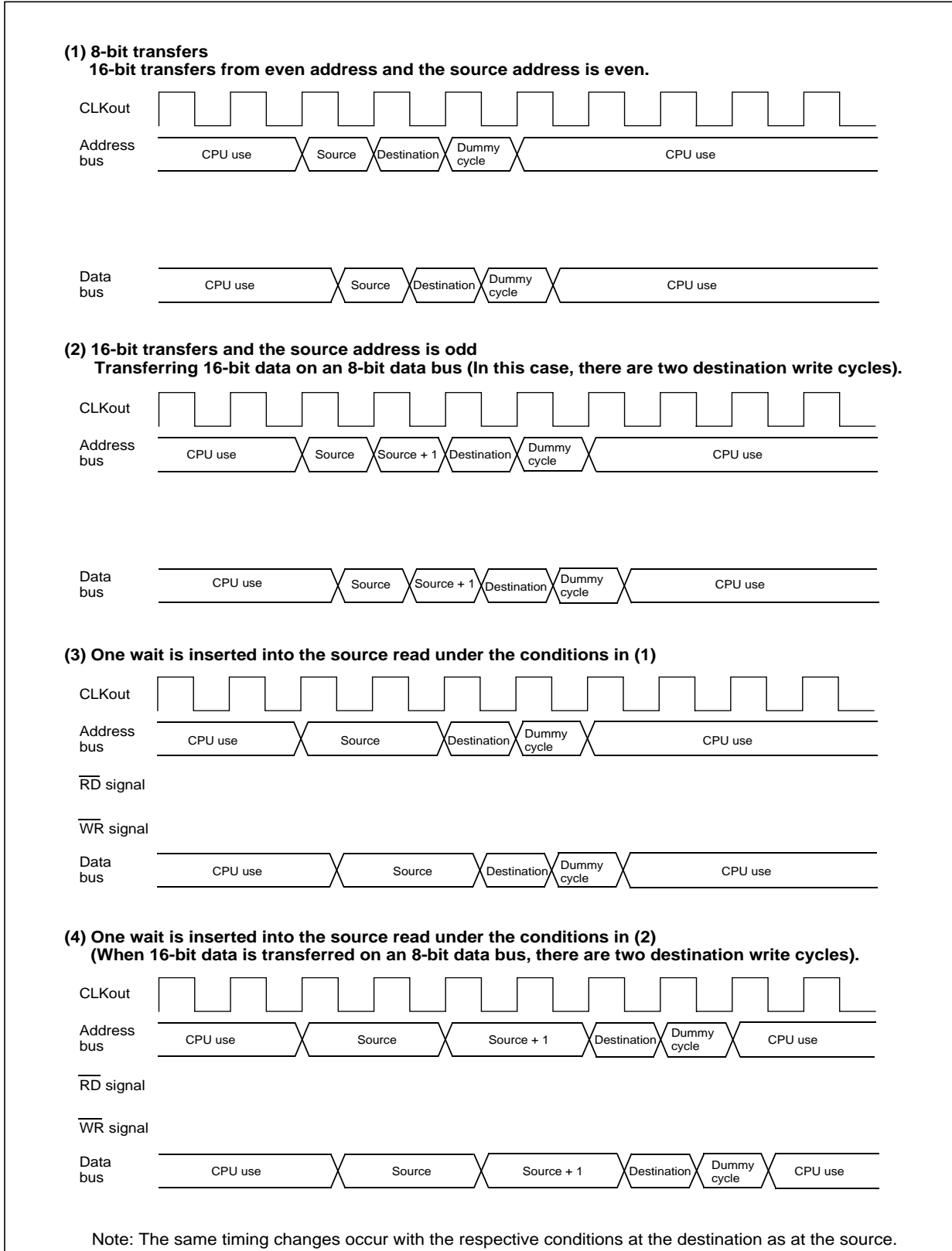


Figure 1.57: Example of the transfer cycle for a source read

Timers

2.20 Timers

There are eight 16-bit timers. These timers can be classified by function into timers A (five) and timers B (three). All these timers function independently. Figure 1.58 shows the block diagram of Timers A and B.

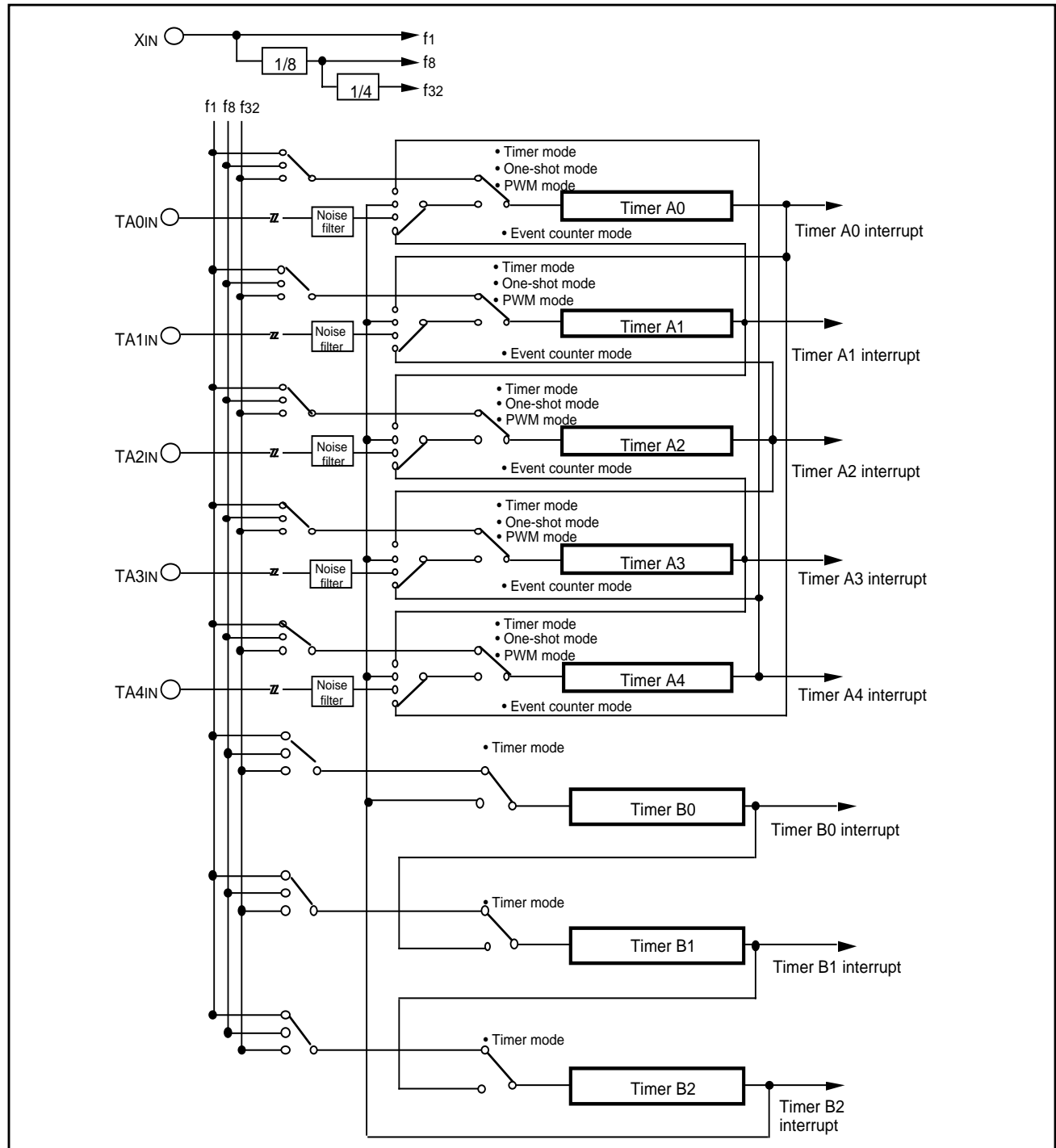


Figure 1.58: Timer A and Timer B block diagram

Timer A

2.21 Timer A

Figure 1.59, Figure 1.60, Figure 1.61, and Figure 1.62 show the timer A-related registers.

Except in event counter mode, timers A0 through A4 all have the same function. Use the timer Ai mode register (i = 0 to 4) bits 0 and 1 to choose the desired mode.

Timer A has the four operation modes listed as follows:

- Timer mode: The timer counts an internal count source.
- Event counter mode: The timer counts pulses from an external source or a timer overflow.
- One-shot timer mode: The timer stops counting when the count reaches "0000₁₆".
- Pulse width modulation (PWM) mode: The timer outputs pulses of a given width.

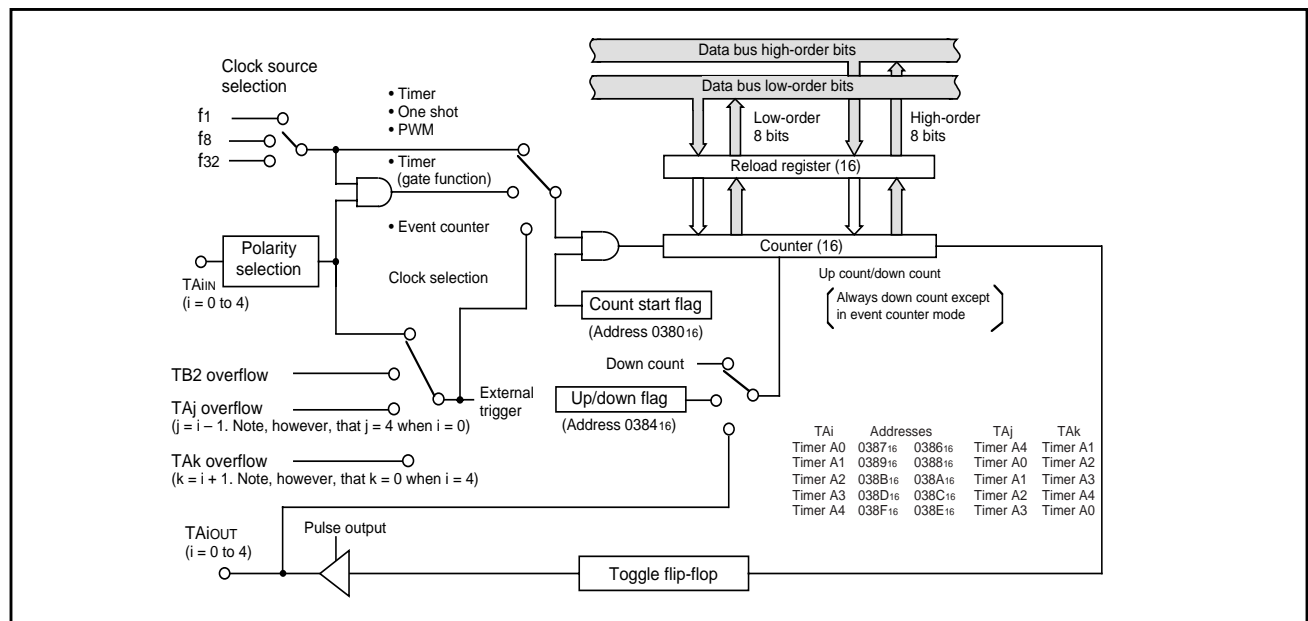


Figure 1.59: Block diagram of Timer A

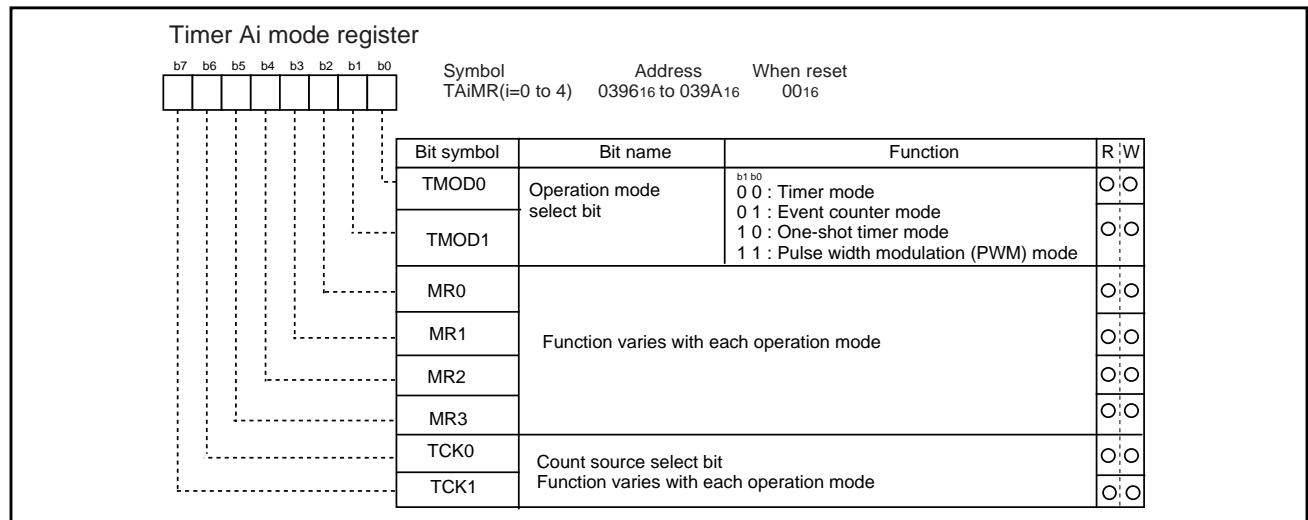


Figure 1.60: Timer A related Registers (1)



Timer A

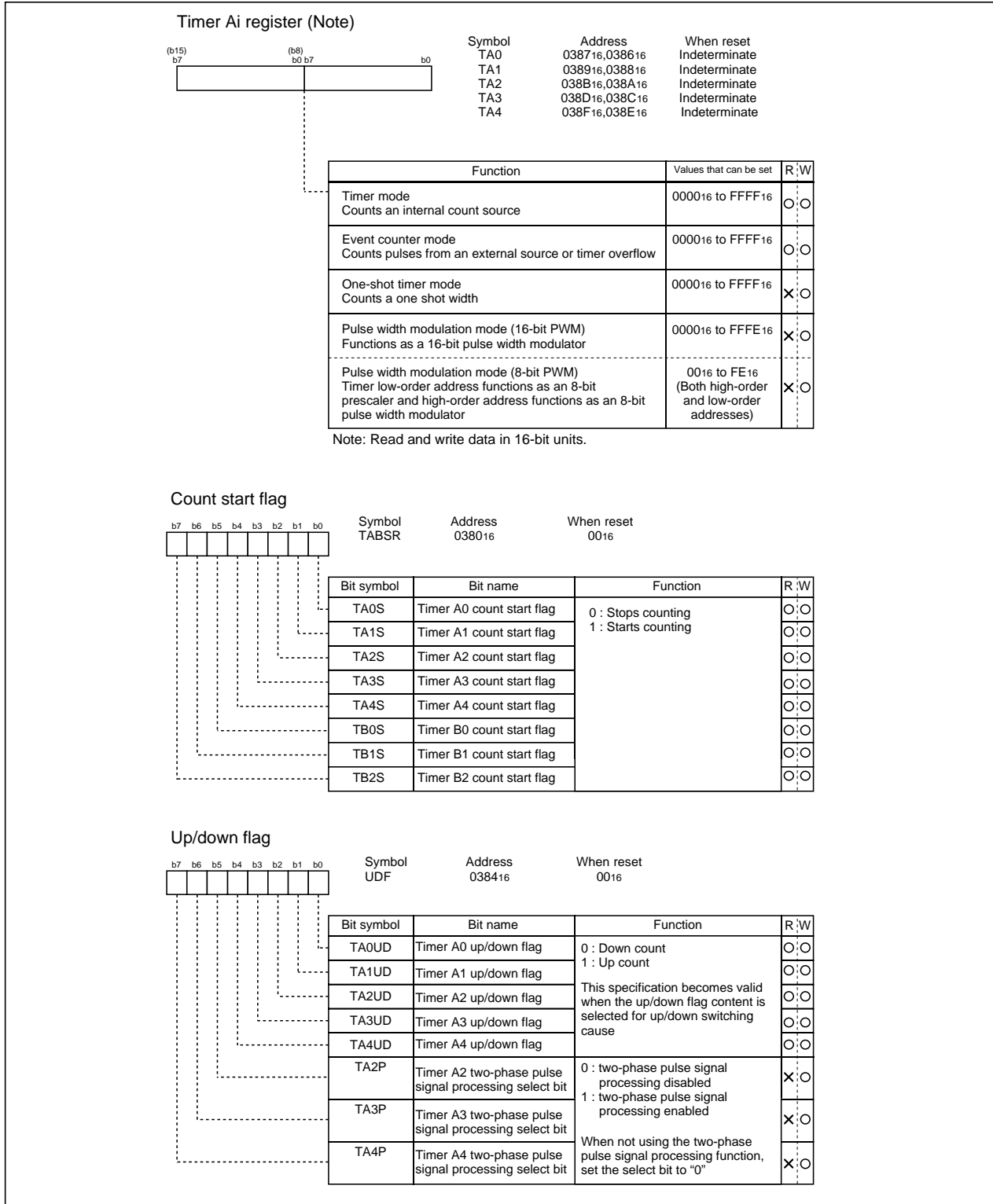


Figure 1.61: Timer A-related registers (2)

Timer A

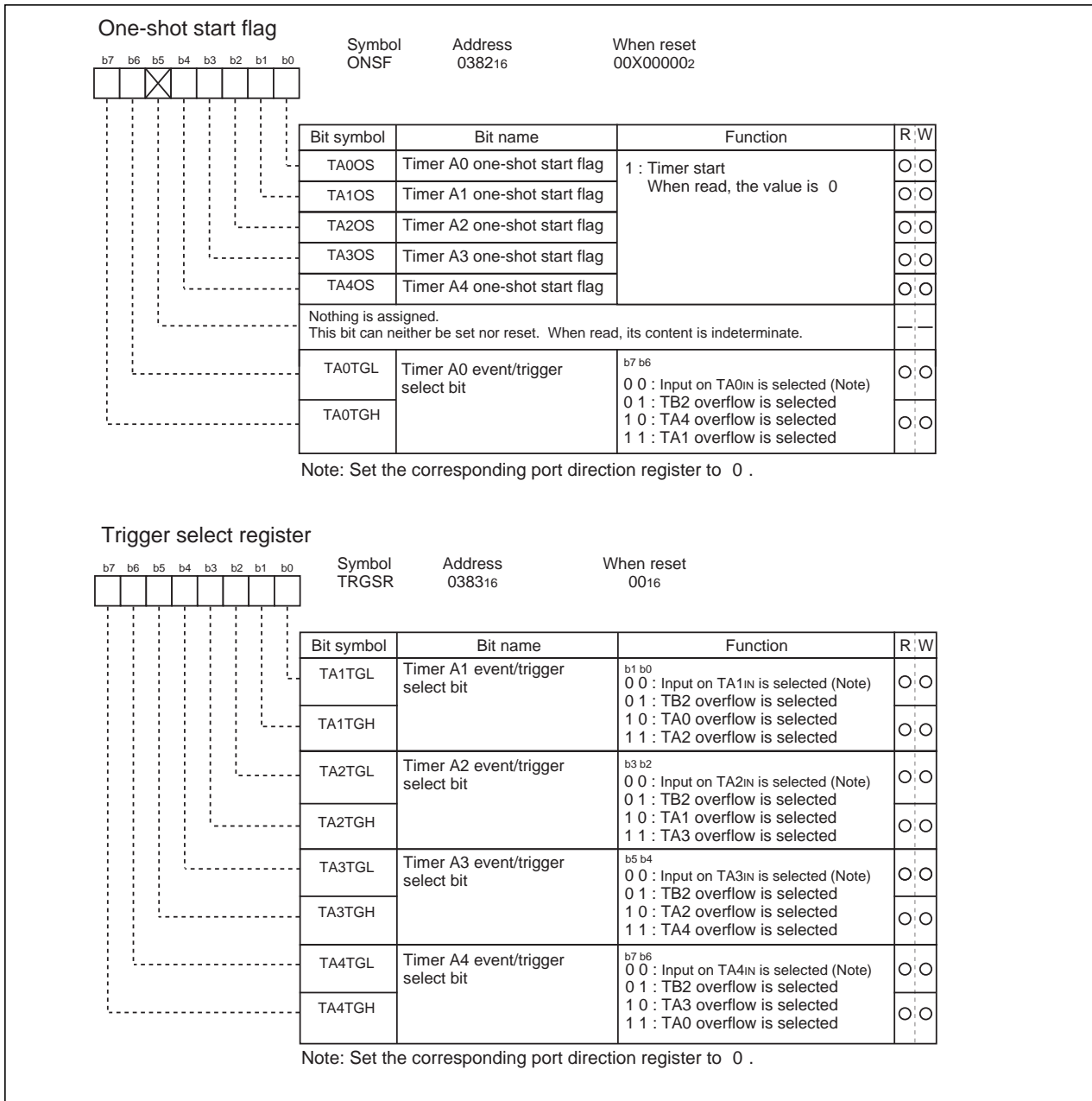


Figure 1.62: Timer A-related registers (3)

Timer A

2.21.1 Timer mode

In this mode, the timer counts an internally generated count source. See Table 1.17 below. Figure 1.63 shows the timer Ai mode register in timer mode.

Table 1.17: Specifications of timer mode

Item	Specification
Count source	f1, f8, f32
Count operation	<ul style="list-style-type: none"> • Down count • When the timer underflows, it loads the reload register contents before continuing counting
Divide ratio	1/(n+1) n: Set value
Count start condition	Count start flag is set (= 1)
Count stop condition	Count start flag is reset (= 0)
Interrupt request generation timing	When the timer underflows
TAiIN pin function	Programmable I/O port or gate input
TAiOUT pin function	Programmable I/O port or pulse output
Read from timer	Count value can be read out by reading timer Ai register
Write to timer	<ul style="list-style-type: none"> • When counting is stopped and a value is written to timer Ai register, it is written to both reload register and counter • When counting is in progress and a value is written to timer Ai register, it is written only to reload register (to be transferred to counter at the next reload time)
Select function	<ul style="list-style-type: none"> • Gate function Counting can be started and stopped by TAiIN pin's input signal • Pulse output function Each time the timer underflows, the TAiOUT pin's polarity is reversed

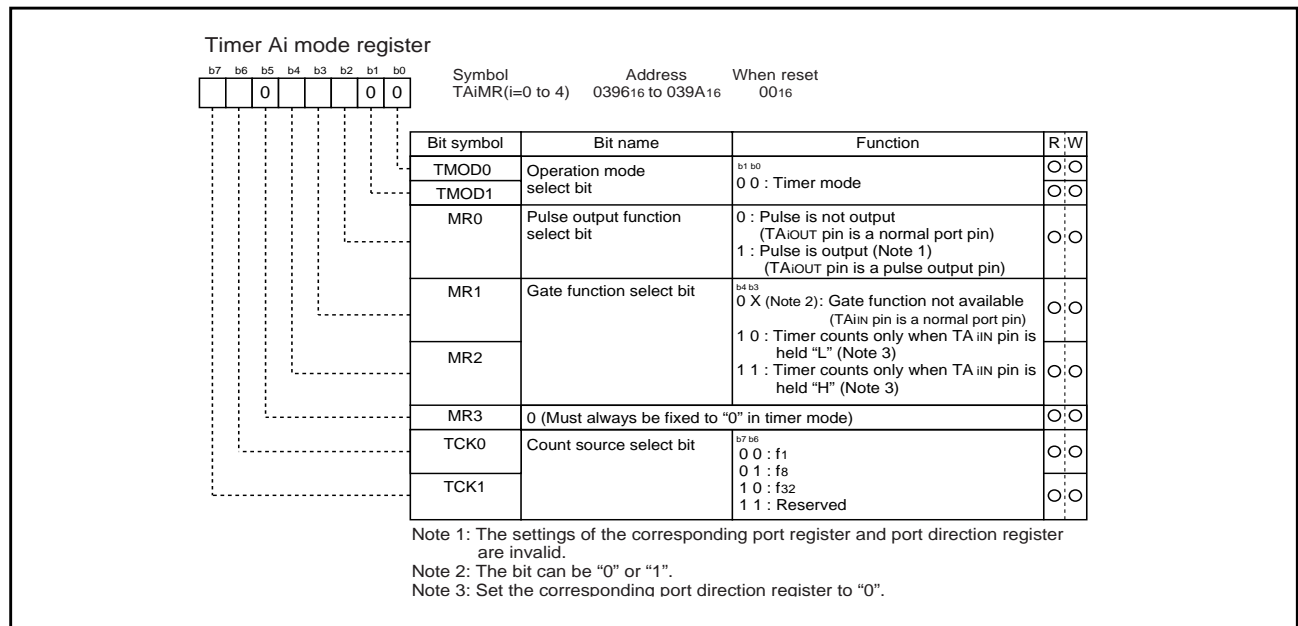


Figure 1.63: Timer Ai mode register in timer mode



Timer A

2.21.2 Event counter mode

In this mode, the timer counts an external signal or an internal timer's overflow. Timers A0 and A1 can count a single-phase external signal. Timers A2, A3, and A4 can count a single-phase and a two-phase external signal. Table 1.18 lists the timer specifications when counting a single-phase external signal. Figure 1.64 shows Timer Ai mode register in event counter mode, single-phase signal.

Table 1.18: Timer specification in event counter mode (when not processing two-phase pulse signal)

Item	Specification
Count source	<ul style="list-style-type: none"> •External signals input to TAIIN pin (effective edge can be selected by software) •TB2 overflow, TAJ overflow
Count operation	<ul style="list-style-type: none"> •Up count or down count can be selected by external signal or software •When the timer overflows or underflows, it loads from the reload register contents before continuing counting. (However, this does not apply when the free-run function is selected.)
Divide ratio	1/ (FFFF ₁₆ - n+1) for up count 1/ (n + 1) for down count n: set value
Count start condition	Count start flag is set (=1)
Count stop condition	Count start flag is reset (=0)
Interrupt request generation timing	Timer overflows or underflows
TAiIN pin function	Programmable I/O port or count source input
TAiOUT pin function	Programmable I/O port, pulse output, or up/down count select input
Read from timer	Count value can be read out by reading timer Ai register
Write to timer	<ul style="list-style-type: none"> •When counting is stopped and a value is written to timer Ai register, it is written to both reload register and counter •When counting is in progress and a value is written to timer Ai register, it is written to only reload register
Select function	<ul style="list-style-type: none"> •Free-run count function When the timer overflows or underflows, the reload register content is not reloaded. •Pulse output function Each time the timer overflows, the TAIOUT pin's polarity is reversed

Timer A

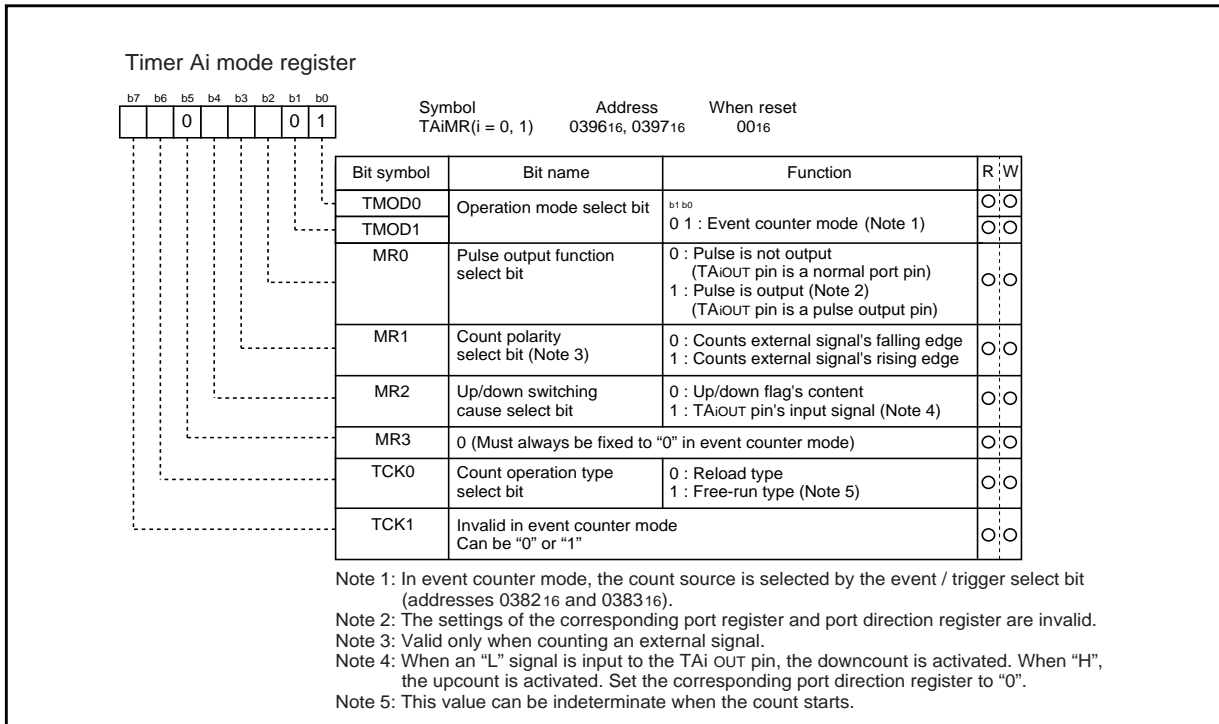


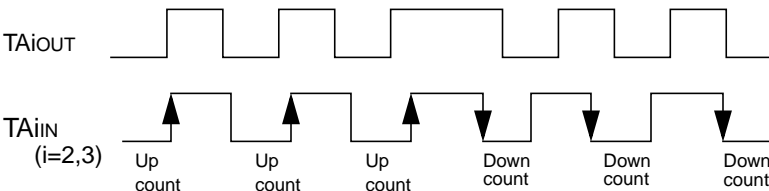
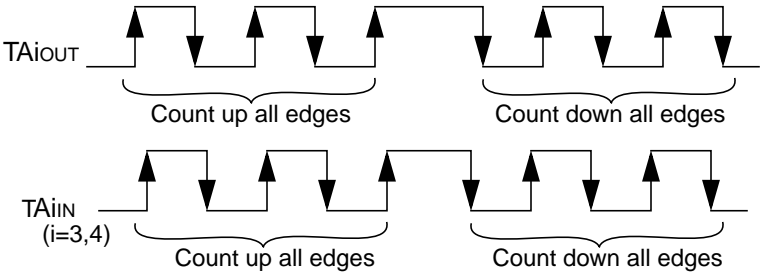
Figure 1.64: Timer Ai mode register in event counter mode, single signal

Table 1.19 shows the Timer specification in event counter mode when processing two-phase signal with timers A2, A3, and A4.

Figure 1.65 shows Timer Ai mode register in event counter mode when processing two-phase signal.

Timer A

Table 1.19: Timer specification in even counter mode (when processing two-phase pulse signal with timers A2, A3, and A4)

Item	Specification
Count Source	•Two-phase pulse signals input to TAIiN or TAIiOUT pin
Count operation	•Up count or down count can be selected by two-phase pulse signal •When the timer overflows or underflows, the reload register content is loaded and the timer starts over again (Note 1)
Divide ratio	1/ (FFFF ₁₆ - n + 1) for up count 1/ (n+1) for down count n: Set value
Count start condition	Count start flag is set (=1)
Count stop condition	Count start flag is reset (=0)
Interrupt request generation timing	Timer overflow or underflows
TAiIN pin function	Two-phase pulse input
TAiOUT pin function	Two-phase pulse input
Read from timer	Count value can be read out by reading timer A2, A3, or A4 register
Writer to timer	•When counting is stopped and a value is written to timer A2, A3, or A4 register, it is written to both the reload register and counter •When counting is in progress and a value is written to timer A2, A3, or A4 register, it is written to only reload register to be transferred to counter at the next reload time.
Select function	<p>•Normal processing operation The timer counts up rising edges or counts down falling edges on the TAIiN pin when input signal on the TAIiOUT pin is "H"</p>  <p>•Multiply-by-4 processing operation If the phase relationship is such that the TAIiN pin goes "H" when the input signal on the TAIiOUT pin is "H", the timer counts up rising and falling edges on the TAIiOUT and TAIiN pins. If the phase relationship is such that the TAIiN pin goes "L" when the input signal on the TAIiOUT pin is "H", the timer counts down rising and falling edges on the TAIiOUT and TAIiN pins.</p> 

Note 1 This does not apply when the free-run function is selected.



Timer A

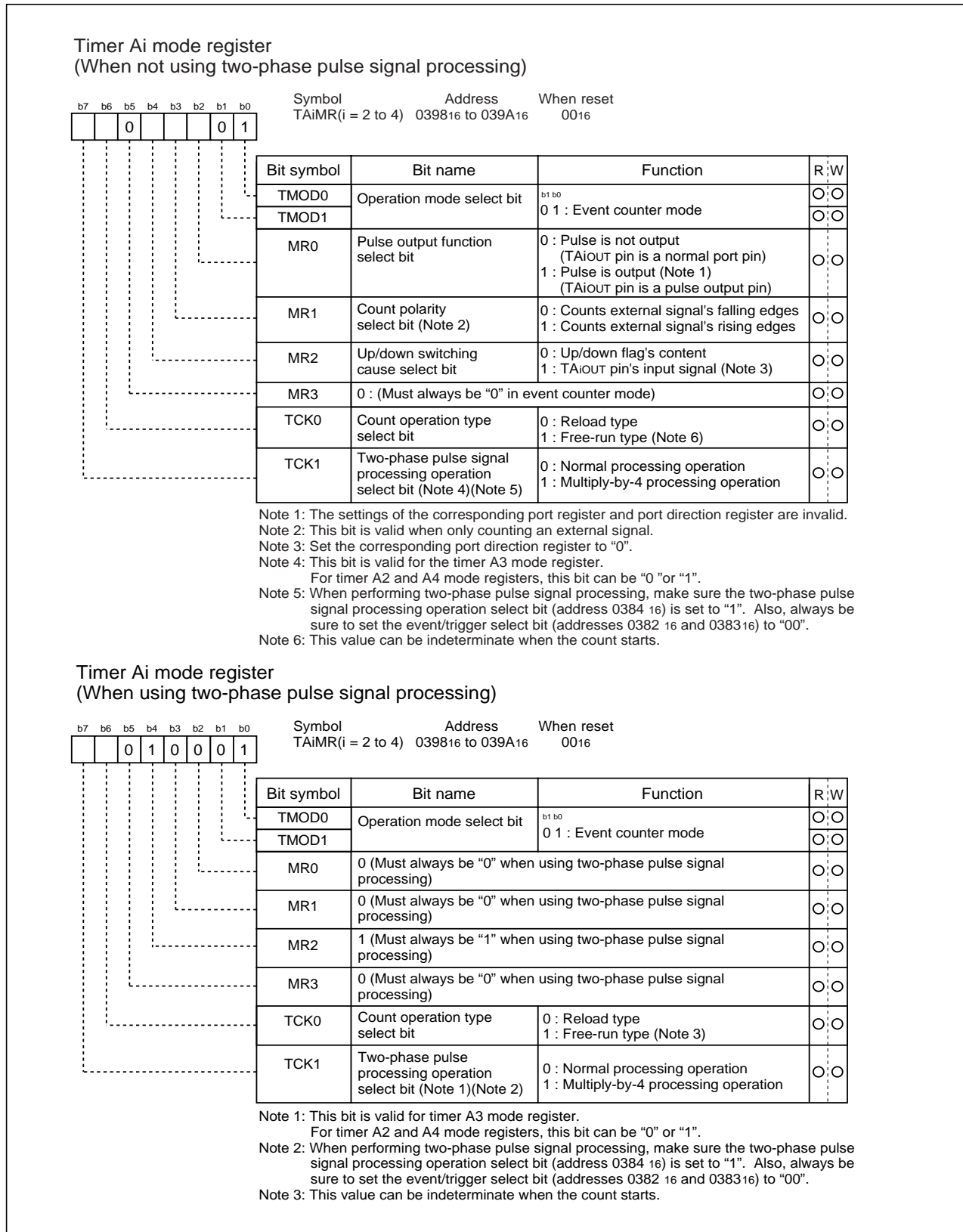


Figure 1.65: Timer Ai mode register in event counter mode, two-phase signal

Timer A

2.21.3 One-shot timer mode

In this mode, the timer operates only once (See Table 1.20). When a trigger occurs, the timer starts up and continues operating for a given period. Figure 1.66 shows the timer Ai mode register in one-shot mode.

Table 1.20: Timer specifications in one-shot timer mode

Item	Specification
Count source	f1, f8, f32
Count operation	<ul style="list-style-type: none"> The timer counts down When the count reaches 0000₁₆, the timer stops counting after reloading a new count If a trigger occurs when counting, the timer reloads a new count and restarts counting
Divide ratio	1/n n: Set value
Count start condition	<ul style="list-style-type: none"> An external trigger is input The selected timer overflows The one-shot start flag is set (= 1)
Count stop condition	<ul style="list-style-type: none"> A new count is reloaded after the count has reached 0000₁₆ The count start flag is reset (= 0)
Interrupt request generation timing	The count reaches 0000 ₁₆
TAiIN pin function	Programmable I/O port or trigger input
TAiOUT pin function	Programmable I/O port or pulse output
Read from timer	When timer Ai register is read, it indicates an indeterminate value
Write to timer	<ul style="list-style-type: none"> When counting is stopped and a value is written to timer Ai register, it is written to both reload register and counter When counting is in progress and a value is written to timer Ai register, it is written to the reload register to be transferred to counter at next load time

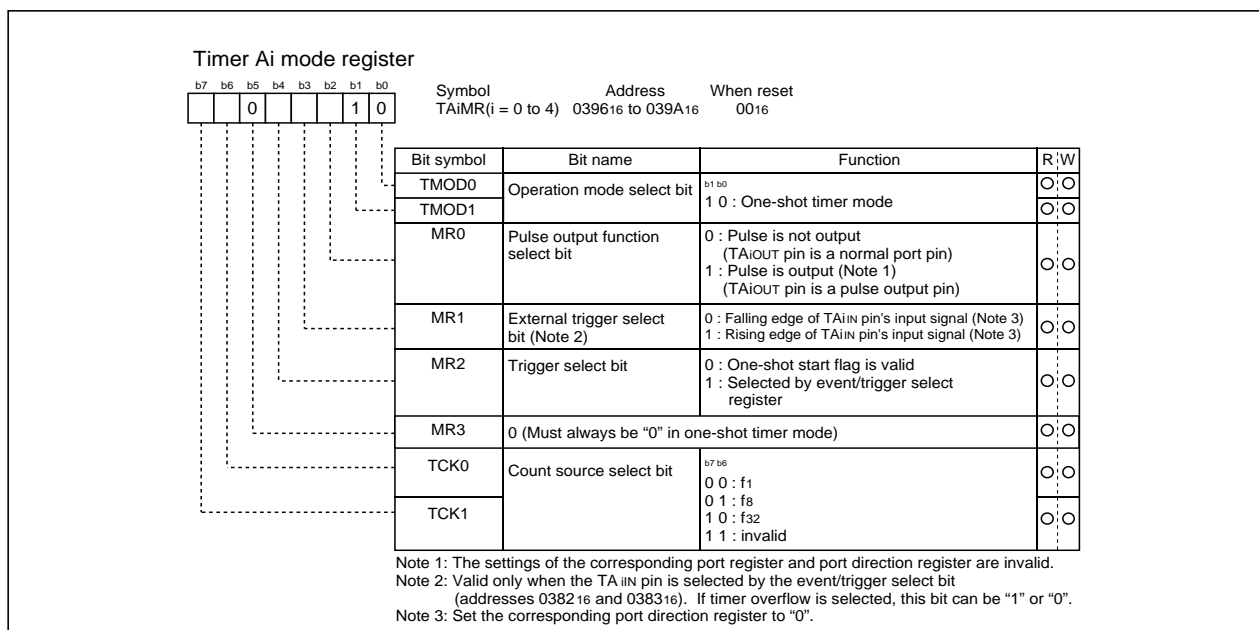


Figure 1.66: Timer Ai mode register in one-shot mode

Timer A

2.21.4 Pulse-width modulation (PWM) mode

In this mode, the timer outputs pulses of a given width in succession (See Table 1.21). In this mode, the counter functions as either a 16-bit pulse-width modulator or an 8-bit pulse-width modulator. Figure 1.67 shows the timer Ai mode register in pulse-width modulation mode. Figure 1.68 shows the example of how a 16-bit pulse-width modulator operates. Figure 1.69 shows the example of how an 8-bit pulse width modulator operates.

Table 1.21: Timer specifications in pulse-width modulation mode

Item	Specification
Count source	f1, f8, f32
Count operation	<ul style="list-style-type: none"> •The timer counts down (operating as an 8-bit or a 16-bit pulse-width modulator) •The timer reloads a new count at a rising edge of PWM pulse and continues counting • The timer is not affected by a trigger that occurs when counting
16-bit PWM	<ul style="list-style-type: none"> •High level width n / f_i n: Set value •Cycle time $(2^{16}-1) / f_i$ fixed
8-bit PWM	<ul style="list-style-type: none"> •High level width $n (m+1) / f_i$ n: values set to timer Ai register's high-order address •Cycle time $(2^8-1) (m+1) / f_i$ m: values set to timer Ai register's low-order address
Count start condition	<ul style="list-style-type: none"> •External trigger is input •The timer overflows •The count start flag is set (= 1)
Count stop condition	•The count start flag is reset (= 0)
Interrupt request generation timing	PWM pulse goes "L"
TAiIN pin function	Programmable I/O port or trigger input
TAiOUT pin function	Pulse output
Read from timer	When timer Ai register is read, it indicates an indeterminate value
Write to timer	<ul style="list-style-type: none"> •When counting is stopped and a value is written to timer Ai register, it is written to both reload register and the counter •When counting in progress and a value is written to timer A register, it is written to only reload register to be transferred to the counter at next reload timer.

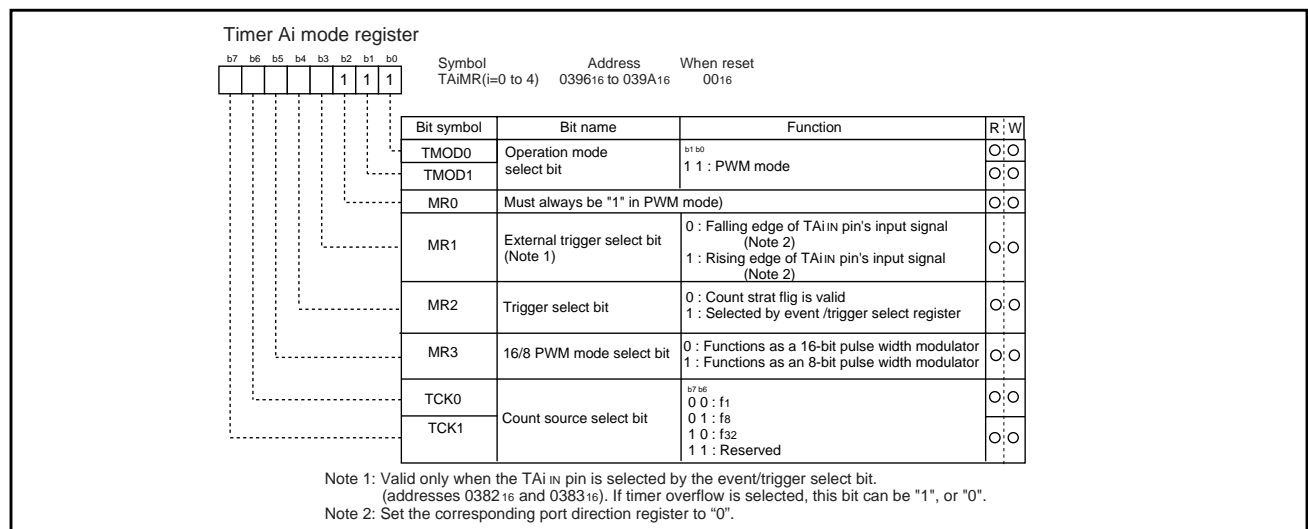


Figure 1.67: Timer Ai mode register in pulse-width modulation mode

Timer A

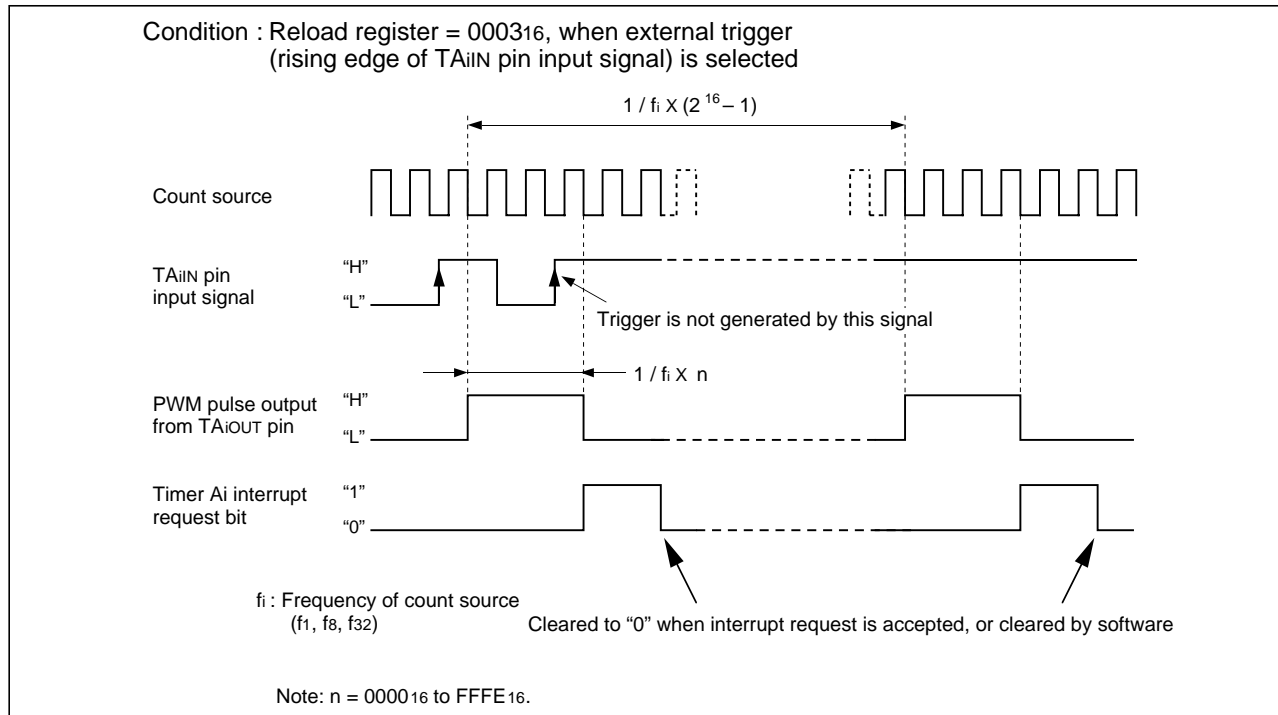


Figure 1.68: Example of how a 16-bit pulse-width modulator operates

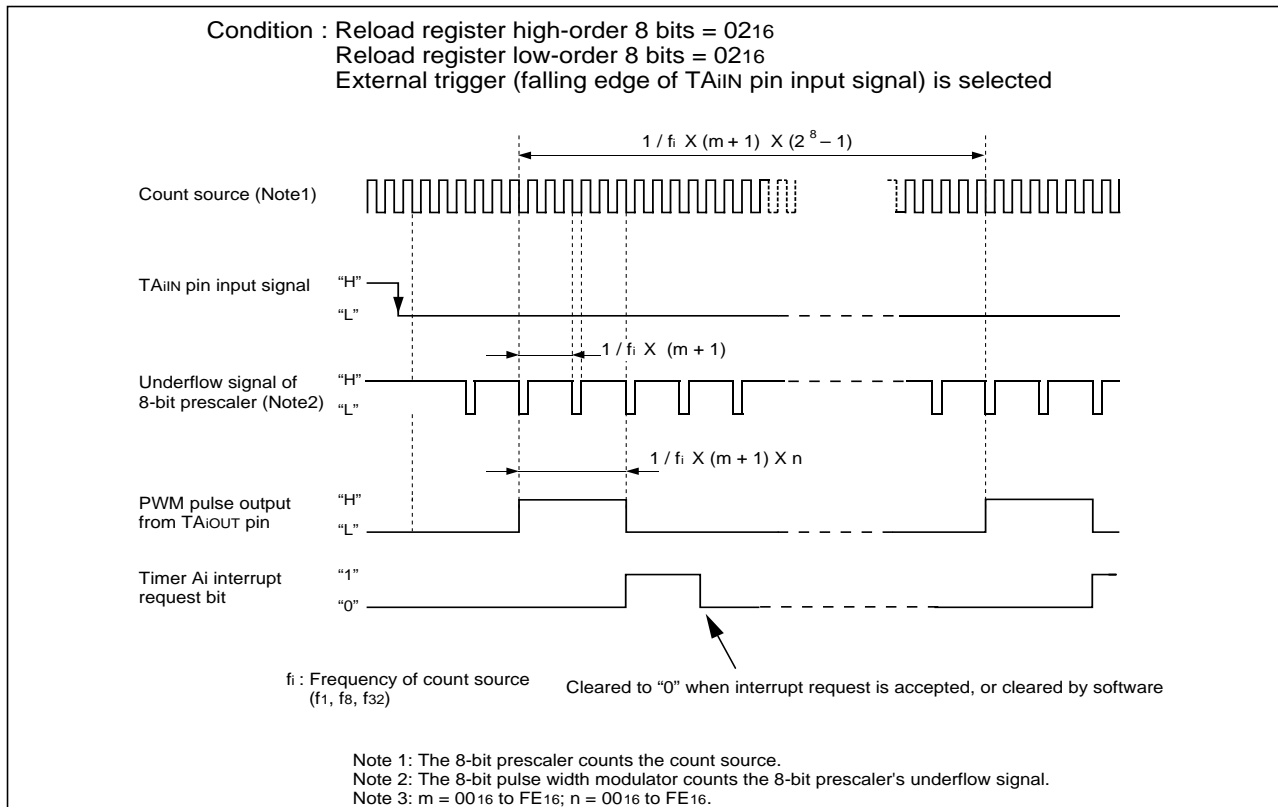


Figure 1.69: Example of how an 8-bit pulse-width modulator operates

Timer B

2.22 Timer B

Figure 1.70 shows the block diagram of timer B. Figure 1.71 and Figure 1.72 show the timer B-related registers. Use the timer Bi mode register (i = 0 to 2) bits 0 and 1 to choose the desired mode. Timer B works in Timer mode only (i.e., the timer counts an in internal count source).

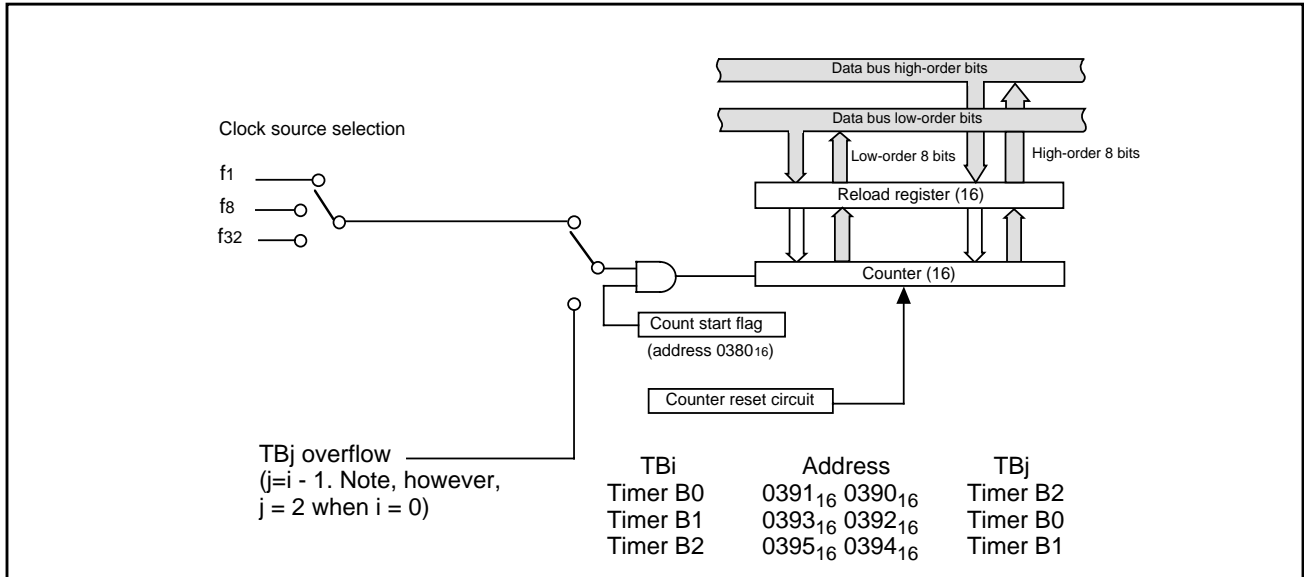


Figure 1.70: Block diagram of Timer B

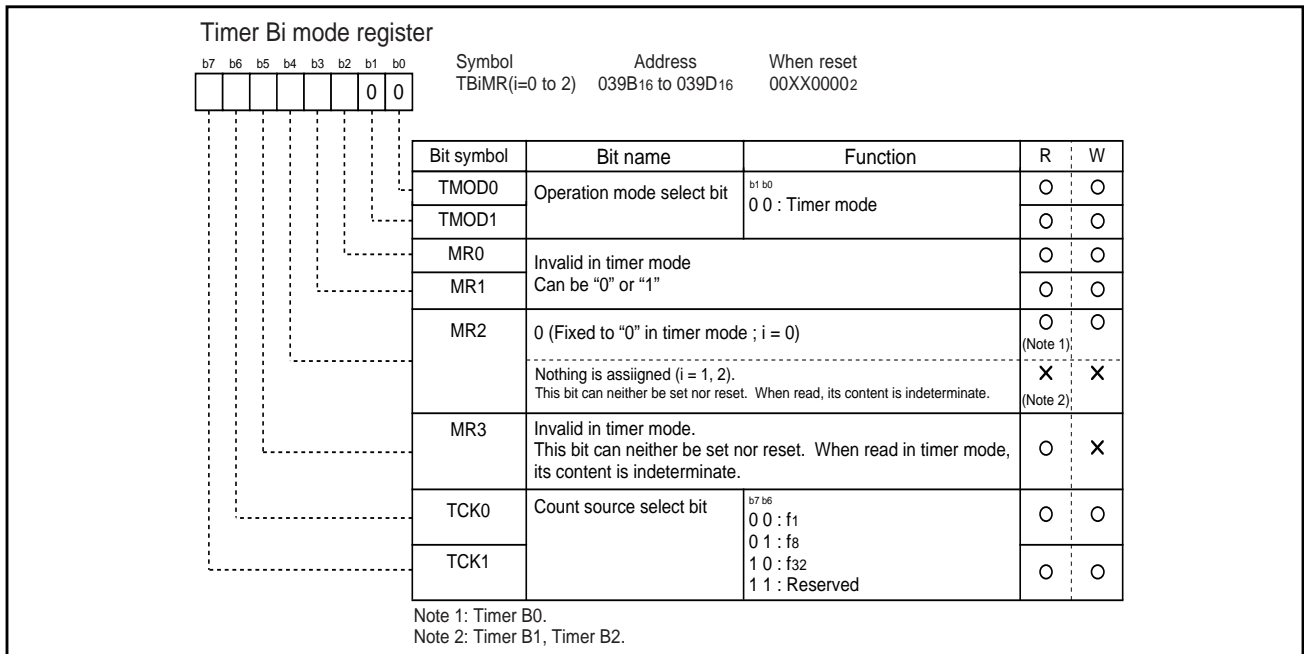


Figure 1.71: Timer B-related registers

Timer B

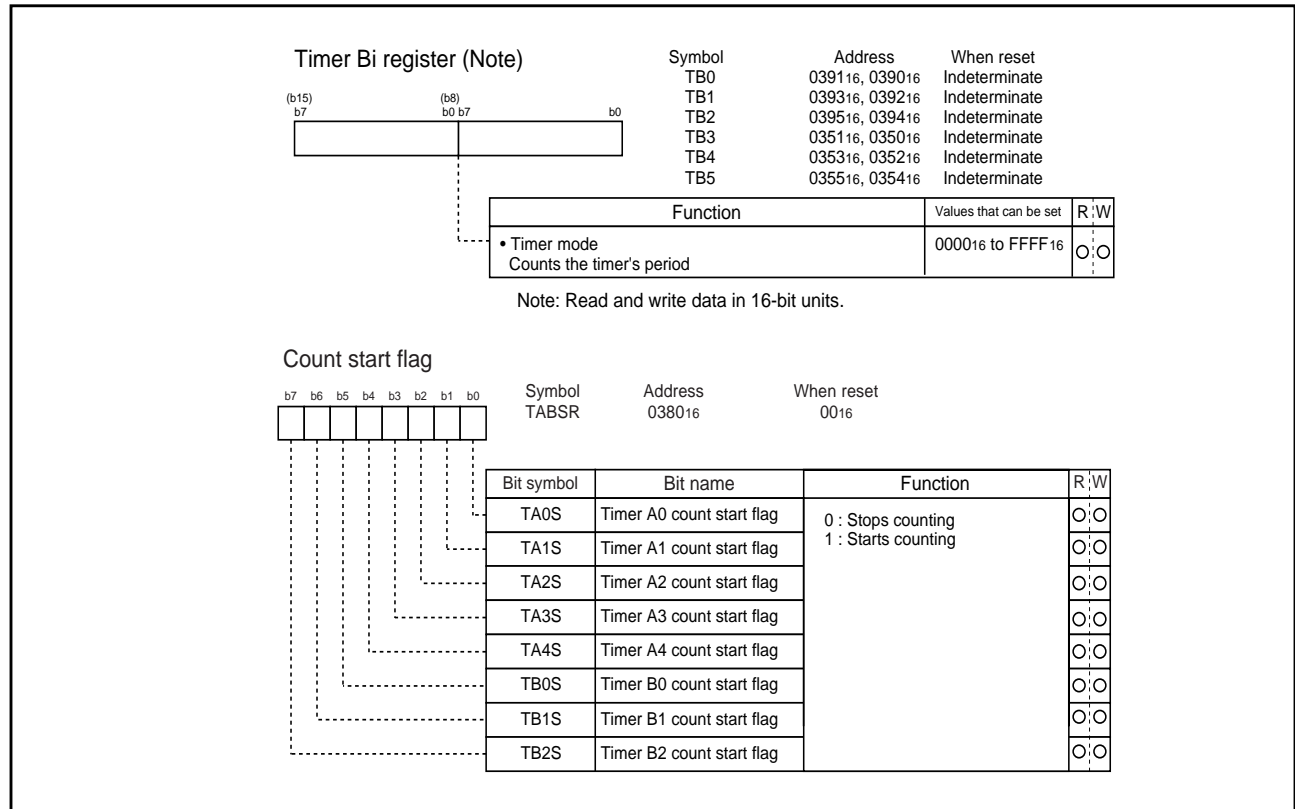


Figure 1.72: Timer B-related registers

2.22.1 Timer mode

In this mode, the timer counts an internally generated count source. (See Table 1.22) Figure 1.73 shows the Timer Bi mode register in timer mode.

Table 1.22: Timer specifications in timer mode

Item	Specification
Count source	f1, f8, f32
Count operation	•Counts down •When the timer underflows, it reloads the reload register contents before continuing counting
Divide ratio	1/(n+1) n: Set value
Count start condition	Count start flag is set (= 1)
Count stop condition	Count start flag is reset (= 0)
Interrupt request generation timing	The timer underflows (see Note)

Note: Timer B2 does not generate an interrupt; it is used only as a prescaler.

Timer B

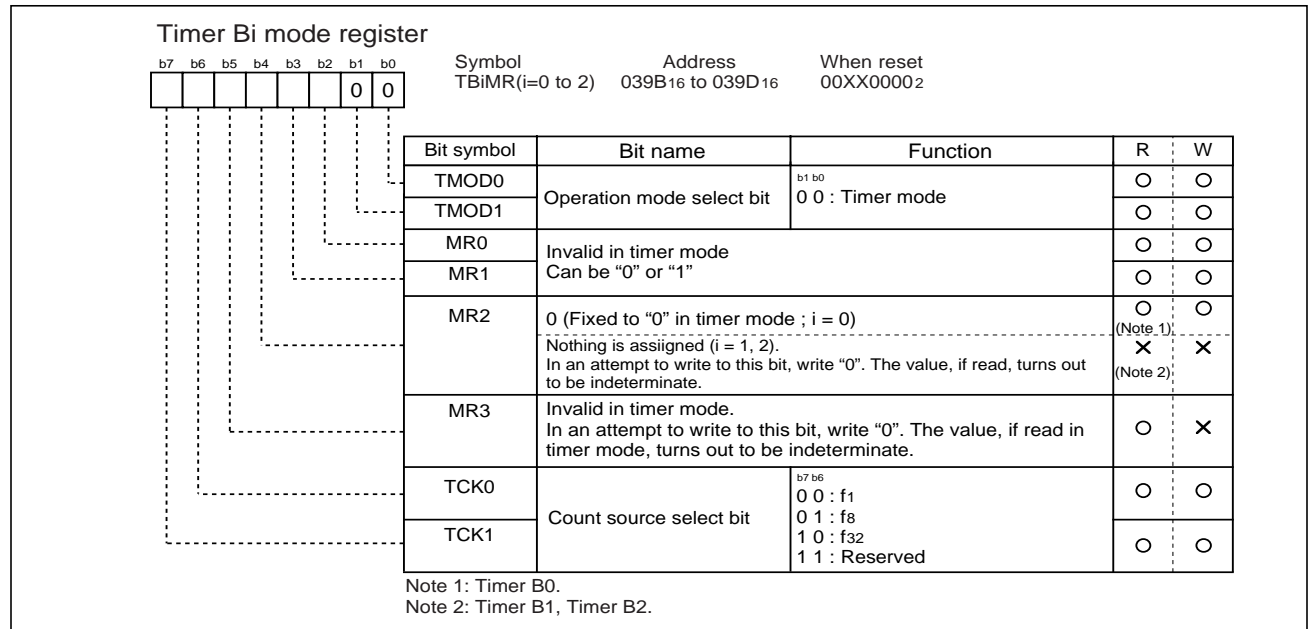


Figure 1.73: Timer Bi mode register in timer mode

UART0 through UART2

2.23 UART0 through UART2

Serial I/O is configured as three channels: UART0, UART1, and UART2. UART0, UART1, and UART2 each have an exclusive timer to generate a transfer clock, so they operate independently of each other.

Figure 1.74 shows the block diagram of UART0, UART1, and UART2.

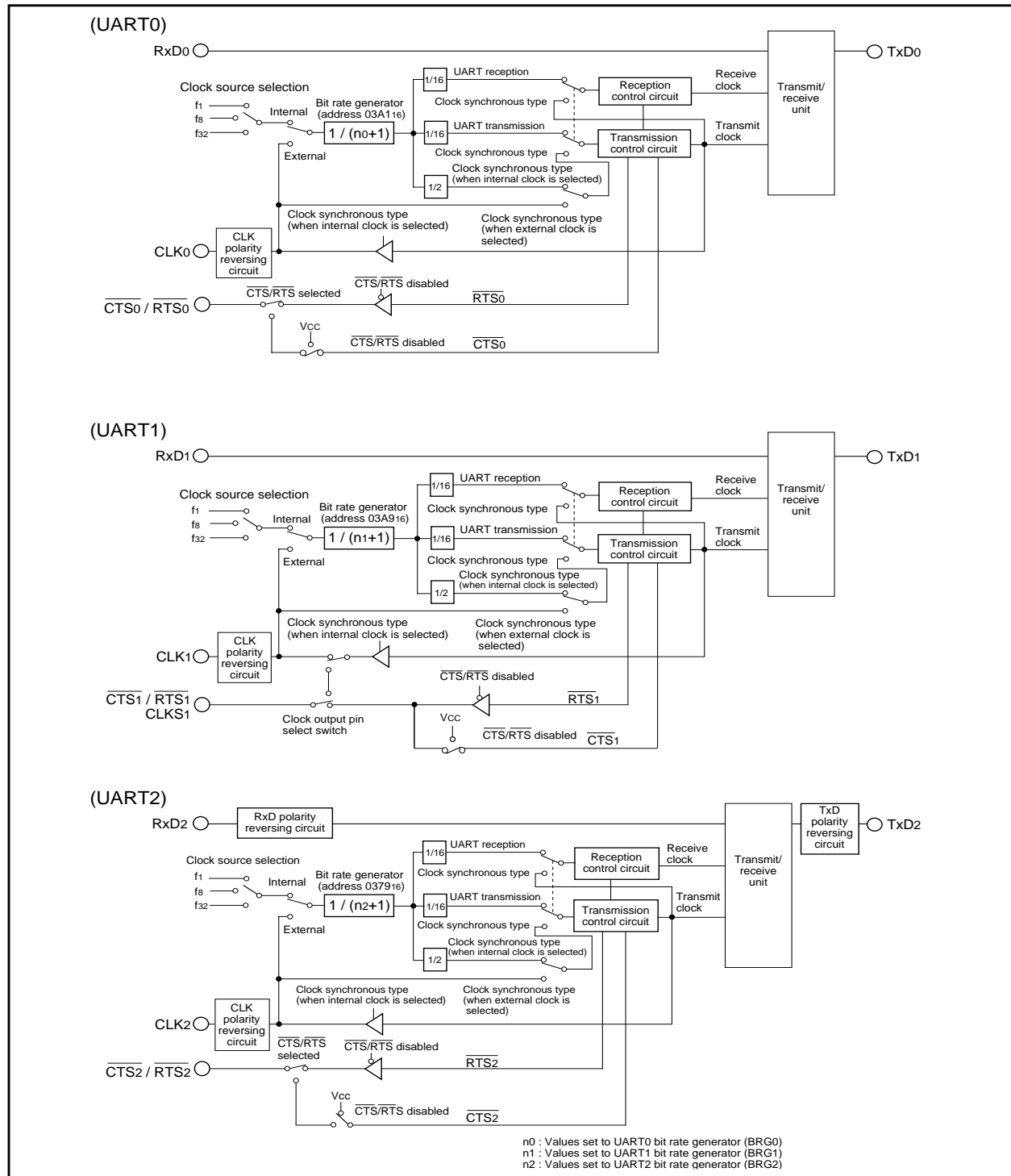


Figure 1.74: Block diagram of UARTi (i=0 to 2)

UART0 through UART2

Figure 1.75 and Figure 1.76 show the block diagram of the transmit/receive unit.

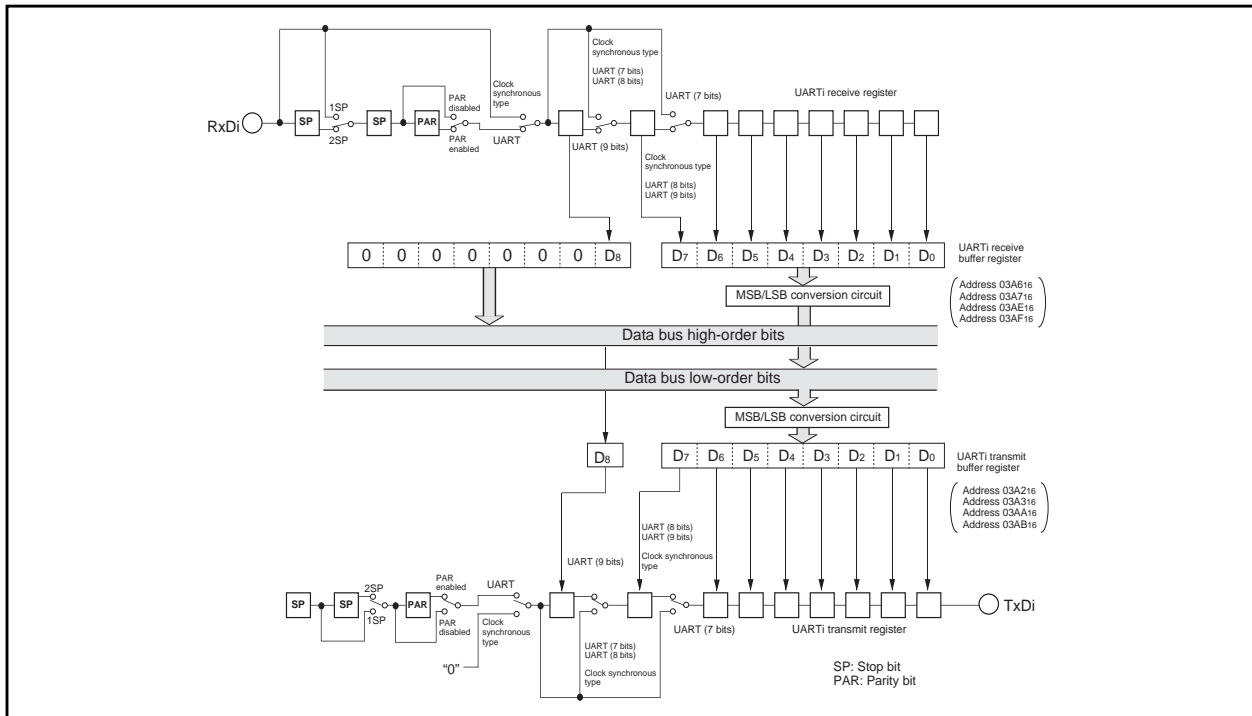


Figure 1.75: Block diagram of UARTi (i=0,1) transmit/receive circuit

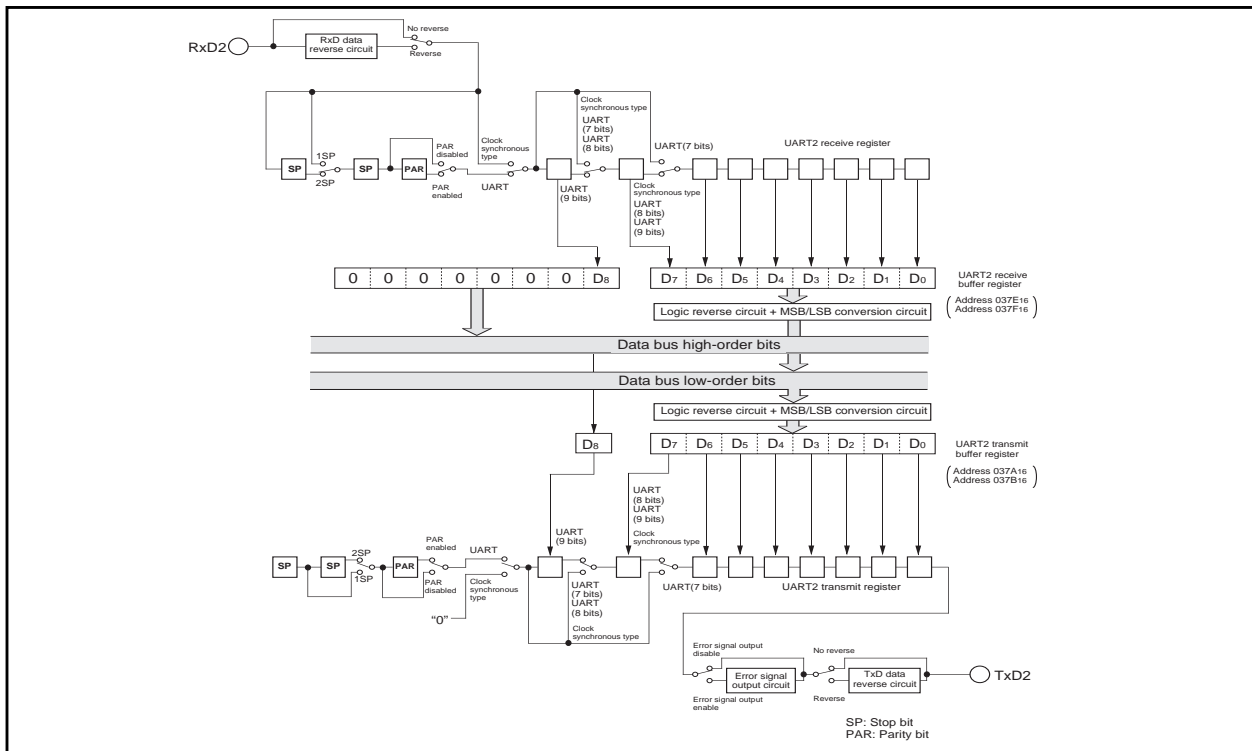


Figure 1.76: Block diagram of UART2 transmit/receive circuit



UART0 through UART2

UARTi (i = 0 to 2) has two operation modes: a clock synchronous serial I/O mode and a clock asynchronous serial I/O mode (UART mode). The contents of the serial I/O mode select bits (bits 0 to 2 at addresses 03A0₁₆, 03A8₁₆ and 0378₁₆) determine whether UARTi is used as a clock synchronous serial I/O or as a UART. Although a few functions are different, UART0 and UART1 have almost the same functions.

UART0 through UART2 are almost equal in their functions with minor exceptions. Table 1.23 shows the comparison of functions of UART0 through UART2, and Figure 1.77, Figure 1.78, Figure 1.79, Figure 1.80, and Figure 1.81 show the registers related to UARTi.

Table 1.23: Comparison of functions of UART0 through UART2

Function	UART0	UART1	UART2
CLK polarity selection	Possible (Note 1)	Possible (Note 1)	Possible (Note 1)
LSB first / MSB first selection	Possible (Note 1)	Possible (Note 1)	Possible (Note 2)
Continuous receive mode selection	Possible (Note 1)	Possible (Note 1)	Possible (Note 1)
Transfer clock output from multiple pins selection	Impossible	Possible (Note 1)	Impossible
Serial data logic switch	Impossible	Impossible	Possible (Note 4)
Sleep mode selection	Possible (Note 3)	Possible (Note 3)	Impossible
TxD, RxD I/O polarity switch	Impossible	Impossible	Possible
TxD, RxD port output format	CMOS output	CMOS output	CMOS output
Parity error signal output	Impossible	Impossible	Possible (Note 4)
Bus collision detection	Impossible	Impossible	Possible

Note 1: Only during clock synchronous serial I/O mode.

Note 2: Only during clock synchronous serial I/O mode and 8-bit UART mode.

Note 3: Only during UART mode.

Note 4: Used for SIM interface.

UART0 through UART2

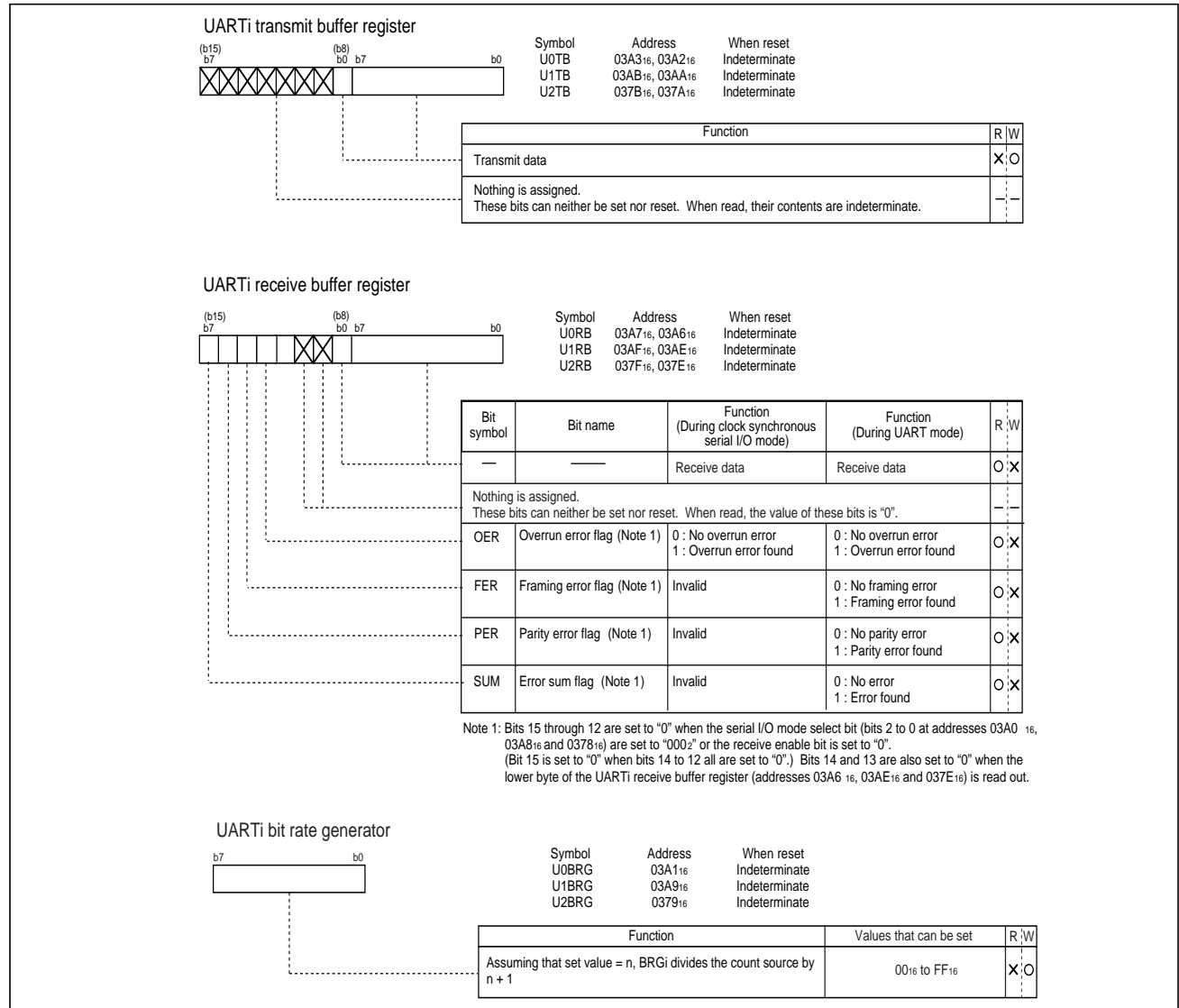


Figure 1.77: Serial I/O-related registers (1)

UART0 through UART2

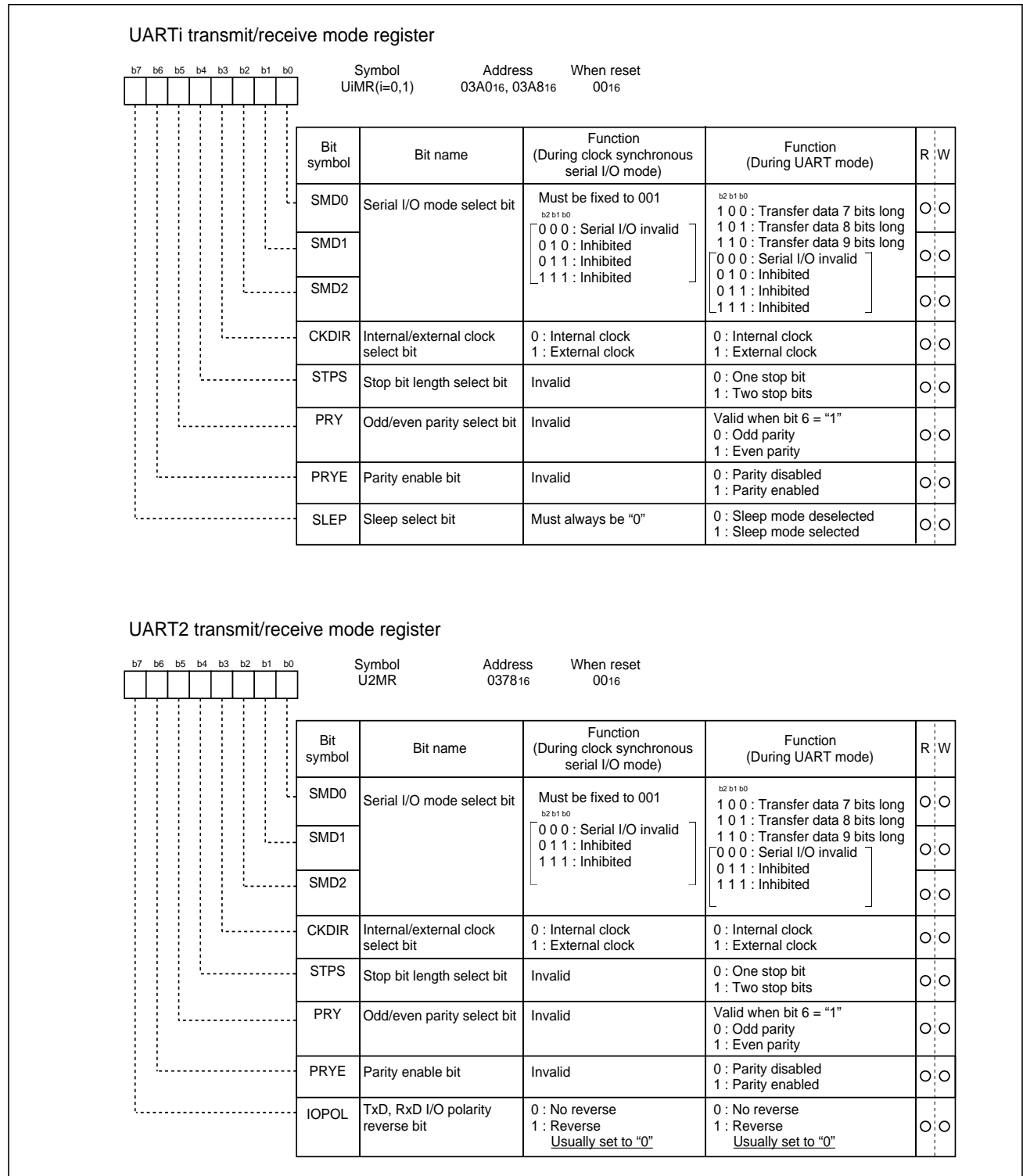


Figure 1.78: Serial I/O-related registers (2)

UART0 through UART2

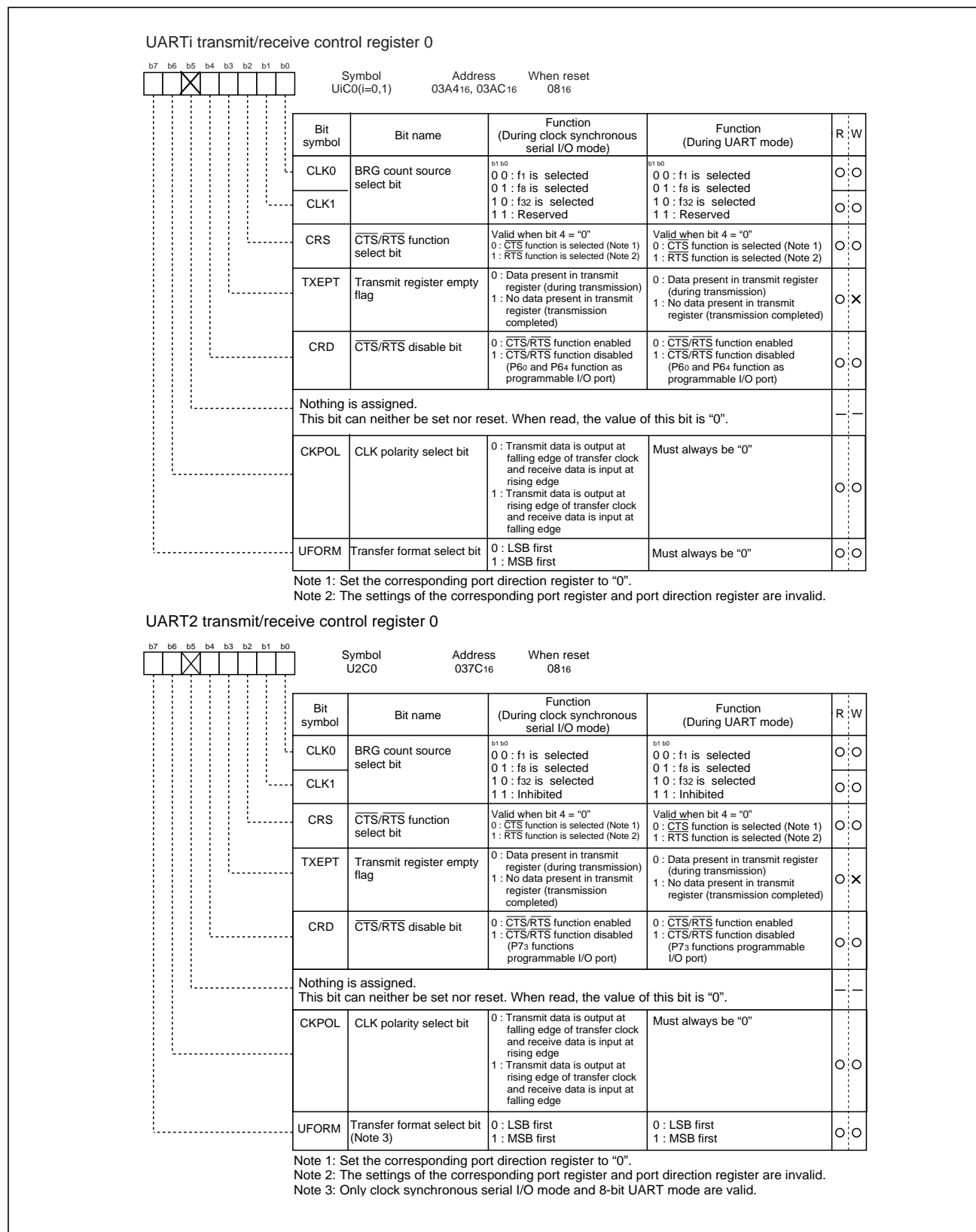


Figure 1.79: Serial I/O-related registers (3)

UART0 through UART2

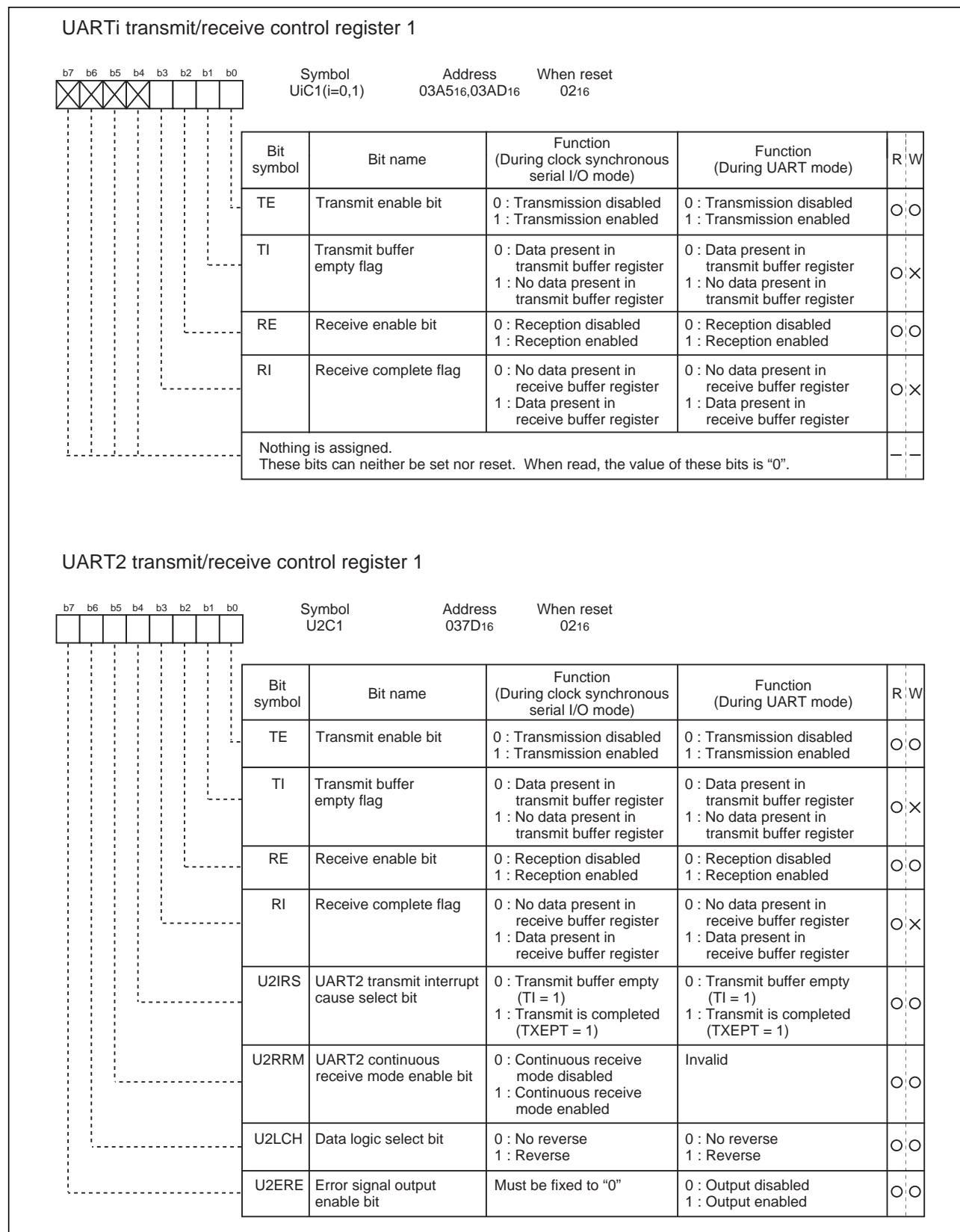


Figure 1.80: Serial I/O-related registers (4)



UART0 through UART2

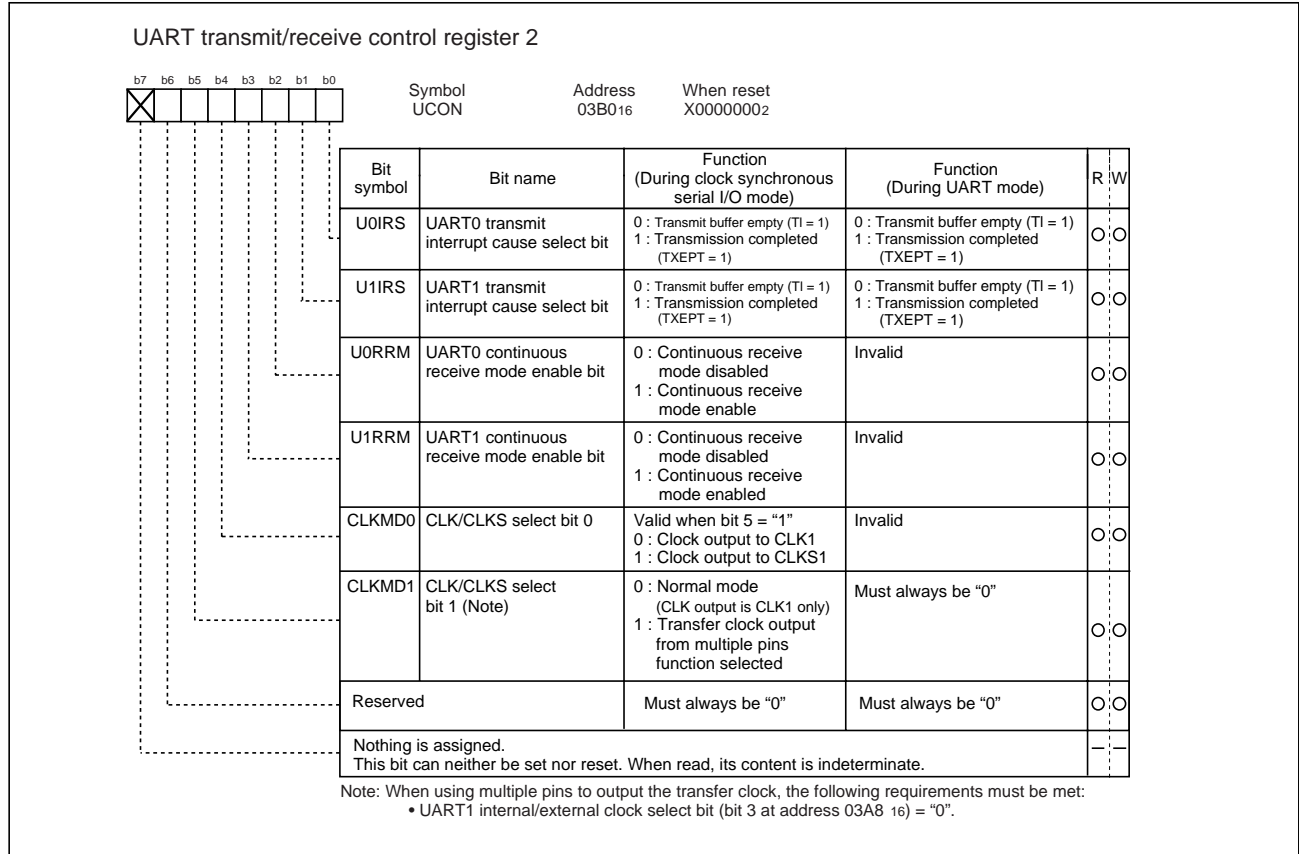


Figure 1.81: Serial I/O-related registers (5)



UART0 through UART2

2.23.1 Clock synchronous serial I/O mode

The clock synchronous serial I/O mode uses a transfer clock to transmit and receive data. Table 1.24 and Table 1.25 list the specifications of the clock synchronous serial I/O mode. Figure 1.82 shows the UARTi transmit/receive mode register.

Table 1.24: Specifications of clock synchronous serial I/O mode (1)

Item	Specification
Transfer data format	<ul style="list-style-type: none"> Transfer data length: 8 bits
Transfer clock	<ul style="list-style-type: none"> When internal clock is selected (bit 3 at addresses 03A0₁₆, 03A8₁₆, 0378₁₆ = "0"): $f_i = 2(n+1)$ (Note 1) $f_i = f_1, f_8, f_{32}$ When external clock is selected (bit 3 at addresses 03A0₁₆, 03A8₁₆, 0378₁₆ = "1"): Input from CLKi pin (Note 2)
Transmission/reception control	<ul style="list-style-type: none"> CTS function/RTS function/CTS, RTS function chosen to be invalid
Transmission start condition	<ul style="list-style-type: none"> To start transmission, the following requirements must be met: <ul style="list-style-type: none"> Transmit enable bit (bit 0 at addresses 03A5₁₆, 03AD₁₆, 037D₁₆) = "1" Transmit buffer empty flag (bit 1 at addresses 03A5₁₆, 03AD₁₆, 037D₁₆) = "0" When CTS function selected, CTS input level = "L" Furthermore, if external clock is selected, the following requirements must also be met: <ul style="list-style-type: none"> CLKi polarity select bit (bit 6 at addresses 03A4₁₆, 03AC₁₆, 037C₁₆) = "0": CLKi input level = "H" CLKi polarity select bit (bit 6 at addresses 03A4₁₆, 03AC₁₆, 037C₁₆) = "1": CLKi input level = "L"
Reception start condition	<ul style="list-style-type: none"> To start reception, the following requirements must be met: <ul style="list-style-type: none"> Receive enable bit (bit 2 at addresses 03A5₁₆, 03AD₁₆, 037D₁₆) = "1" Transmit enable bit (bit 0 at addresses 03A5₁₆, 03AD₁₆, 037D₁₆) = "1" Transmit buffer empty flag (bit 1 at addresses 03A5₁₆, 03AD₁₆, 037D₁₆) = "0" Furthermore, if external clock is selected, the following requirements must also be met: <ul style="list-style-type: none"> CLKi polarity select bit (bit 6 at addresses 03A4₁₆, 03AC₁₆, 037C₁₆) = "0": CLKi input level = "H" CLKi polarity select bit (bit 6 at addresses 03A4₁₆, 03AC₁₆, 037C₁₆) = "1": CLKi input level = "L" When transmitting <ul style="list-style-type: none"> Transmit interrupt cause select bit (bits 0, 1 at address 03B0₁₆, bit 4 at address 037D₁₆) = "0": Interrupts requested when data transfer from UARTi Transmit interrupt cause select bit (bits 0, 1 at address 03B0₁₆, bit 4 at address 037D₁₆) = "1": Interrupts requested when data transmission from
Error detection	<ul style="list-style-type: none"> Overrun error (Note 3) This error occurs when the next data is ready before contents of UARTi receive buffer is read.

Note 1: "n" denotes the value 00₁₆ to FF₁₆ that is set to the UART bit rate generator.

Note 2: Maximum 5 Mbps.

Note 3: If an overrun error occurs, the UARTi receive buffer will have the next data written in. Note also that the UARTi receive interrupt request bit is not set to "1".

UART0 through UART2

Table 1.25: Specifications of clock synchronous serial I/O mode (2)

Item	Specification
Select function	<ul style="list-style-type: none"> • CLK polarity selection Whether transmit data is output/input at the rising edge or falling edge of the transfer clock can be selected • LSB first/MSB first selection Whether transmission/reception begins with bit 0 or bit 7 can be selected • Continuous receive mode selection Reception is enabled simultaneously by a read from the receive buffer register • Transfer clock output from multiple pins selection (UART1) UART1 transfer clock can be chosen by software to be output from one of the two pins set • Switching serial data logic (UART2) Whether to reverse data in writing to the transmission buffer register or reading the reception buffer register can be selected. • Switching serial data logic (UART2) This function is reversing TxD port output and RxD port input. All I/O data level is reversed.

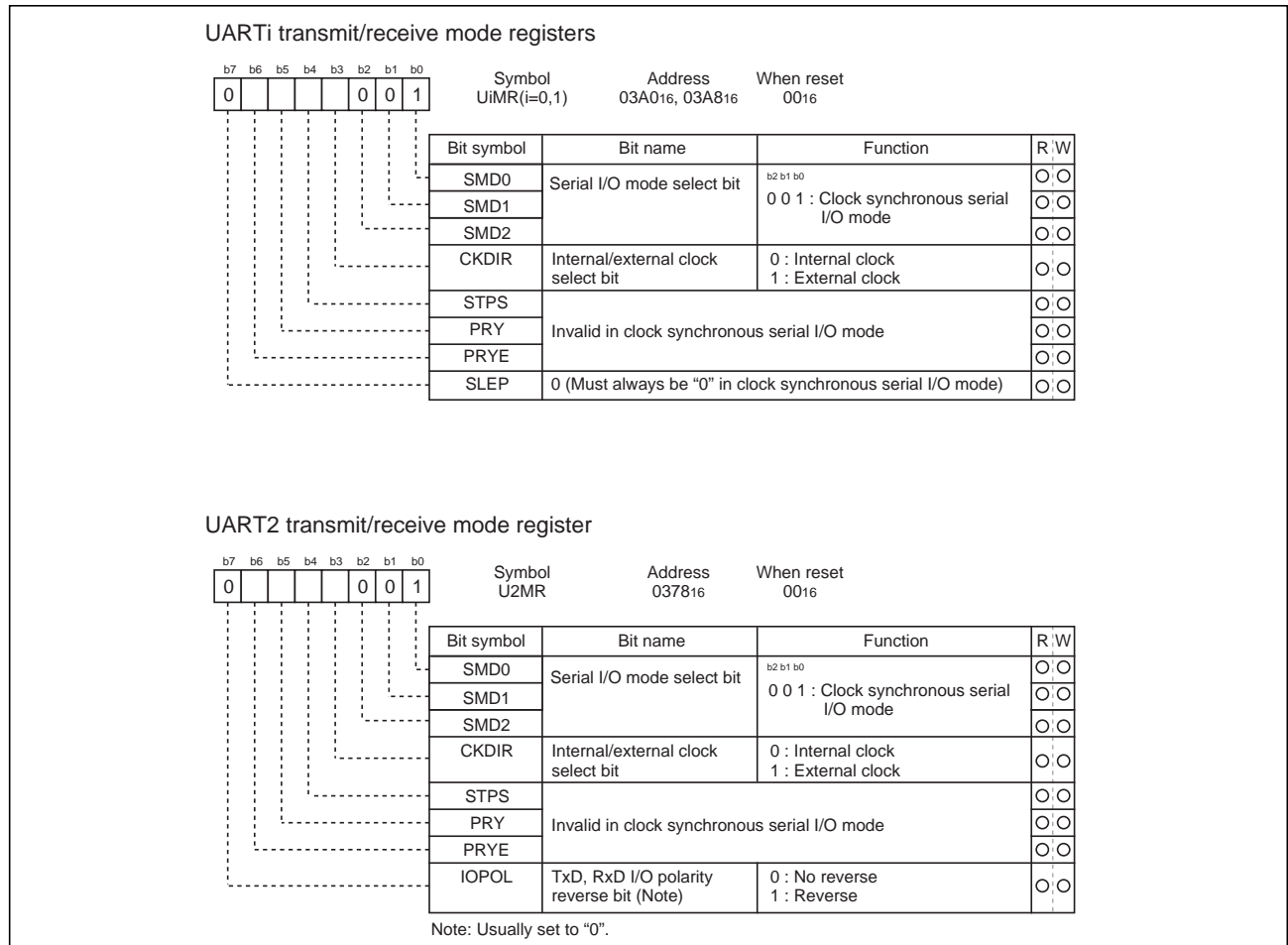


Figure 1.82: UARTi transmit/receive mode register in clock synchronous serial I/O mode



UART0 through UART2

Table 1.26 lists the functions of the input/output pins during clock synchronous serial I/O mode. This table shows the pin functions when the transfer clock output from multiple pins function is not selected. Note that for a period from when the UARTi operation mode is selected to when transfer starts, the TxD pin outputs a "H". The typical clock synchronous timing diagrams are shown in Figure 1.83.

Table 1.26: Input/output pin functions in clock synchronous serial I/O mode

Pin name	Function	Method of selection
TxDi (P63, P67, P70)	Serial data output	(Outputs dummy data when performing reception only)
RxDi (P62, P66, P71)	Serial data input	Port P62, P66, and P71 direction register (bits 2 and 6 at address 03EE ₁₆ , bit 1 at address 03EF ₁₆) = "0" (Can be used as an input port when performing transmission only.)
CLKi (P61, P65, P72)	Transfer clock output	Internal/external clock select bit (bit 3 at address 03A0 ₁₆ , 03A8 ₁₆ , 0378 ₁₆) = "0"
	Transfer clock input	Internal/external clock select bit (bit 3 at address 03A0 ₁₆ , 03A8 ₁₆ , 0378 ₁₆) = "1" Port P61, P65, and P72 direction register (bits 1 and 5 at address 03EE ₁₆ , bit 2 at address 03EF ₁₆) = "0"
CTS _i /RTS _i (P60, P64, P73)	$\overline{\text{CTS}}$ input	$\overline{\text{CTS}}/\text{RTS}$ disable bit (bit 4 at address 03A4 ₁₆ , 03AC ₁₆ , 037C ₁₆) = "0" $\overline{\text{CTS}}/\text{RTS}$ function select bit (bit 2 at address 03A4 ₁₆ , 03AC ₁₆ , 037C ₁₆) = "0" Port P60, P64 and P73 direction register (bits 0 and 4 at address 03EE ₁₆ , bit 3 at address 03EF ₁₆) = "0"
	$\overline{\text{RTS}}$ output	$\overline{\text{CTS}}/\text{RTS}$ disable bit (bit 4 at address 03A4 ₁₆ , 03AC ₁₆ , 037C ₁₆) = "0" $\overline{\text{CTS}}/\text{RTS}$ function select bit (bit 2 at address 03A4 ₁₆ , 03AC ₁₆ , 037C ₁₆) = "1"
	Programmable I/O port	$\overline{\text{CTS}}/\text{RTS}$ disable bit (bit 4 at address 03A4 ₁₆ , 03AC ₁₆ , 037C ₁₆) = "1"

UART0 through UART2

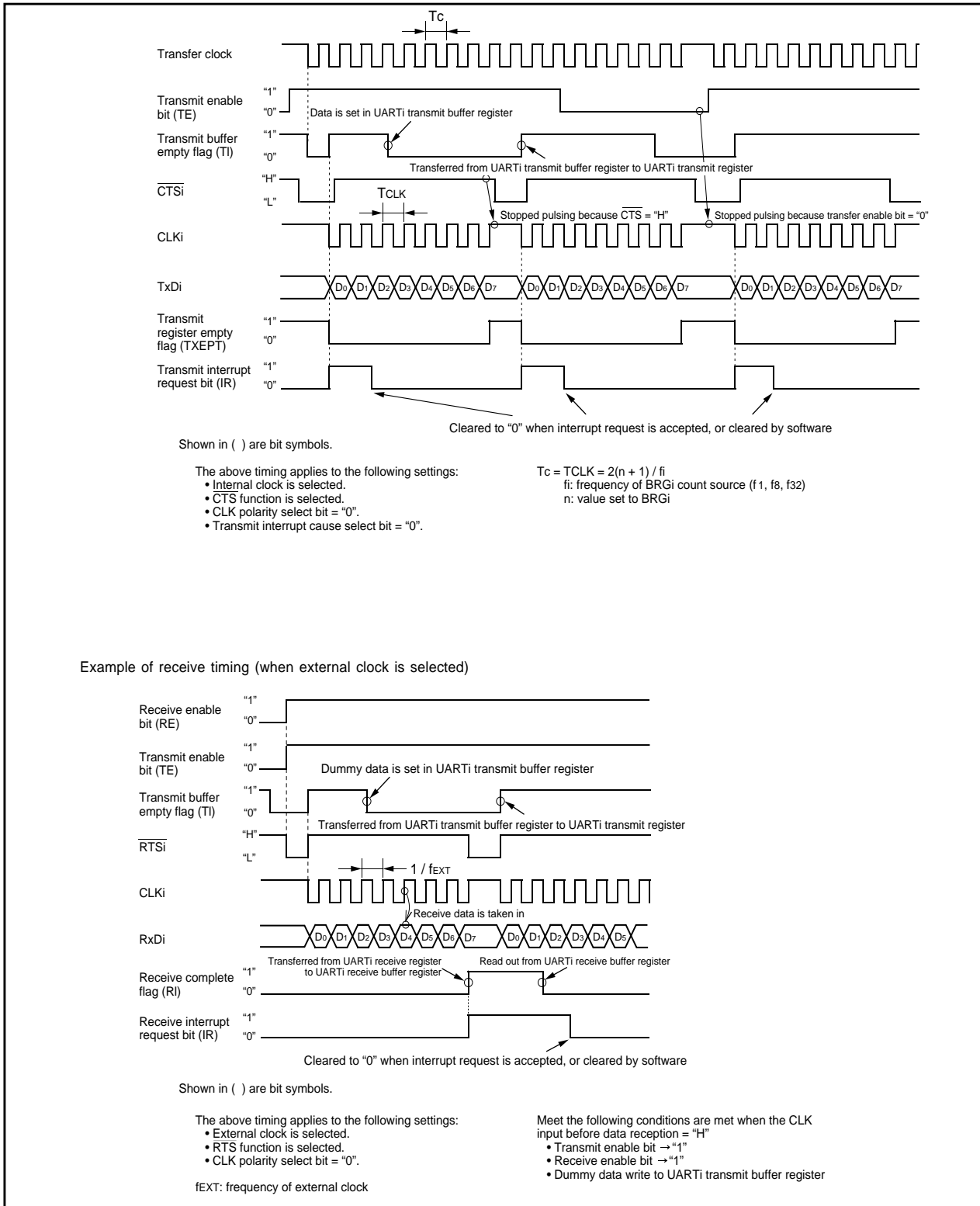


Figure 1.83: Typical transmit/receive timings in clock synchronous serial I/O mode Polarity select function

UART0 through UART2

2.23.1.1 Polarity select function

As shown in Figure 1.84, the CLK polarity select bit (bit 6 at addresses 03A4₁₆, 03AC₁₆, 037C₁₆) allows selection of the polarity of the transfer clock.

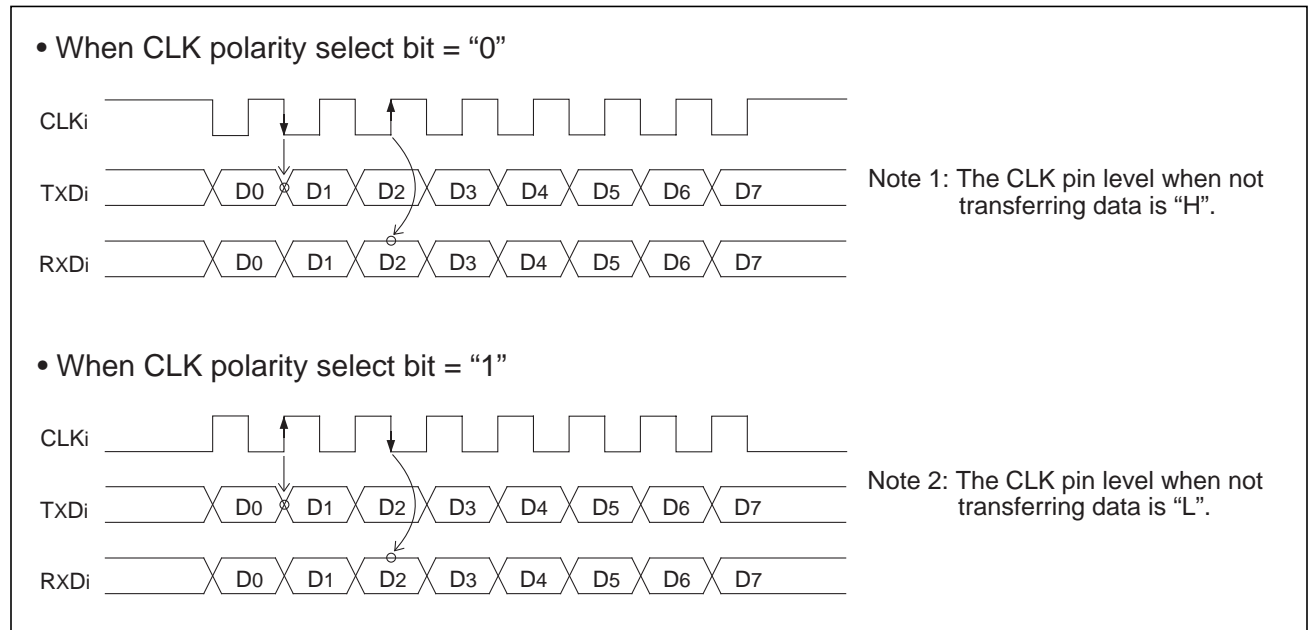


Figure 1.84: Polarity of transfer clock

2.23.1.2 LSB first/MSB first select function

As shown in Figure 1.85, when the transfer format select bit (bit 7 at addresses 03A4₁₆, 03AC₁₆, 037C₁₆) = "0", the transfer format is "LSB first"; when the bit = "1", the transfer format is "MSB first".

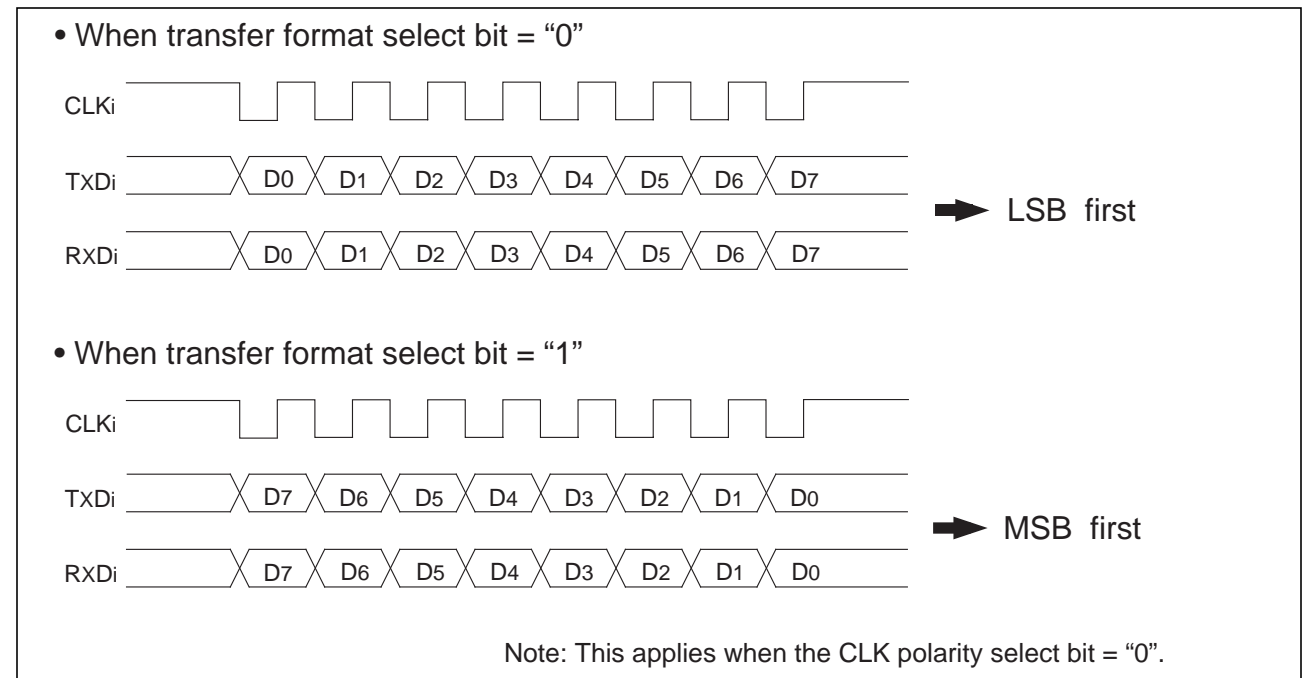


Figure 1.85: Transfer format

UART0 through UART2

2.23.1.3 Transfer clock output from multiple pins function (UART1)

This function allows the setting two transfer clock output pins and choosing one of the two to output a clock by using the CLK and CLKS select bit (bits 4 and 5 at address 03B0₁₆). See Figure 1.86. The multiple pins function is valid only when the internal clock is selected for UART1. Note that when this function is selected, UART1 CTS/RTS function cannot be used.

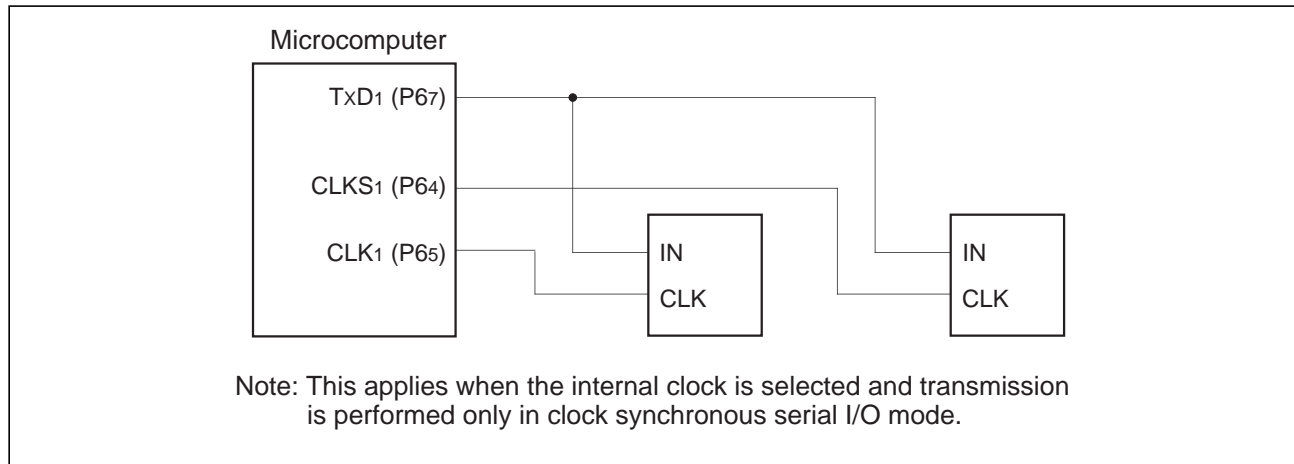


Figure 1.86: The transfer clock output from the multiple pins function usage

2.23.1.4 Continuous receive mode

If the continuous receive mode enable bit (bits 2 and 3 at address 03B0₁₆, bit 5 at address 037D₁₆) is set to "1", the unit is placed in continuous receive mode. In this mode, when the receive buffer register is read out, the unit simultaneously goes to a receive enable state without having to set dummy data to the transmit buffer register back again.

2.23.1.5 Serial data logic switch function (UART2)

When the data logic select bit (bit6 at address 037D₁₆) = "1", and writing to transmit buffer register or reading from receive buffer register, data is reversed. Figure 1.87 shows the example of serial data logic switch timing.

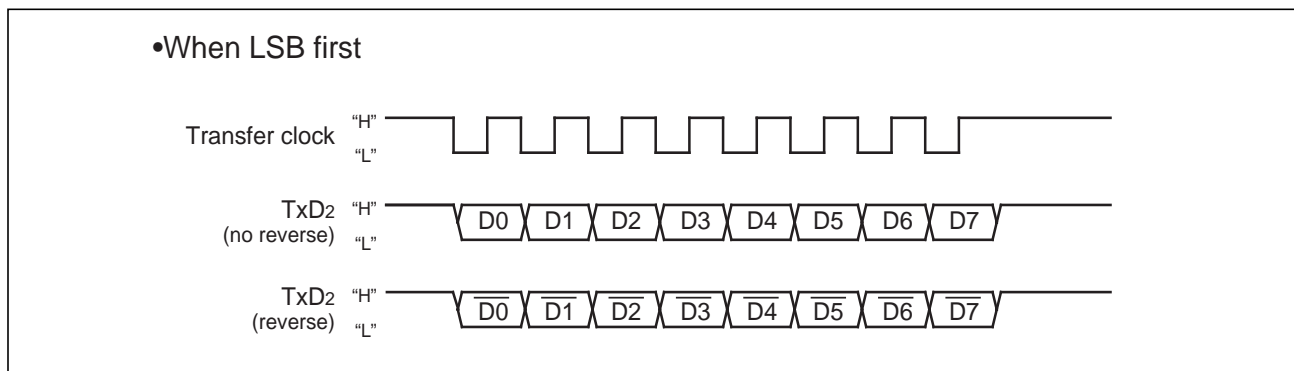


Figure 1.87: Serial data logic switch timing

UART0 through UART2

2.23.2 Clock asynchronous serial I/O (UART) mode

The UART mode allows transmitting and receiving data after setting the desired transfer rate and transfer data format. Table 1.27 and Table 1.28 list the specifications of the UART mode. Figure 1.88 shows the UARTi transmit/receive mode register.

Table 1.27: Specifications of UART Mode (1)

Item	Specification
Transfer data format	<ul style="list-style-type: none"> • Character bit (transfer data): 7 bits, 8 bits, or 9 bits as selected • Start bit: 1 bit • Parity bit: Odd, even, or nothing as selected • Stop bit: 1 bit or 2 bits as selected
Transfer clock	<ul style="list-style-type: none"> • When internal clock is selected (bit 3 at addresses 03A0₁₆, 03A8₁₆, 0378₁₆ = "0"): $f_i/16(n+1)$ (Note 1) $f_i = f_1, f_8, f_{32}$ • When external clock is selected (bit 3 at addresses 03A0₁₆, 03A8₁₆, 0378₁₆ = "1"): $f_{EXT}/16(n+1)$(Note 1) (Note 2)
Transmission/reception control	<ul style="list-style-type: none"> • CTS function/RTS function/CTS, RTS function chosen to be invalid
Transmission start condition	<ul style="list-style-type: none"> • To start transmission, the following requirements must be met: <ul style="list-style-type: none"> - Transmit enable bit (bit 0 at addresses 03A5₁₆, 03AD₁₆, 037D₁₆) = "1" - Transmit buffer empty flag (bit 1 at addresses 03A5₁₆, 03AD₁₆, 037D₁₆) = "0" - When CTS function selected, CTS input level = "L"
Reception start condition	<ul style="list-style-type: none"> • To start reception, the following requirements must be met: <ul style="list-style-type: none"> - Receive enable bit (bit 2 at addresses 03A5₁₆, 03AD₁₆, 037D₁₆) = "1" - Start bit detection
Interrupt request generation timing	<ul style="list-style-type: none"> • When transmitting <ul style="list-style-type: none"> - Transmit interrupt cause select bits (bits 0,1 at address 03B0₁₆, bit4 at address 037D₁₆) = "0": Interrupts requested when data transfer from UARTi transfer buffer register to UARTi transmit register is completed - Transmit interrupt cause select bits (bits 0, 1 at address 03B0₁₆, bit4 at address 037D₁₆) = "1": Interrupts requested when data transmission from UARTi transfer register is completed • When receiving <ul style="list-style-type: none"> - Interrupts requested when data transfer from UARTi receive register to UARTi receive buffer register is completed
Error detection	<ul style="list-style-type: none"> • Overrun error (Note 3) This error occurs when the next data is ready before contents of UARTi receive buffer register are read out • Framing error This error occurs when the number of stop bits set is not detected • Parity error This error occurs when if parity is enabled, the number of 1's in parity and character bits does not match the number of 1's set • Error sum flag This flag is set (= 1) when any of the overrun, framing, and parity errors is encountered

Note 1: 'n' denotes the value 00₁₆ to FF₁₆ that is set to the UARTi bit rate generator.

Note 2: fEXT is input from the CLKi pin.

Note 3: If an overrun error occurs, the UARTi receive buffer will have the next data written in. Note also that the UARTi receive interrupt request bit is not set to "1"

UART0 through UART2

Table 1.28: Specifications of UART Mode (2)

Item	Specification
Select function	<ul style="list-style-type: none"> • Sleep mode selection (UART0, UART1) This mode is used to transfer data to and from one of multiple slave micro-computers • Serial data logic switch (UART2) This function is reversing logic value of transferring data. Start bit, parity bit and stop bit are not reversed. • TxD, RxD I/O polarity switch This function is reversing TxD port output and RxD port input. All I/O data level is reversed.

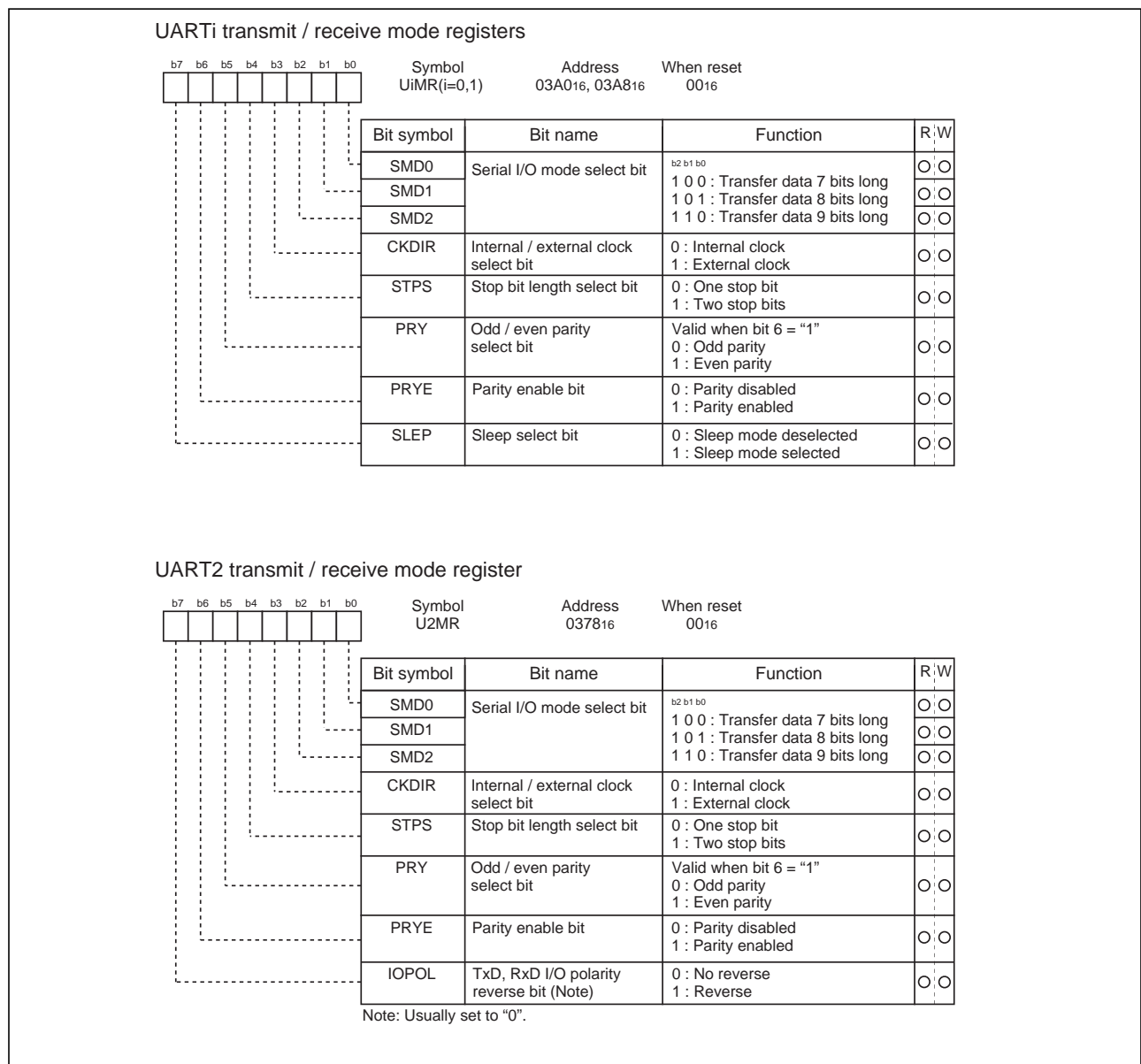


Figure 1.88: UARTi transmit/receive mode register in UART mode



UART0 through UART2

Table 1.29 lists the functions of the input/output pins during UART mode. Note that for a period from when the UARTi operation mode is selected to when transfer starts, the TxDi pin outputs a "H".

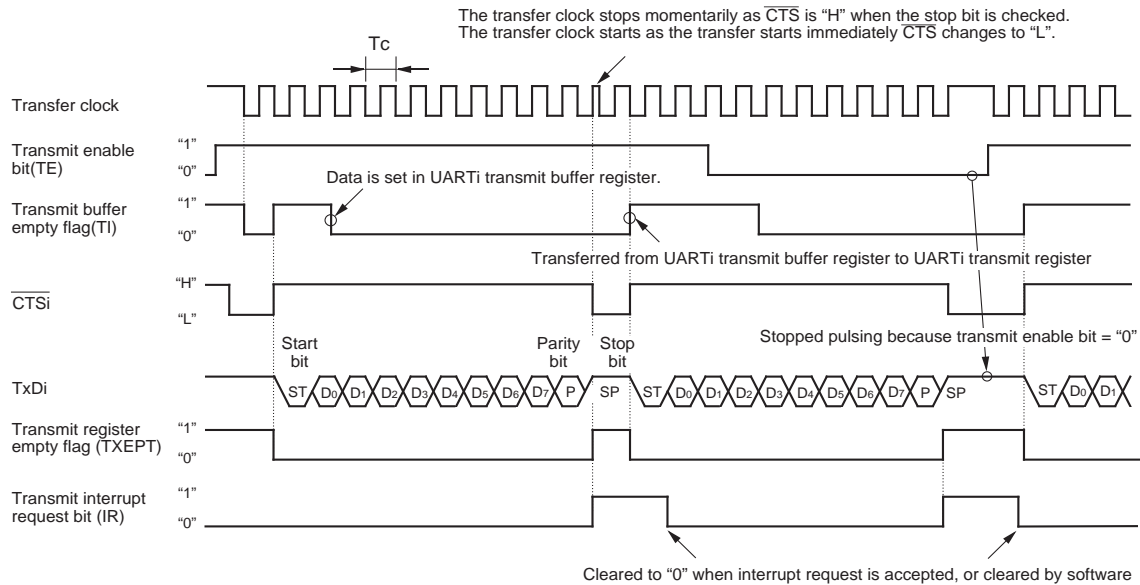
Table 1.29: Input/output pin functions in UART mode

Pin name	Function	Method of selection
TxDi (P63, P67, P70)	Serial data output	
RxDi (P62, P66, P71)	Serial data input	Port P62, P66, and P71 direction register (bits 2 and 6 at address 03EE ₁₆ bit 1 at address 03EF ₁₆) = "0" (Can be used as an input port when performing transmission only.)
CLKi (P61, P65, P72)	Programmable I/O port	Internal/external clock select bit (bit 3 at address 03A0 ₁₆ , 03A8 ₁₆ , 0378 ₁₆) = "0"
	Transfer clock input	Internal/external clock select bit (bit 3 at address 03A0 ₁₆ , 03A8 ₁₆ , 0378 ₁₆) = "1" Port P61, P65, and P72 direction register (bits 1 and 5 at address 03EE ₁₆ , bit 2 at address 03EF ₁₆) = "0"
$\overline{\text{CTS}}_i/\overline{\text{RTS}}_i$ (P60, P64, P73)	$\overline{\text{CTS}}$ input	$\overline{\text{CTS}}/\overline{\text{RTS}}$ disable bit (bit 4 at address 03A4 ₁₆ , 03AC ₁₆ , 037C ₁₆) = "0" $\overline{\text{CTS}}/\overline{\text{RTS}}$ function select bit (bit 2 at address 03A4 ₁₆ , 03AC ₁₆ , 037C ₁₆) = "0" Port P60, P64 and P73 direction register (bits 0 and 4 at address 03EE ₁₆ , bit 3 at address 03EF ₁₆) = "0"
	$\overline{\text{RTS}}$ output	$\overline{\text{CTS}}/\overline{\text{RTS}}$ disable bit (bit 4 at address 03A4 ₁₆ , 03AC ₁₆ , 037C ₁₆) = "0" $\overline{\text{CTS}}/\overline{\text{RTS}}$ function select bit (bit 2 at address 03A4 ₁₆ , 03AC ₁₆ , 037C ₁₆) = "1"
	Programmable I/O port	$\overline{\text{CTS}}/\overline{\text{RTS}}$ disable bit (bit 4 at address 03A4 ₁₆ , 03AC ₁₆ , 037C ₁₆) = "1"

Figure 1.89 and Figure 1.90 show the typical UART mode transmit and receive timing diagrams.

UART0 through UART2

• Example of transmit timing when transfer data is 8 bits long (parity enabled, one stop bit)



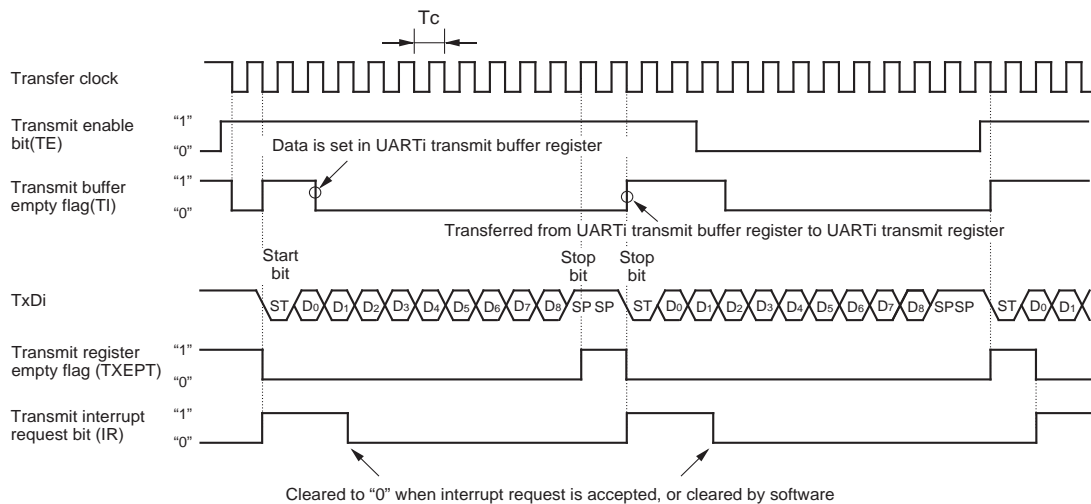
Shown in () are bit symbols.

- The above timing applies to the following settings :
- Parity is enabled.
 - One stop bit.
 - CTS function is selected.
 - Transmit interrupt cause select bit = "1".

$$T_c = 16(n + 1) / f_i \text{ or } 16(n + 1) / f_{EXT}$$

f_i : frequency of BRGi count source (f_1, f_8, f_{32})
 f_{EXT} : frequency of BRGi count source (external clock)
 n : value set to BRGi

• Example of receive timing when transfer data is 8 bits long (parity enabled, one stop bit)



Shown in () are bit symbols.

- The above timing applies to the following settings :
- Parity is disabled.
 - Two stop bits.
 - CTS function is disabled.
 - Transmit interrupt cause select bit = "0".

$$T_c = 16(n + 1) / f_i \text{ or } 16(n + 1) / f_{EXT}$$

f_i : frequency of BRGi count source (f_1, f_8, f_{32})
 f_{EXT} : frequency of BRGi count source (external clock)
 n : value set to BRGi

Figure 1.89: Typical transmit timings in UART mode

UART0 through UART2

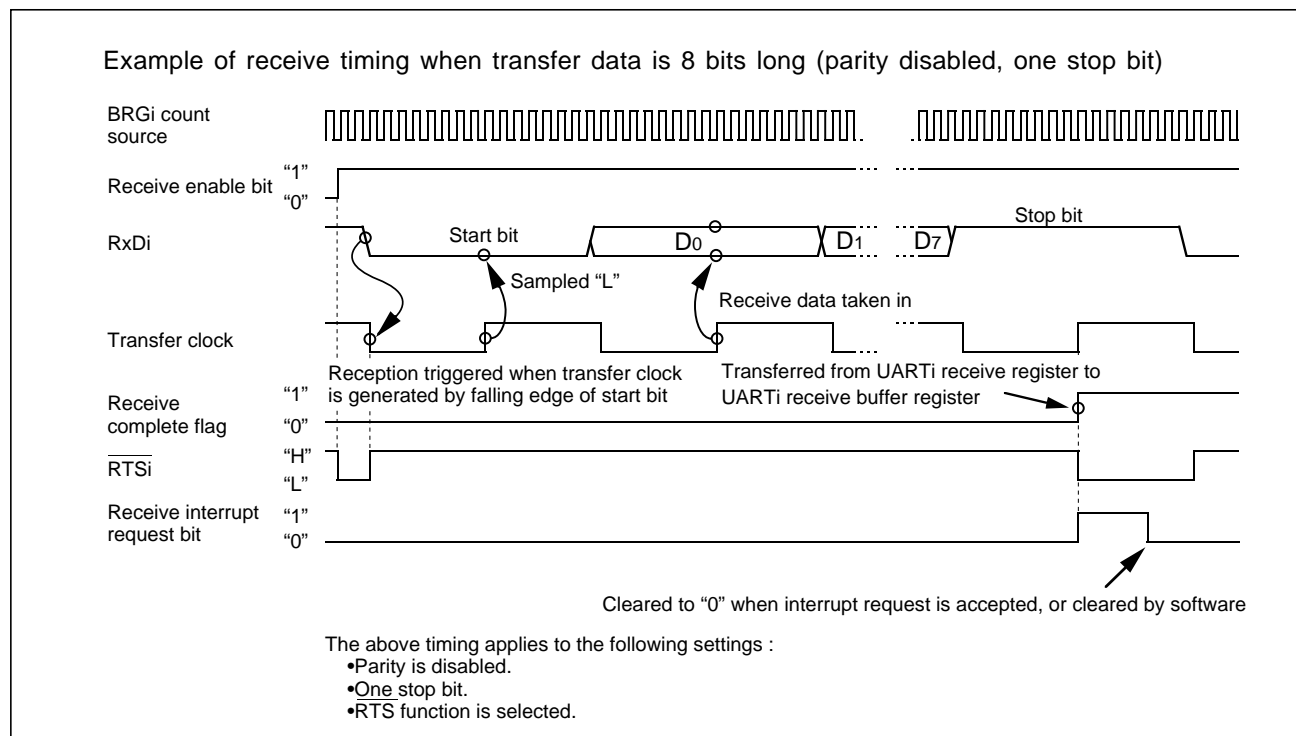


Figure 1.90: Typical receive timing in UART mode

2.23.2.1 Sleep mode (UART0, UART1)

This mode is used to transfer data between specific microcomputers among multiple microcomputers connected using UARTi. The sleep mode is selected when the sleep select bit (bit 7 at addresses 03A0₁₆, 03A8₁₆) is set to "1" during reception. In this mode, the unit performs receive operation when the MSB of the received data = "1" and does not perform receive operation when the MSB = "0".

2.23.2.2 Function for switching serial data logic (UART2)

When the data logic select bit (bit 6 of address 037D₁₆) is assigned 1, data is inverted in writing to the transmission buffer register or reading the reception buffer register. Figure 1.91 shows the example of timing for switching serial data logic.

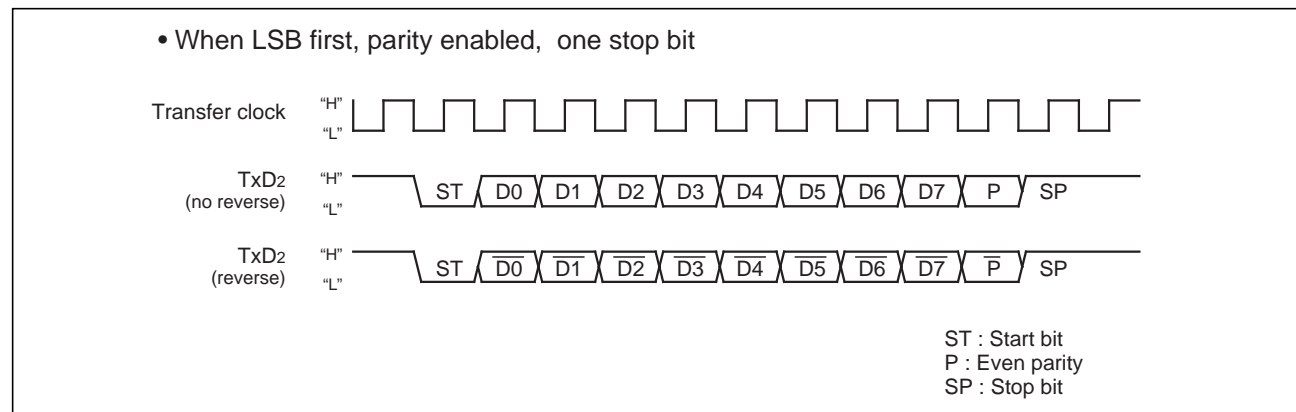


Figure 1.91: Timing for switching serial data logic

UART0 through UART2

2.23.2.3 TxD, RxD I/O polarity reverse function (UART2)

This function is to reverse TxD pin output and RxD pin input. The level of any data to be input or output (including the start bit, stop bit(s), and parity bit) is reversed. Set this function to "0" (not to reverse) for usual use.

2.23.2.4 Bus collision detection function (UART2)

This function is to sample the output level of the TxD pin and the input level of the RxD pin at the rising edge of the transfer clock; if their values are different, then an interrupt request occurs. Figure 1.92 shows the example of detection timing of a buss collision (in UART mode).

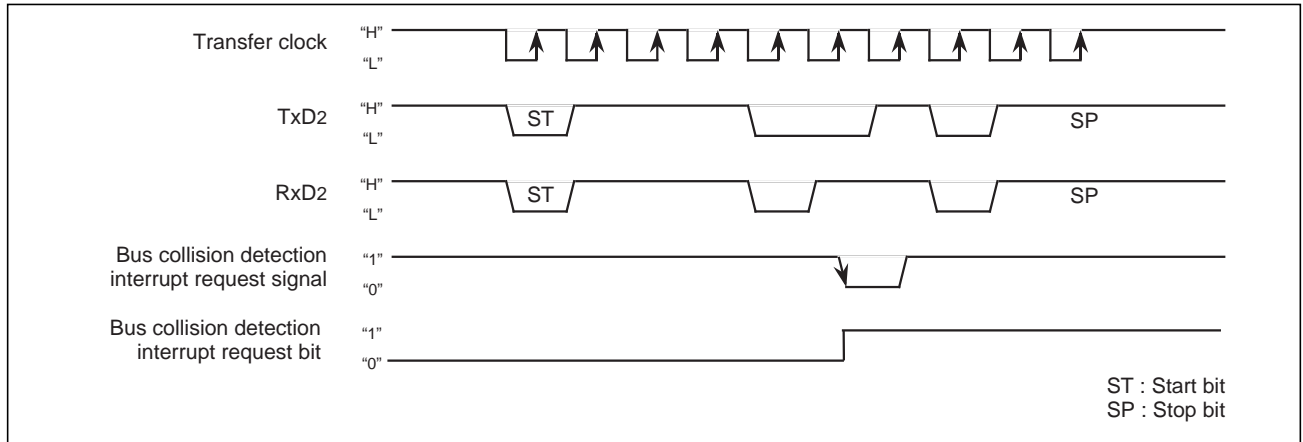


Figure 1.92: Detection timing of a bus collision (in UART mode)



UART0 through UART2

2.23.3 Clock-asynchronous serial I/O mode (compliant with the SIM interface)

The SIM interface is used for connecting the microcomputer with a memory card I/C or the like; adding some extra settings in UART2 clock-asynchronous serial I/O mode allows the user to effect this function. Table 1.30 shows the specifications of clock-asynchronous serial I/O mode (compliant with the SIM interface). Figure 1.93 shows the typical transmit/receive timing in UART mode.

Table 1.30: Specifications of clock-asynchronous serial I/O mode (compliant with the SIM interface)

Item	Specification
Transfer data format	<ul style="list-style-type: none"> • Transfer data 8-bit UART mode (bit 2 through bit 0 of address 0378₁₆ = "1012") • One stop bit (bit 4 of address 0378₁₆ = "0") • With the direct format chosen Set parity to "even" (bit 5 and bit 6 of address 0378₁₆ = "1" and "1" respectively) Set data logic to "direct" (bit 6 of address 037D₁₆ = "0"). Set transfer format to LSB (bit 7 of address 037C₁₆ = "0"). • With the inverse format chosen Set parity to "odd" (bit 5 and bit 6 of address 0378₁₆ = "0" and "1" respectively) Set data logic to "inverse" (bit 6 of address 037D₁₆ = "1") Set transfer format to MSB (bit 7 of address 037C₁₆ = "1")
Transfer clock	<ul style="list-style-type: none"> • With the internal clock chosen (bit 3 of address 0378₁₆ = "0"): f_i / 16 (n + 1) (Note 1): f_i=f₁, f₈, f₃₂ • With an external clock chosen (bit 3 of address 0378₁₆ = "1"): f_{EXT} / 16 (n+1) (Note 1) (Note 2)
Transmission / reception control	<ul style="list-style-type: none"> • Disable the CTS and RTS function (bit 4 of address 037C₁₆ = "1")
Other settings	<ul style="list-style-type: none"> • The sleep mode select function is not available for UART2 • Set transmission interrupt factor to "transmission completed" (bit 4 of address 037D₁₆ = "1")
Transmission start condition	<ul style="list-style-type: none"> • To start transmission, the following requirements must be met: <ul style="list-style-type: none"> - Transmit enable bit (bit 0 of address 037D₁₆) = "1" - Transmit buffer empty flag (bit 1 of address 037D₁₆) = "0"
Reception start condition	<ul style="list-style-type: none"> • To start reception, the following requirements must be met: <ul style="list-style-type: none"> - Reception enable bit (bit 2 of address 037D₁₆) = "1" - Detection of a start bit • When transmitting When data transmission from the UART2 transfer register is completed (bit 4 of address 037D₁₆ = "1") • When receiving When data transfer from the UART2 receive register to the UART2 receive buffer register is completed
Error detection	<ul style="list-style-type: none"> • Overrun error (see the specifications of clock-asynchronous serial I/O) (Note 3) • Framing error (see the specifications of clock-asynchronous serial I/O) • Parity error (see the specifications of clock-asynchronous serial I/O) <ul style="list-style-type: none"> - On the reception side, an "L" level is output from the TxD2 pin by use of the parity error signal output function (bit 7 of address 037D₁₆ = "1") when a parity error is detected - On the transmission side, a parity error is detected by the level of input to the RxD2 pin when a transmission interrupt occurs • The error sum flag (see the specifications of clock-asynchronous serial I/O)

Note 1: 'n' denotes the value 00₁₆ to FF₁₆ that is set to the UARTi bit rate generator.

Note 2: f_{EXT} is input from the CLK2 pin.

Note 3: If an overrun error occurs, the UART2 receive buffer will have the next data written in. Note also that the UARTi receive interrupt request bit is not set to "1".

UART0 through UART2

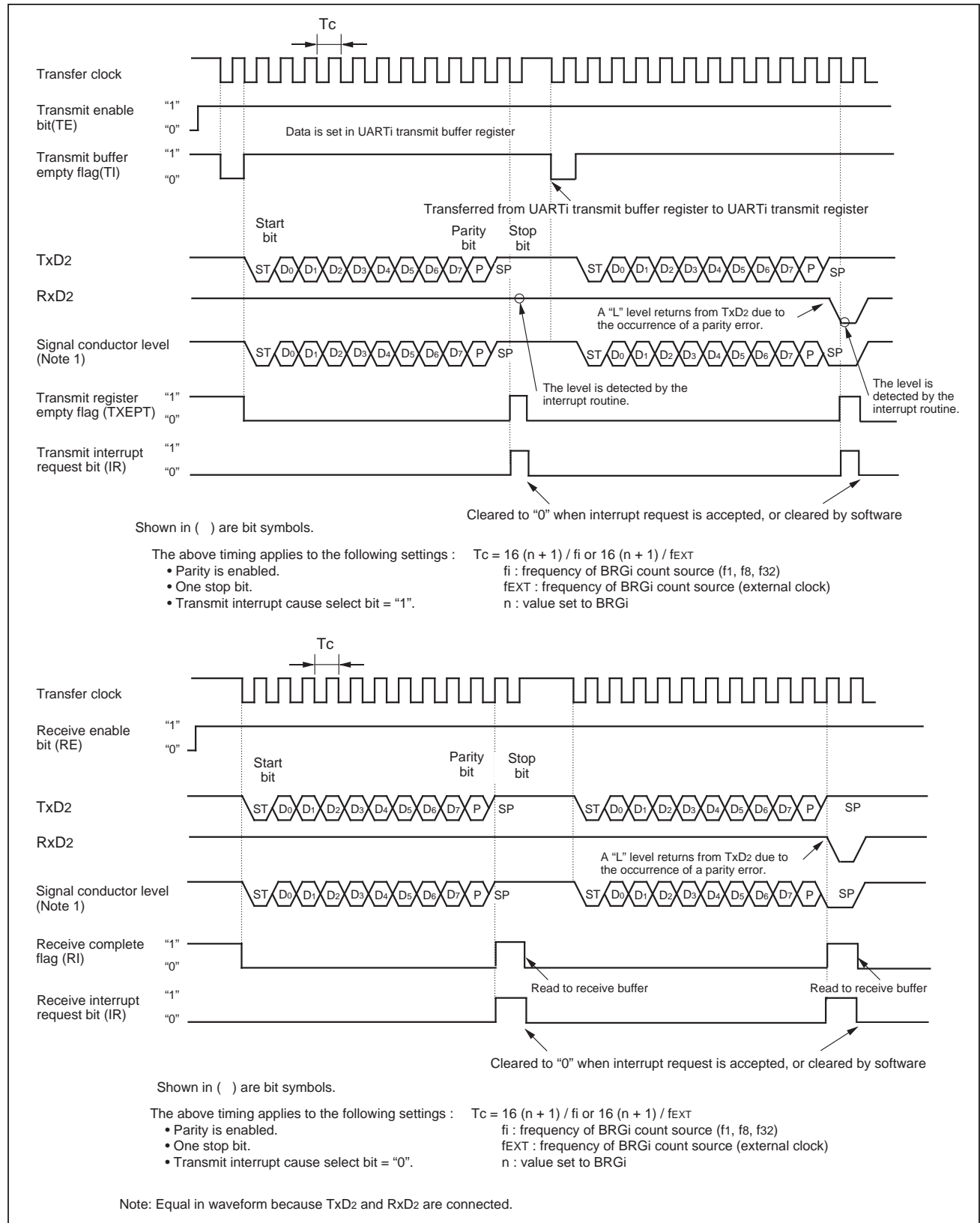


Figure 1.93: Typical transmit/receive timing in UART mode (compliant with the SIM interface)

UART0 through UART2

2.23.3.1 Function for outputting a parity error signal

With the error signal output enable bit (bit 7 of address 037D₁₆) assigned "1", you can output an "L" level from the TxD2 pin when a parity error is detected. In step with this function, the generation timing of a transmission completion interrupt changes to the detection timing of a parity error signal. Figure 1.94 shows the output timing of the parity error signal.

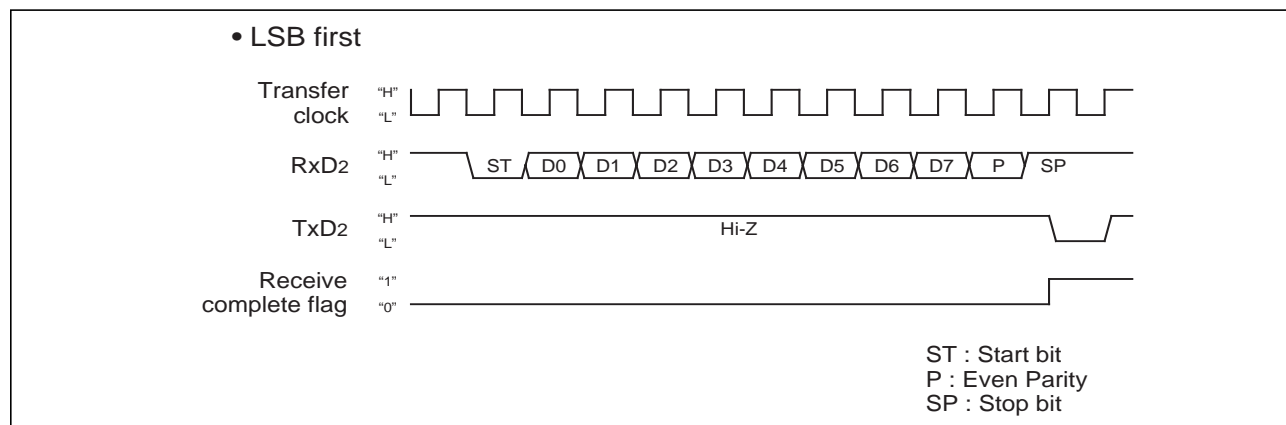


Figure 1.94: Output timing of the parity error signal

2.23.3.2 Direct format/inverse format

Connecting the SIM card allows you to switch between direct format and inverse format. If you choose the direct format, D0 data is output from TxD2. If you choose the inverse format, D7 data is inverted and output from TxD2.

Figure 1.95 shows the SIM interface format.

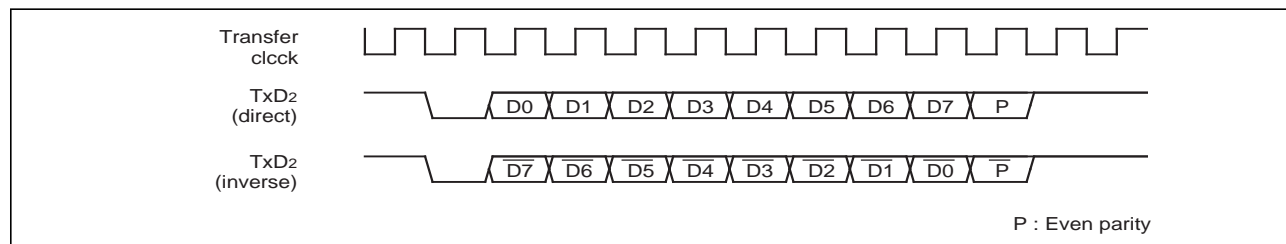


Figure 1.95: SIM interface format

Figure 1.96 shows the example of connecting the SIM interface with TxD2 and RxD2.

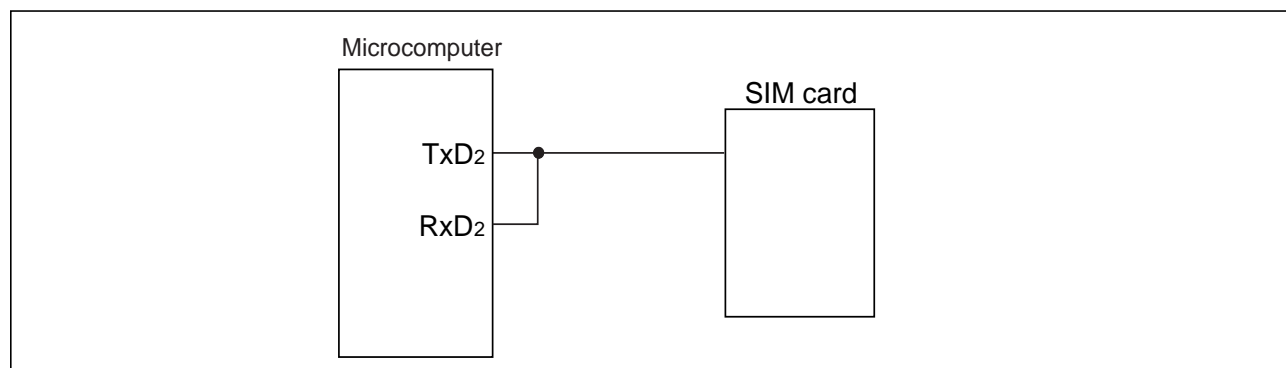


Figure 1.96: Connecting the SIM interface



A-D Converter

2.24 A-D Converter

The A-D converter consists of one 10-bit successive approximation A-D converter circuit with a capacitive coupling amplifier. Pins P100 to P107 function as the analog signal input pins. The direction registers of these pins for A-D conversion must therefore be set to input. The Vref connect bit (bit 5 at address 03D7₁₆) can be used to isolate the resistance ladder of the A-D converter from the reference voltage input pin (VREF) when the A-D converter is not used. Doing so stops any current flowing into the resistance ladder from VREF, reducing the power dissipation. When using the A-D converter, start A-D conversion only after setting bit 5 of 03D7₁₆ to connect VREF.

The result of A-D conversion is stored in the A-D registers of the selected pins. When set to 10-bit precision, the low 8 bits are stored in the even addresses and the high 2 bits in the odd addresses. When set to 8-bit precision, the low 8 bits are stored in the even addresses.

Table 1.31 shows the performance of the A-D converter. Figure 1.97 shows the block diagram of the A-D converter, and Figure 1.98 and Figure 1.99 show the A-D converter-related registers.

Table 1.31: Performance of A-D Converter

Item	Performance	
Method of A-D conversion	Successive approximation (capacitive coupling amplifier)	
Analog input voltage (Note)	0V to AVCC (VCC)	
Operating clock fAD	VCC = 5V	fAD/divide-by-2 or fAD/divide-by-4 or fAD, fAD=f(Xin)
Resolution	8-bit or 10-bit (selectable)	
Absolute precision	VCC = 5V	<ul style="list-style-type: none"> • Without sample and hold function 3LSB • With sample and hold function (8-bit resolution) 2LSB • With sample and hold function (10-bit resolution) 3LSB
Operating modes	One-shot mode, repeat mode, single sweep mode, repeat sweep mode 0, and repeat sweep mode 1	
Analog input pins	8pins (AN0 to AN7)	
A-D conversion start condition	<ul style="list-style-type: none"> • Software trigger A-D conversion starts when the A-D conversion start flag changes to "1" • External trigger (can be retriggered) A-D conversion starts when the A-D conversion start flag is "1" and the $\overline{AD_TRG}/P87$ input changes from "H" to "L" 	
Conversion speed per pin	<ul style="list-style-type: none"> • Without sample and hold function 8-bit resolution: 49 ϕAD cycles, 10-bit resolution: 59 ϕAD cycles • With sample and hold function 8-bit resolution: 28 ϕAD cycles, 10-bit resolution: 33 ϕAD cycles 	
Note	Does not depend on use of sample and hold function.	

A-D Converter

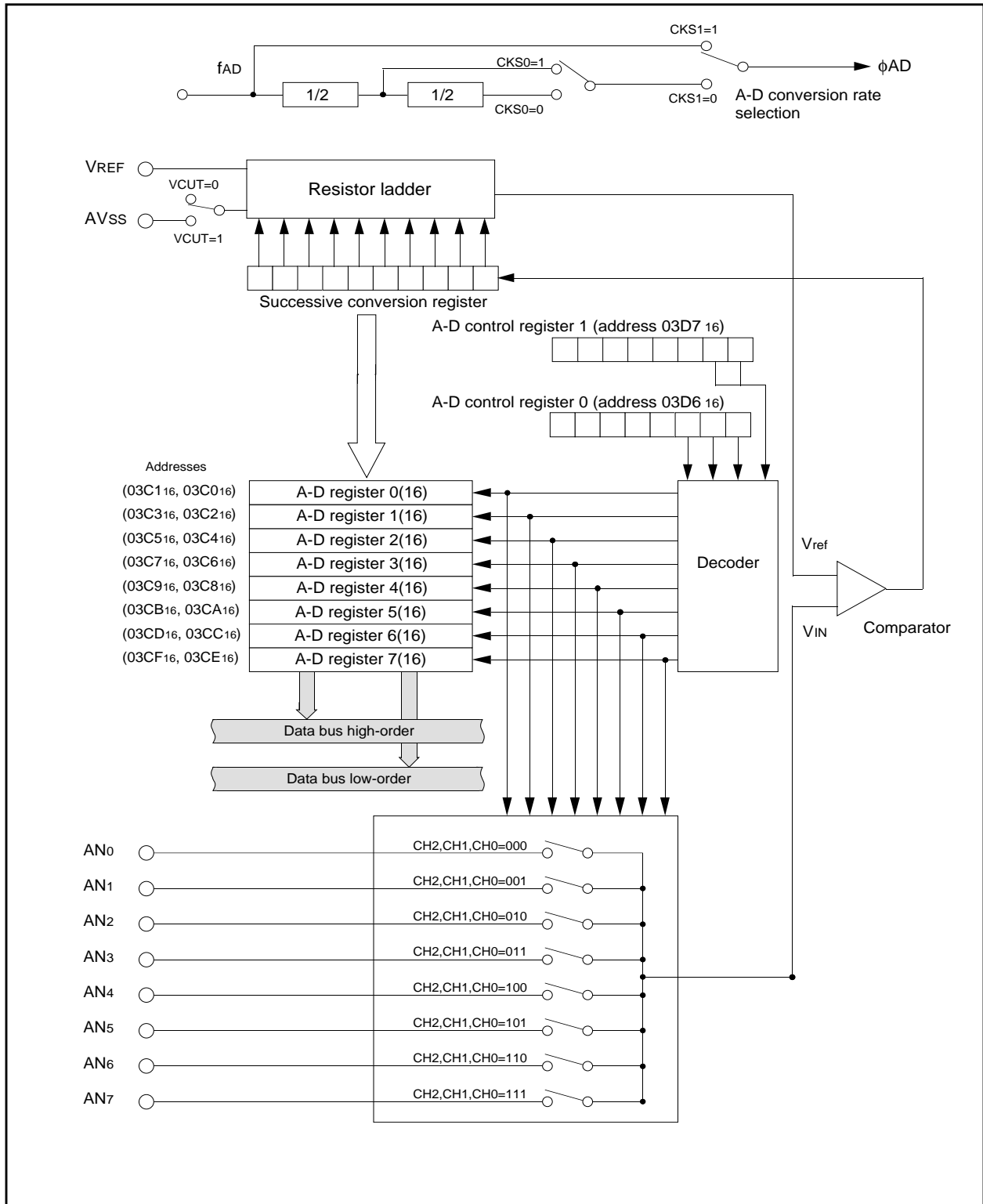


Figure 1.97: Block diagram of A-D converter

A-D Converter

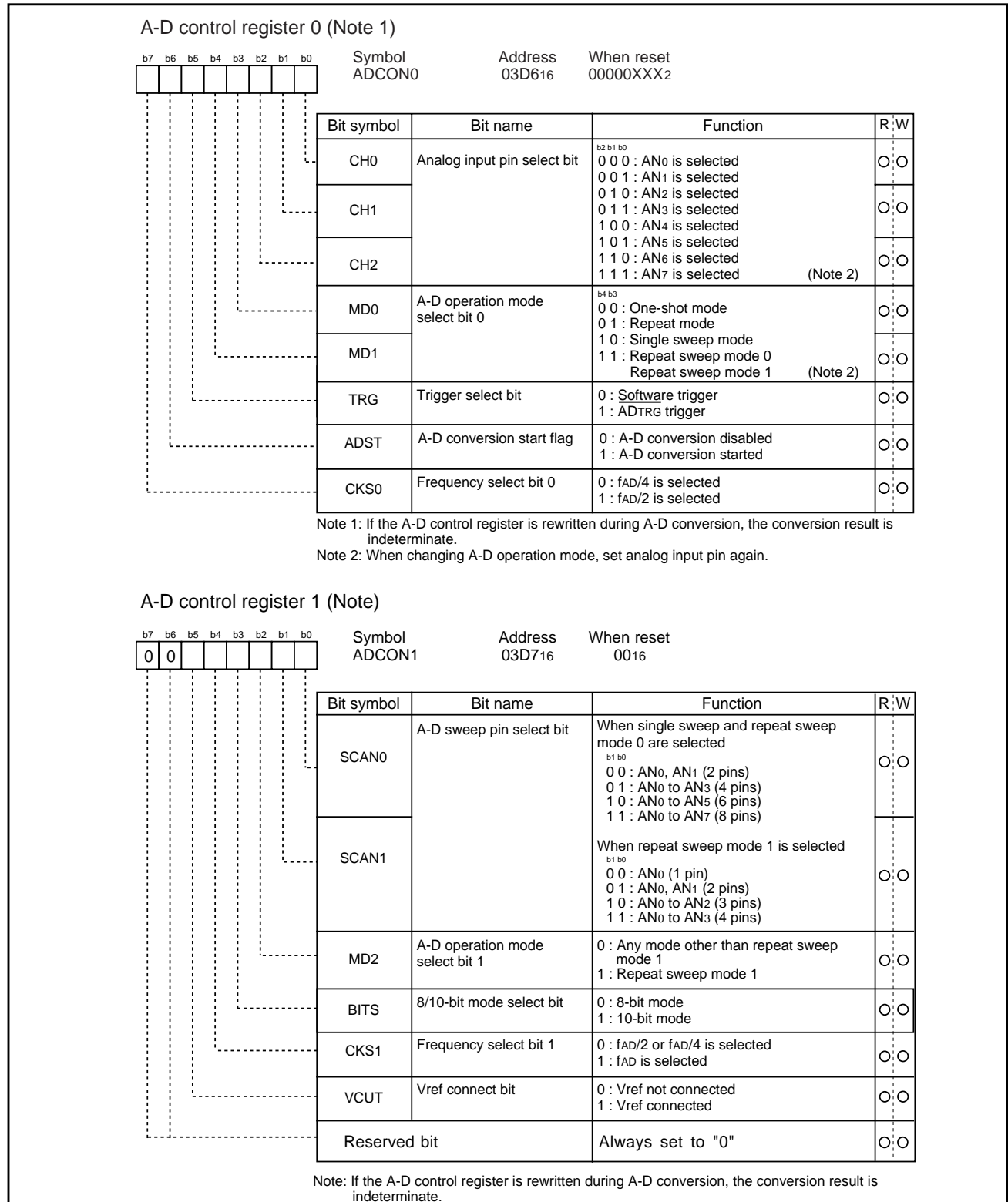


Figure 1.98: A-D converter-related registers (1)

A-D Converter

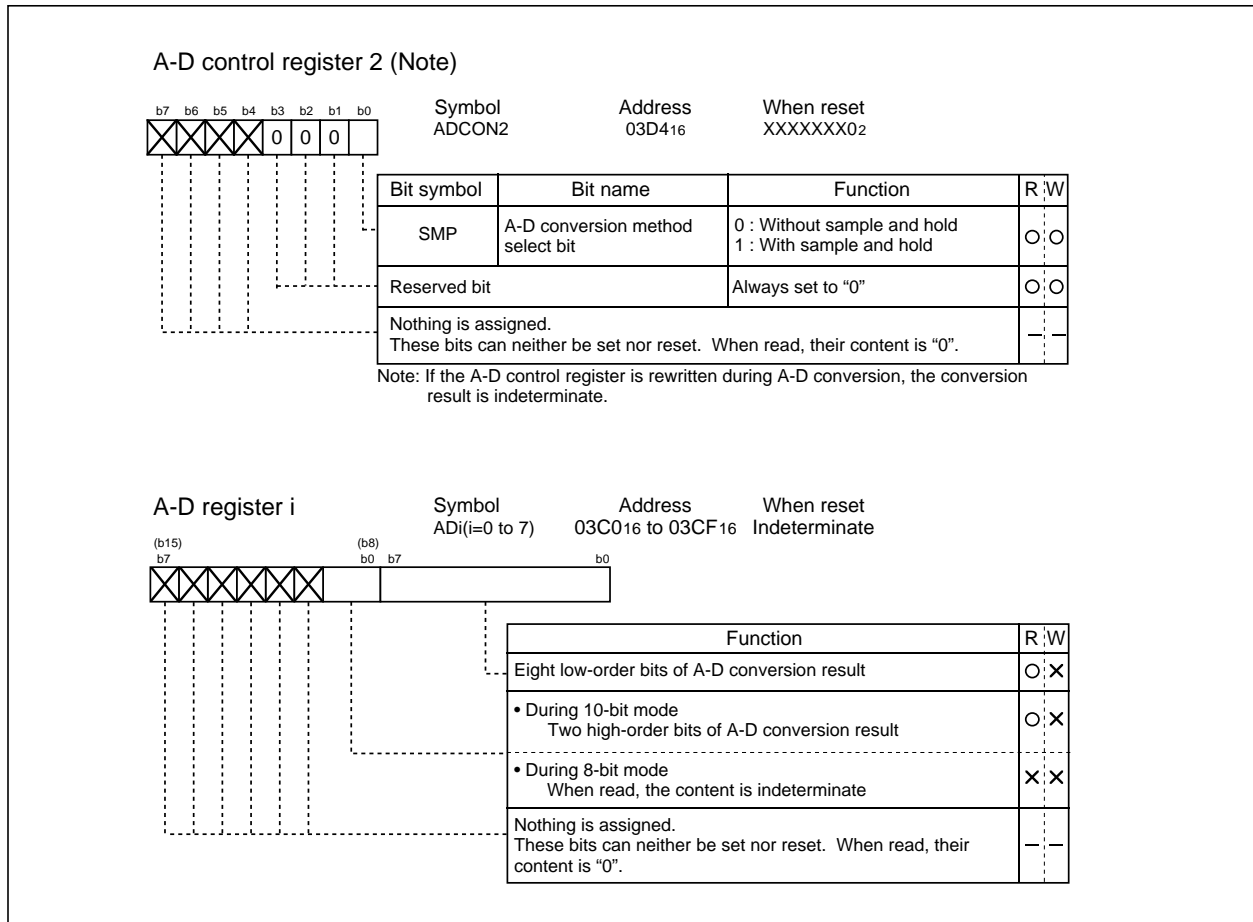


Figure 1.99: A-D converter-related registers (2)

A-D Converter

2.24.1 One-shot mode

In one-shot mode, the pin selected using the analog input pin select bit is used for one-shot A-D conversion. Table 1.32 shows the specifications of one-shot mode. Figure 1.100 shows the A-D control register in one-shot mode.

Table 1.32: One-shot mode specification

Item	Specification
Function	The pin selected by the analog input pin select bit is used for one A-D conversion
Start condition	Writing "1" to A-D conversion start flag
Stop condition	<ul style="list-style-type: none"> •End of A-D conversion (A-D conversion start flag changes to "0", except when external trigger is selected) •Writing "0" to A-D conversion start flag
Interrupt request generation timing	End of A-D conversion
Input pin	One of AN0 to AN7, as selected
Reading of result of A-D converter	Read A-D register corresponding to selected pin

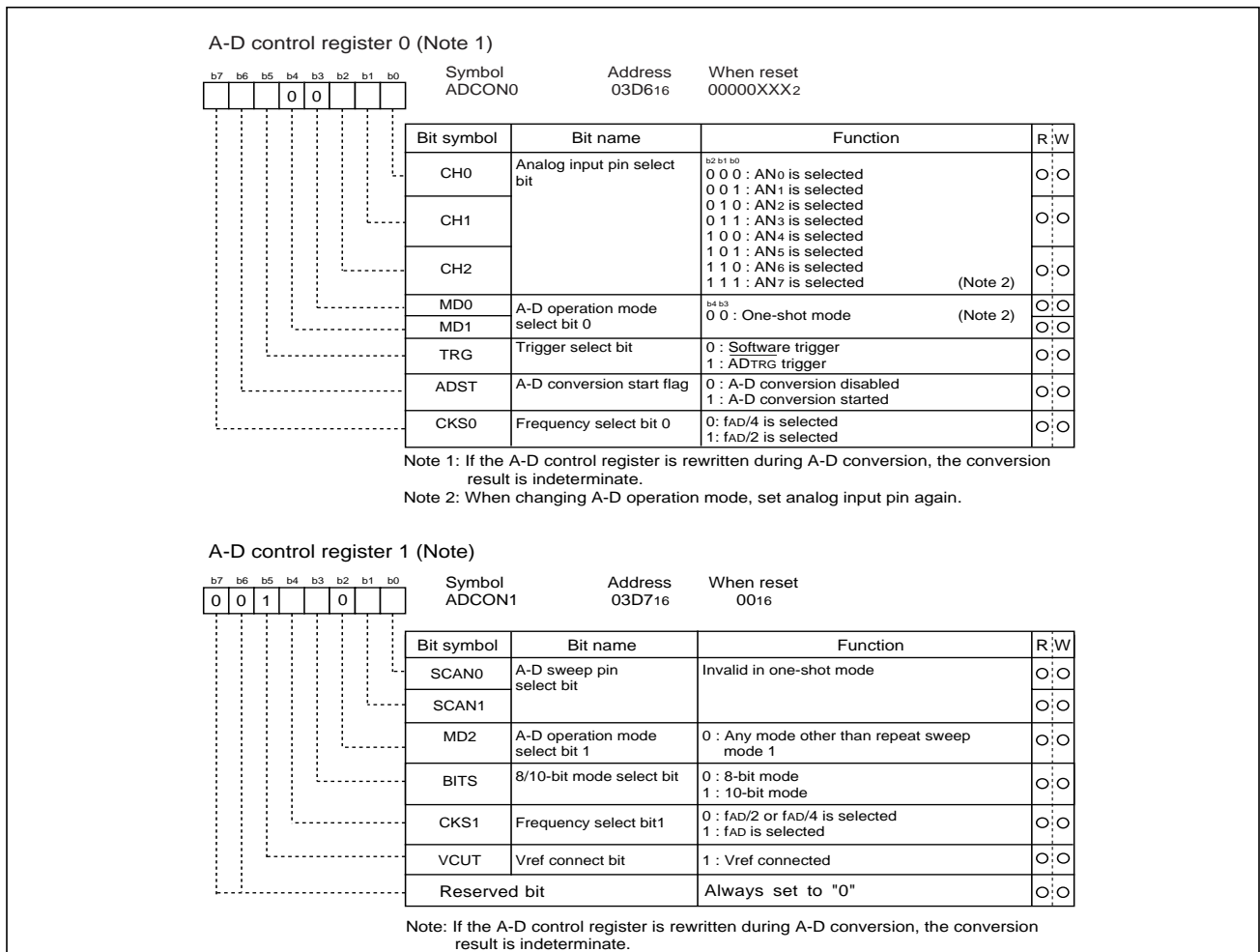


Figure 1.100: A-D conversion register in one-shot mode

A-D Converter

2.24.2 Repeat mode

In repeat mode, the pin selected using the analog input pin select bit is used for repeated A-D conversion. Table 1.33 shows the specifications of repeat mode. Figure 1.101 shows the A-D control register in repeat mode.

Table 1.33: Repeat sweep mode 0 specifications

Item	Specification
Function	The pin selected by the analog input pin select bit is used for repeated A-D conversion
Star condition	Writing "1" to A-D conversion start flag
Stop condition	Writing "0" to A-D conversion start flag
Interrupt request generation timing	None generated
Input pin	One of AN0 to AN7, as selected
Reading of result of A-D converter	Read A-D register corresponding to selected pin

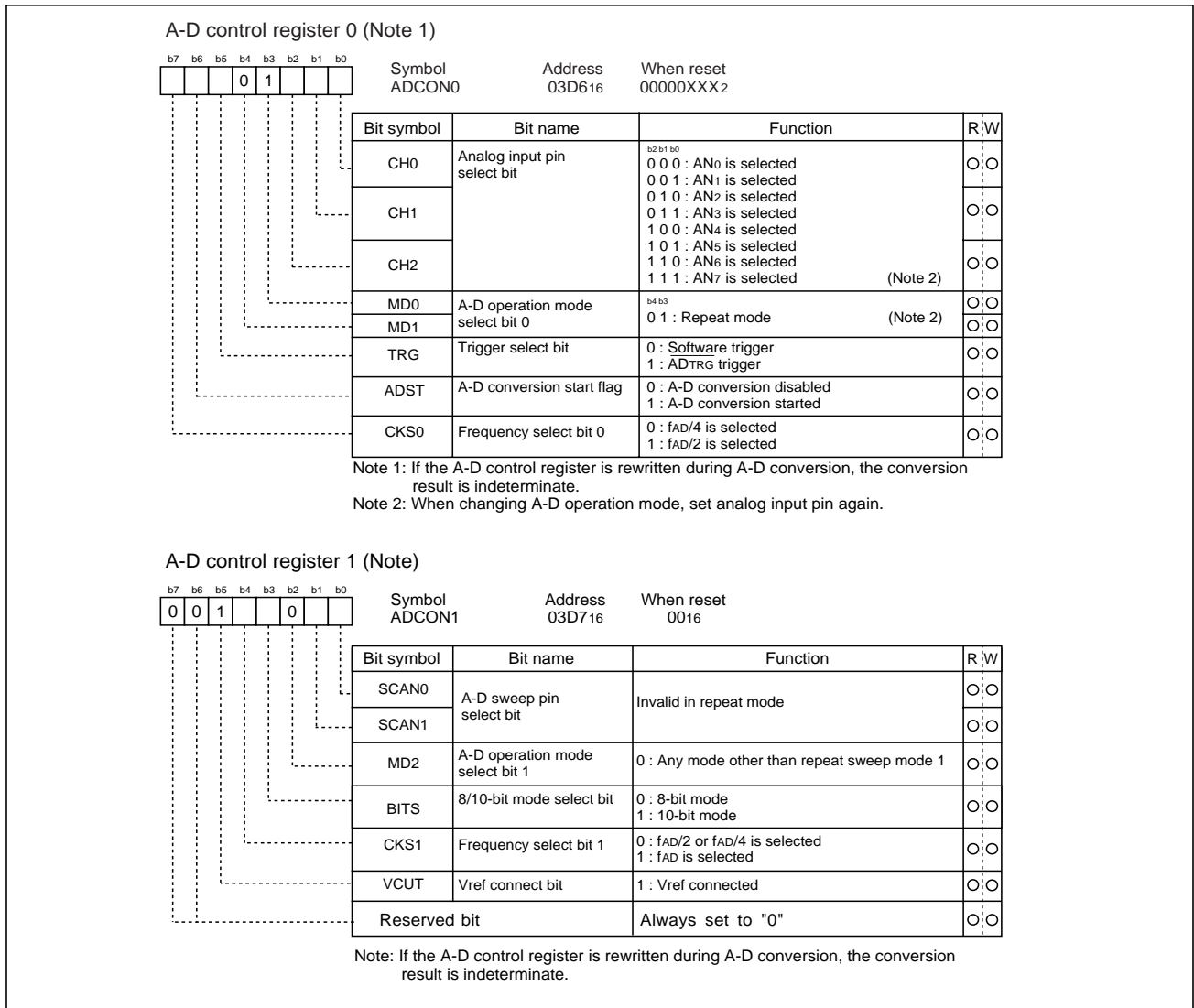


Figure 1.101: A-D conversion register in repeat mode

A-D Converter

2.24.3 Single sweep mode

In single sweep mode, the pins selected using the A-D sweep pin select bit are used for one-by-one A-D conversion. Table 1.34 shows the specifications of single sweep mode. Figure 1.102 shows the A-D control register in single sweep mode.

Table 1.34: Single sweep mode specification

Item	Specification
Function	The pins selected by the A-D sweep pin select bit are used for one-by-one A-D conversion
Start condition	Writing "1" to A-D converter start flag
Stop condition	<ul style="list-style-type: none"> •End of A-D conversion (A-D conversion start flag changes to "0", except when external trigger is selected) •Writing "0" to A-D conversion start flag
Interrupt request generation timing	End of A-D conversion
Input pin	AN0 and AN1 (2 pins), AN0 to AN3 (4 pins), AN0 to AN5 (6 pins), or AN0 to AN7 (8 pins)
Reading of result of A-D converter	Read A-D register corresponding to selected pin

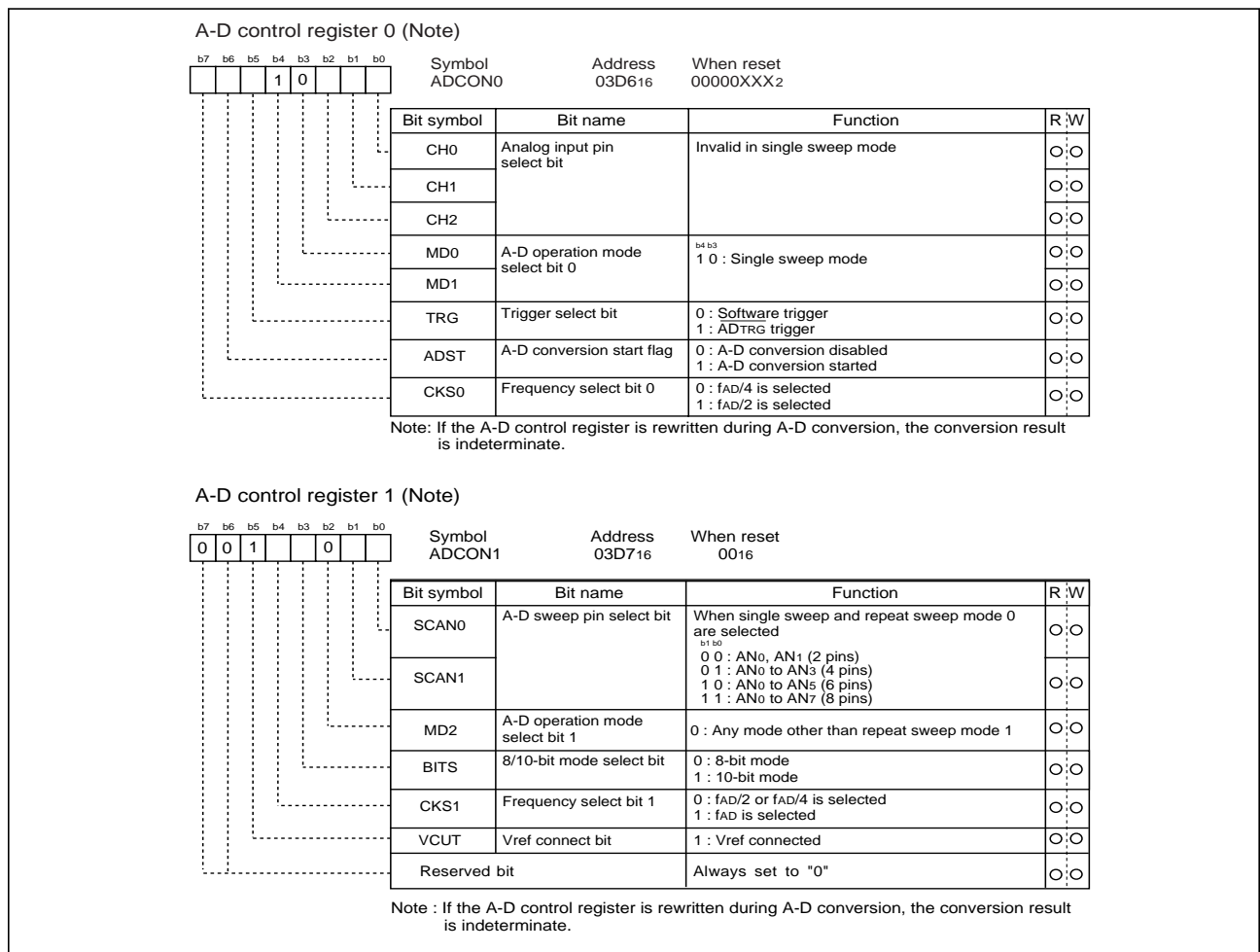


Figure 1.102: A-D conversion register in single sweep mode

A-D Converter

2.24.4 Repeat sweep mode 0

In repeat sweep mode 0, the pins selected using the A-D sweep pin select bit are used for repeat sweep A-D conversion. Table 1.35 shows the specifications of repeat sweep mode 0. Figure 1.103 shows the A-D control register in repeat sweep mode 0.

Table 1.35: Repeat sweep mode 0 specifications

Item	Specification
Function	The pins selected by the A-D sweep pin select bit are used for repeat sweep A-D conversion
Start condition	Writing "1" to A-D conversion start flag
Stop condition	Writing "0" to A-D conversion start flag
Interrupt request generation timing	None generated
Input pin	AN0 and AN1 (2 pins), AN0 to AN3 (4 pins), AN0 to AN5 (6 pins), or AN0 to AN7 (8 pins)
Reading of result of A-D converter	Read A-D register corresponding to selected pin (at any time)

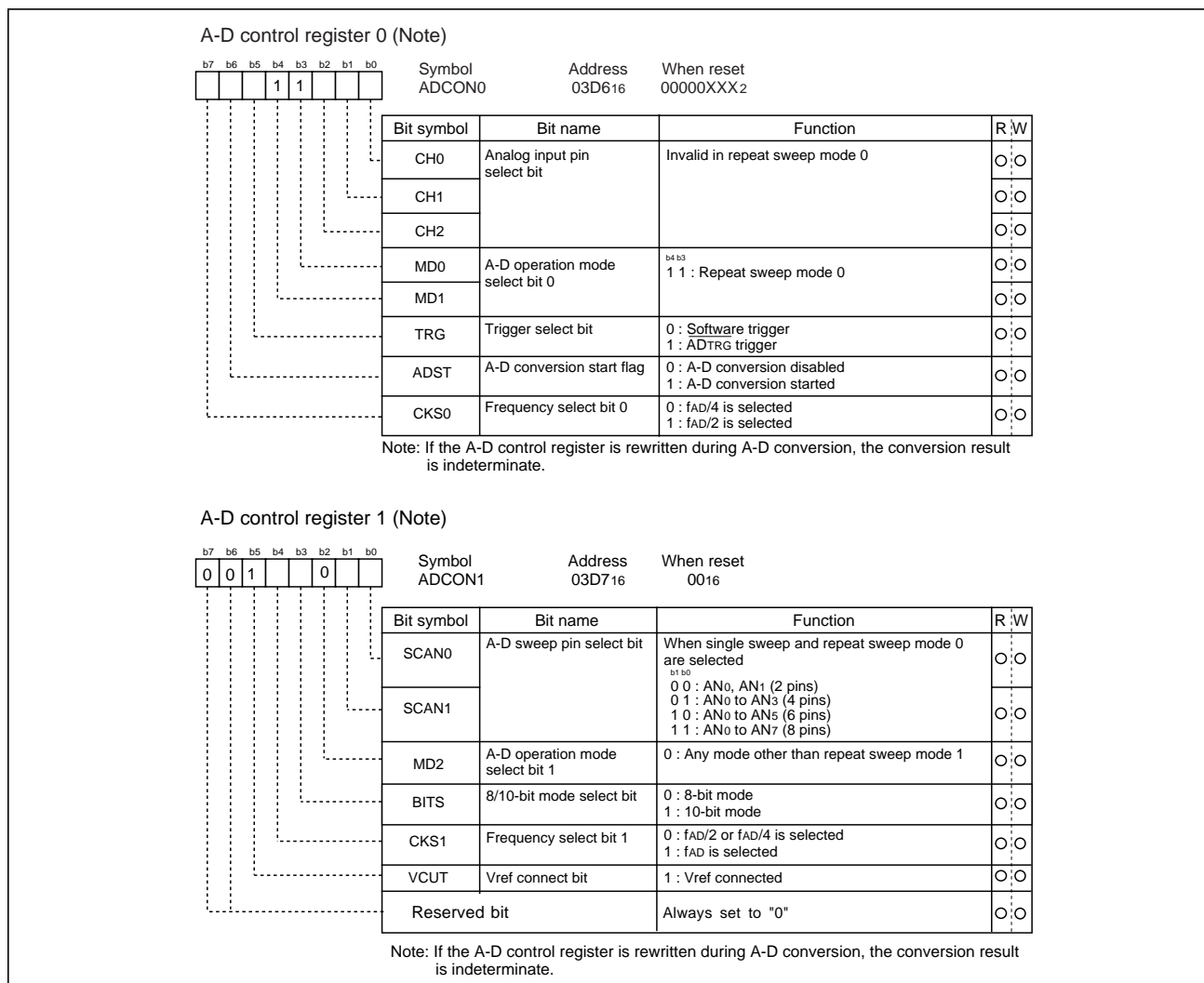


Figure 1.103: A-D conversion register in repeat sweep mode 0

A-D Converter

2.24.5 Repeat sweep mode 1

In repeat sweep mode 1, all pins are used for A-D conversion with emphasis on the pin or pins selected using the A-D sweep pin select bit. Table 1.36 shows the specifications of repeat sweep mode 1. Figure 1.104 show the A-D control in repeat sweep mode 1.

Table 1.36: Repeat sweep mode 1 specification

Item	Specification
Function	All pins perform repeat sweep A-D conversion, with emphasis on the pin or pins selected by the A-D sweep pin select bit Example: AN0 selected AN0 AN1 AN0 AN2 AN0 AN3, etc.
Start condition	Writing "1" to A-D conversion start flag
Stop condition	Writing "0" to A-D conversion start flag
Interrupt request generation timing	None generated
Input pin	AN0 (1 pin), AN0 and AN1 (2 pins), AN0 to AN2 (3 pins), AN0 to AN3 (4 pins)
Reading of result of A-D converter	Read A-D register corresponding to selected pin (at any time)

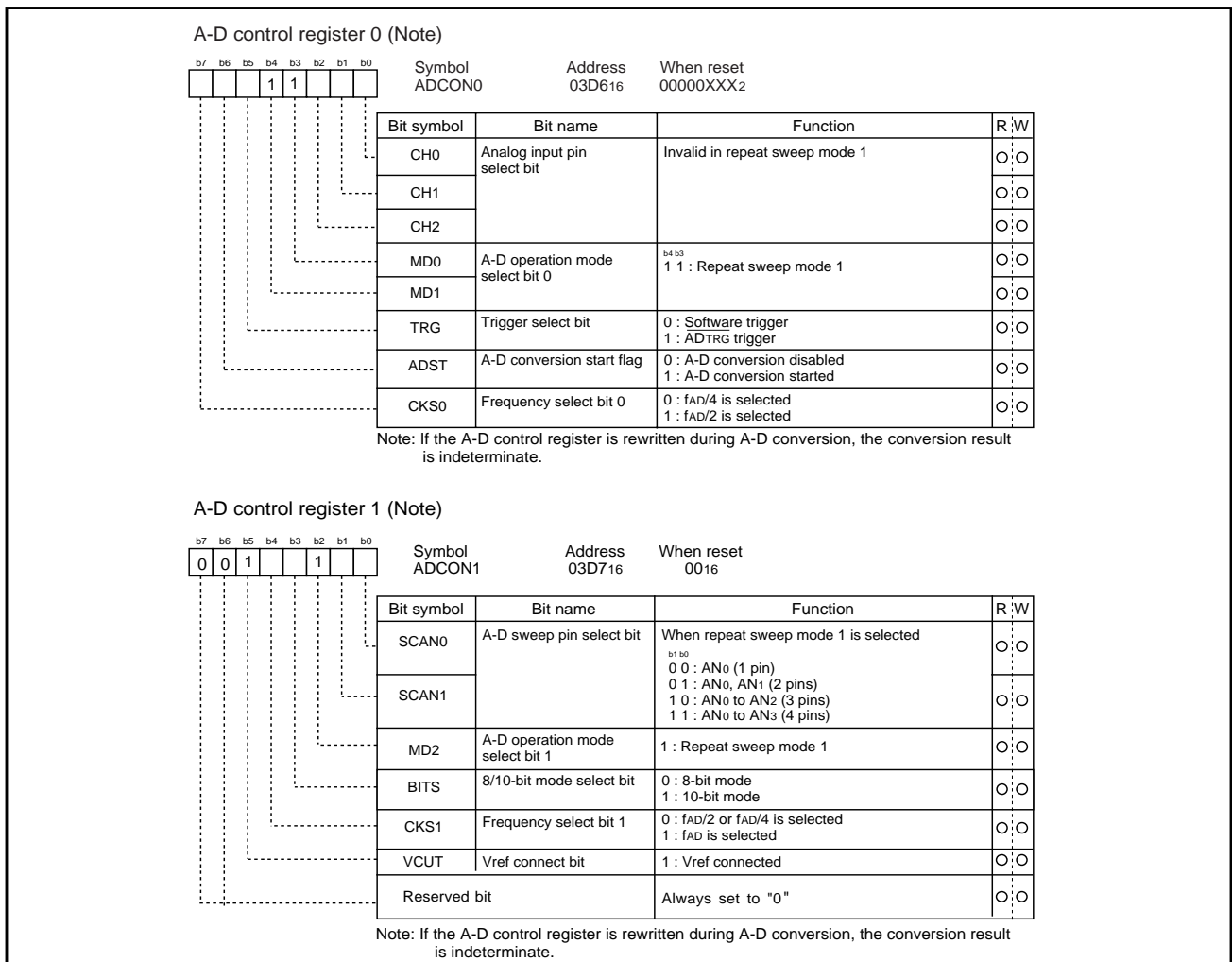


Figure 1.104: A-D conversion register in repeat sweep mode 1



A-D Converter

2.24.6 Sample and hold

Sample and hold is selected by setting bit 0 of the A-D control register 2 (address $03D4_{16}$) to "1". When sample and hold is selected, the rate of conversion of each pin increases. As a result, a 28ϕ AD cycle is achieved with 8-bit resolution and 33ϕ AD with 10-bit resolution. Sample and hold can be selected in all modes. However, in all modes, be sure to specify before starting A-D conversion whether sample and hold is to be used.

CRC Calculation Circuit

2.25 CRC Calculation Circuit

The Cyclic Redundancy Check (CRC) calculation circuit detects an error in data blocks. The microcomputer uses a generator polynomial of CRC_CCITT ($X^{16} + X^{12} + X^5 + 1$) to generate CRC code.

The CRC code is a 16-bit code generated for a block of a given data length in multiples of 8 bits. The CRC code is set in a CRC data register each time one byte of data is transferred to a CRC input register after writing an initial value into the CRC data register. Generation of CRC code for one byte of data is completed in two machine cycles.

Figure 1.105 shows the block diagram of the CRC circuit. Figure 1.106 shows the CRC-related registers.

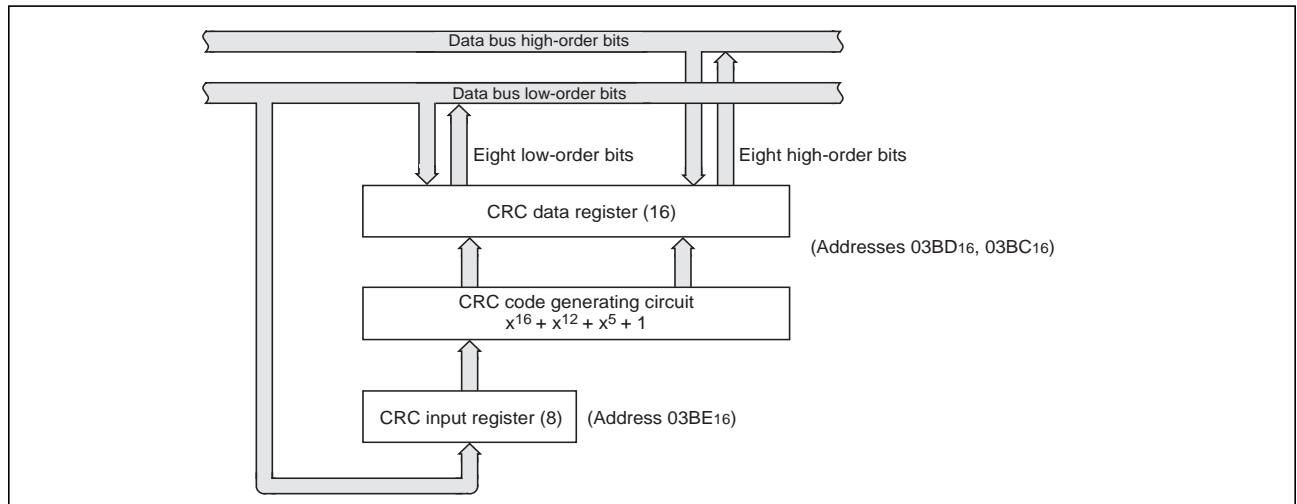


Figure 1.105: Block diagram of CRC circuit

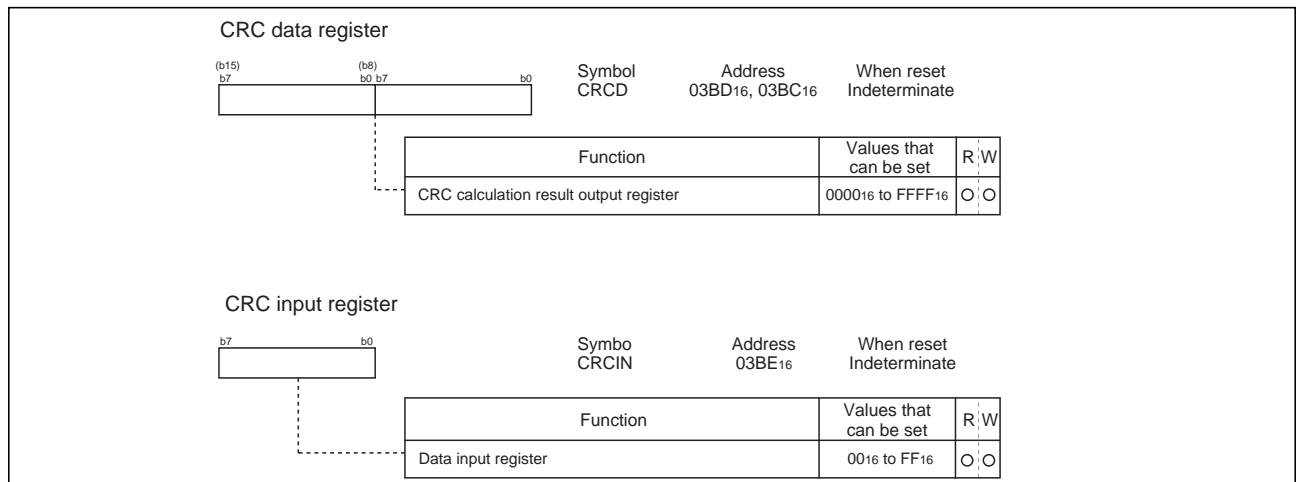


Figure 1.106: CRC-related registers



Programmable I/O Ports

2.26 Programmable I/O Ports

There are 63 programmable I/O ports: P0 to P3, P6 to P8 (excluding P85), and P10. Each port can be set independently for input or output using the direction register. A pull-up resistance for each block of 4 ports can be set. P85 is an input-only port and has no built-in pull-up resistance.

Figure 1.107, Figure 1.108 and Figure 1.109 show the programmable I/O ports.

Each pin functions as a programmable I/O port and as the I/O for the built-in peripheral devices.

To use the pins as the inputs for the built-in peripheral devices, set the direction register of each pin to input mode. When the pins are used as the outputs for the built-in peripheral devices, they function as outputs regardless of the contents of the direction registers. Unused I/O pins can be terminated as shown in Figure 1.114 and Table 1.37 .

2.26.1 Direction registers

Figure 1.110 shows the direction registers.

These registers are used to choose the direction of the programmable I/O ports. Each bit in these registers corresponds one for one to each I/O pin.

Note: There is no direction register bit for P85.

2.26.2 Port registers

Figure 1.111 shows the port registers.

These registers are used to write and read data for input and output to and from an external device. A port register consists of a port latch to hold output data and a circuit to read the status of a pin. Each bit in port registers corresponds one for one to each I/O pin.

2.26.3 Pull-up control registers

Figure 1.112 shows the pull-up control registers. The pull-up control register can be set to apply a pull-up resistance to each block of 4 ports. When ports are set to have a pull-up resistance, the pull-up resistance is connected only when the direction register is set for input.

2.26.4 High drive capacity registers

Figure 1.113 shows the Port 2 and PWM drive capacity register. Port 2 can be configured to drive an LED by increasing the drive strength of the corresponding bit's N-channel transistor. Each Timer output (TA0OUT~TA4OUT) can be configured for high-drive capability by increasing the drive strength of the corresponding bits.

Programmable I/O Ports

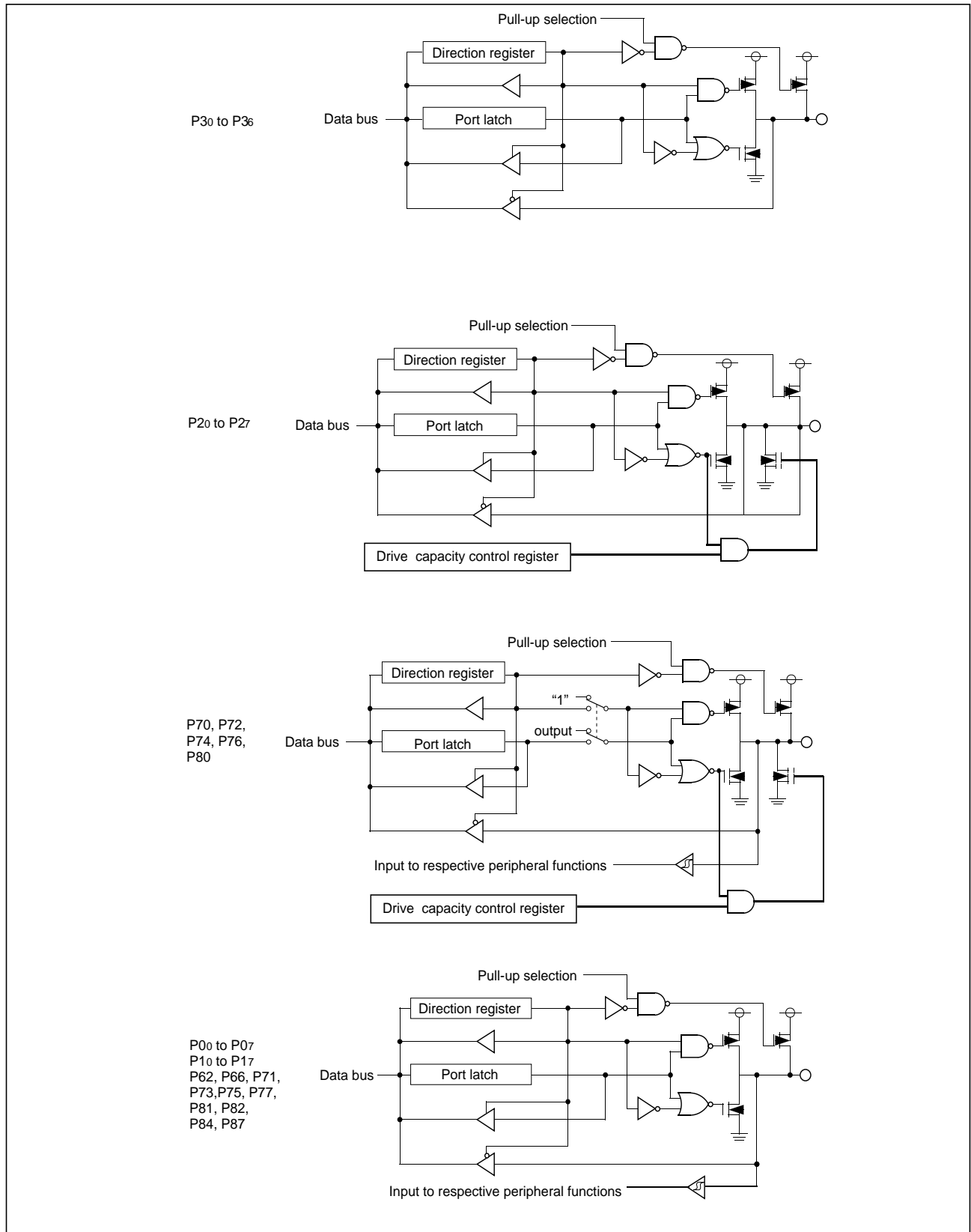


Figure 1.107: Programmable I/O ports (1)

Programmable I/O Ports

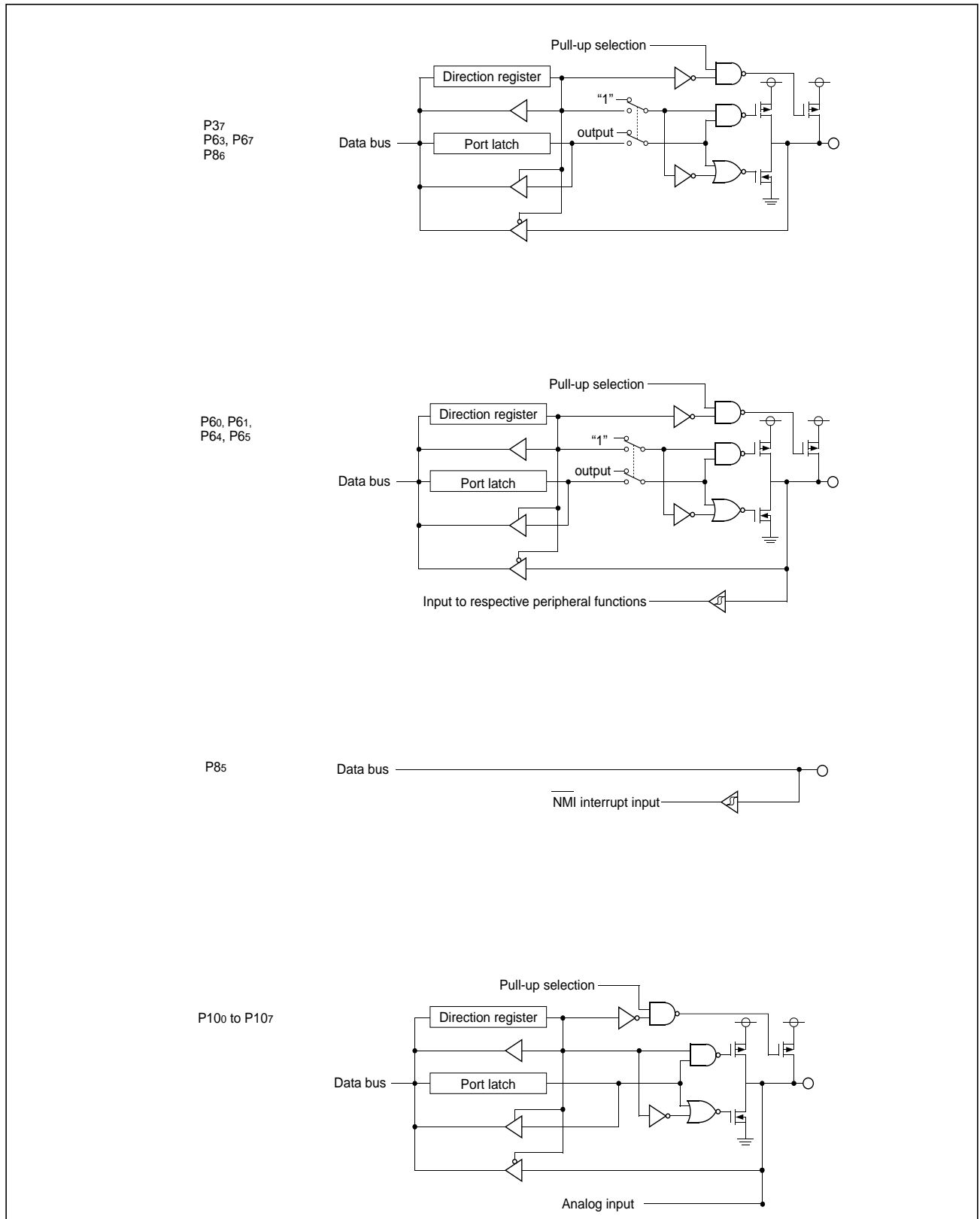


Figure 1.108: Programmable I/O ports (2)

Programmable I/O Ports

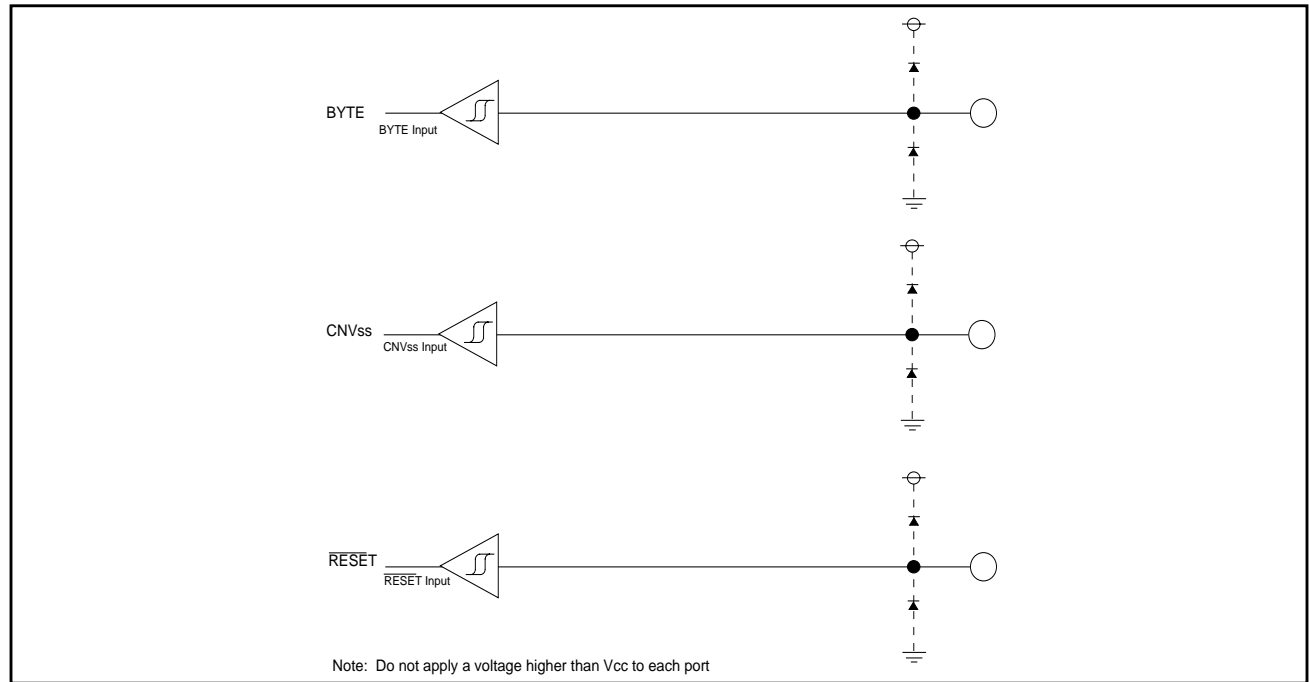


Figure 1.109: Programmable I/O Ports (3)

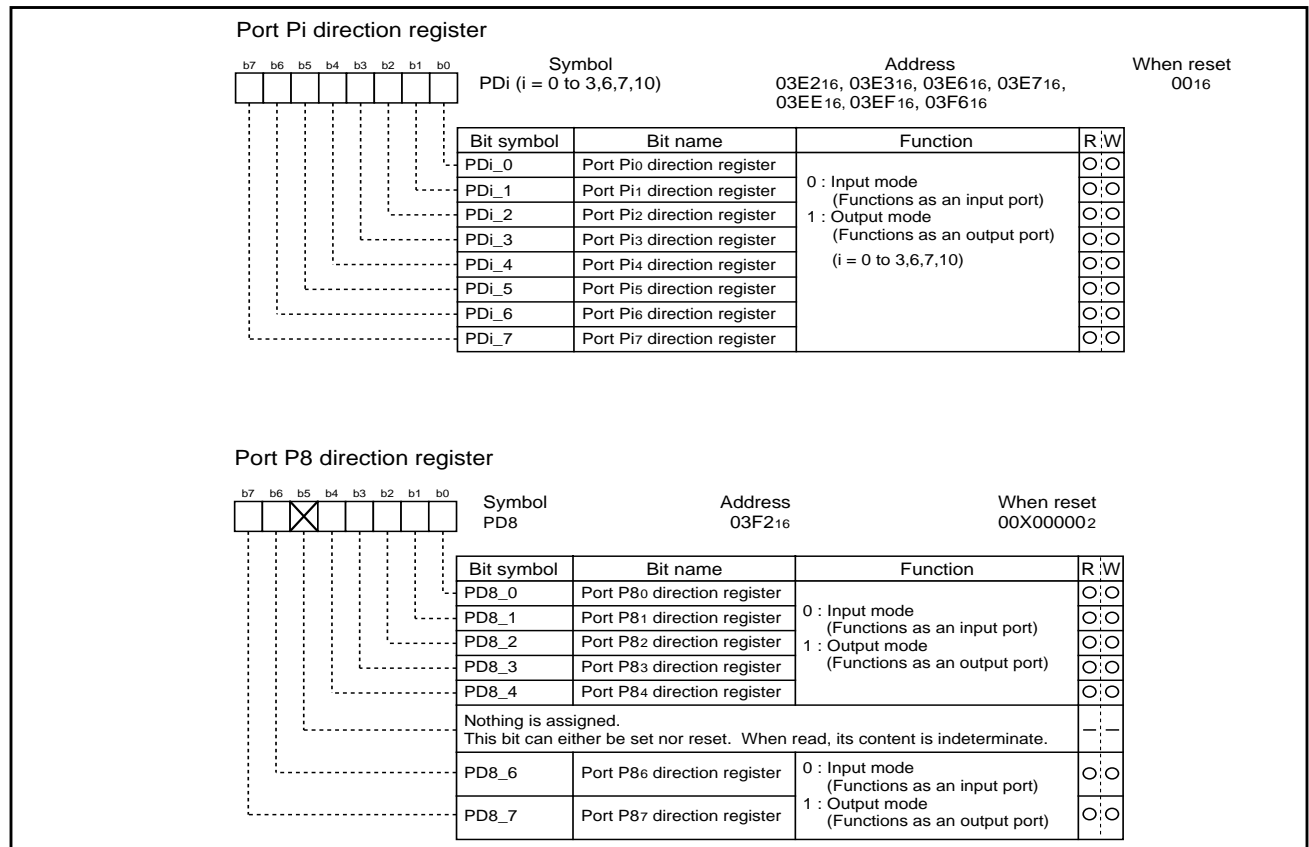


Figure 1.110: Direction register

Programmable I/O Ports

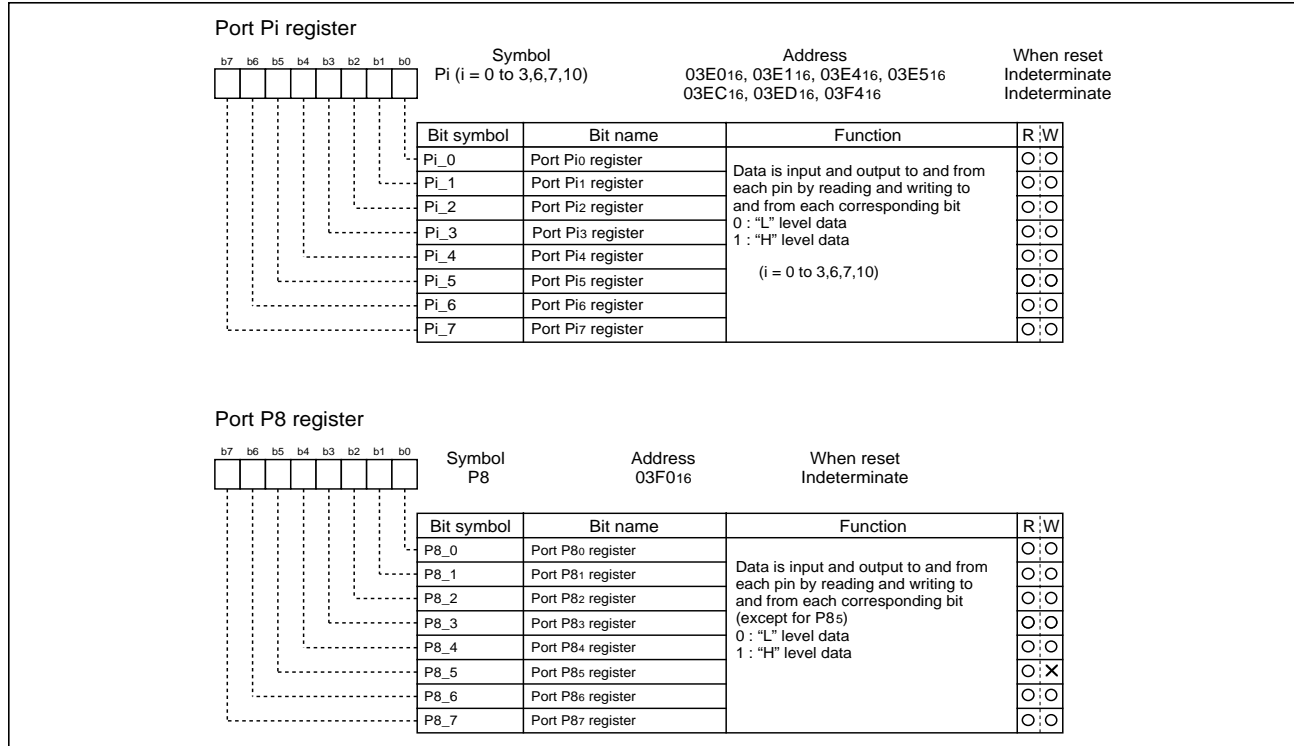


Figure 1.111: Port register

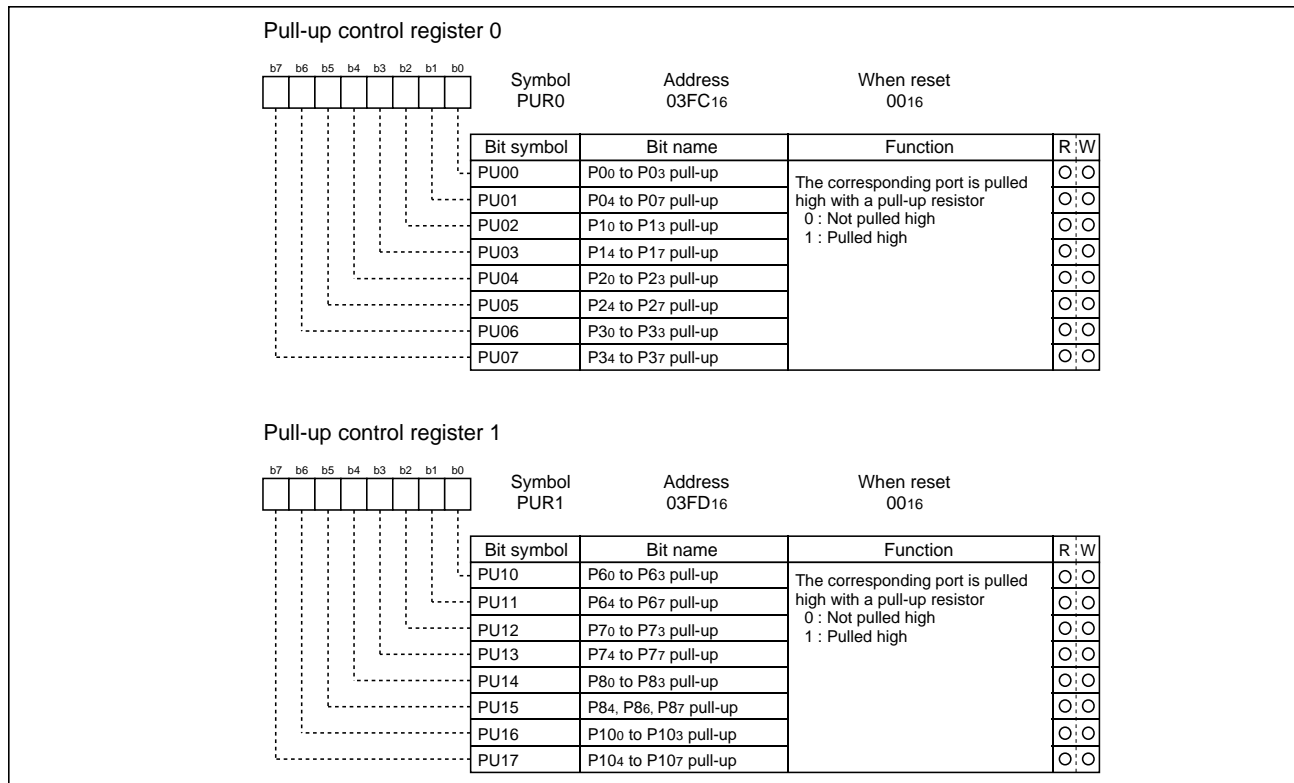


Figure 1.112: Pull-up control register

Programmable I/O Ports

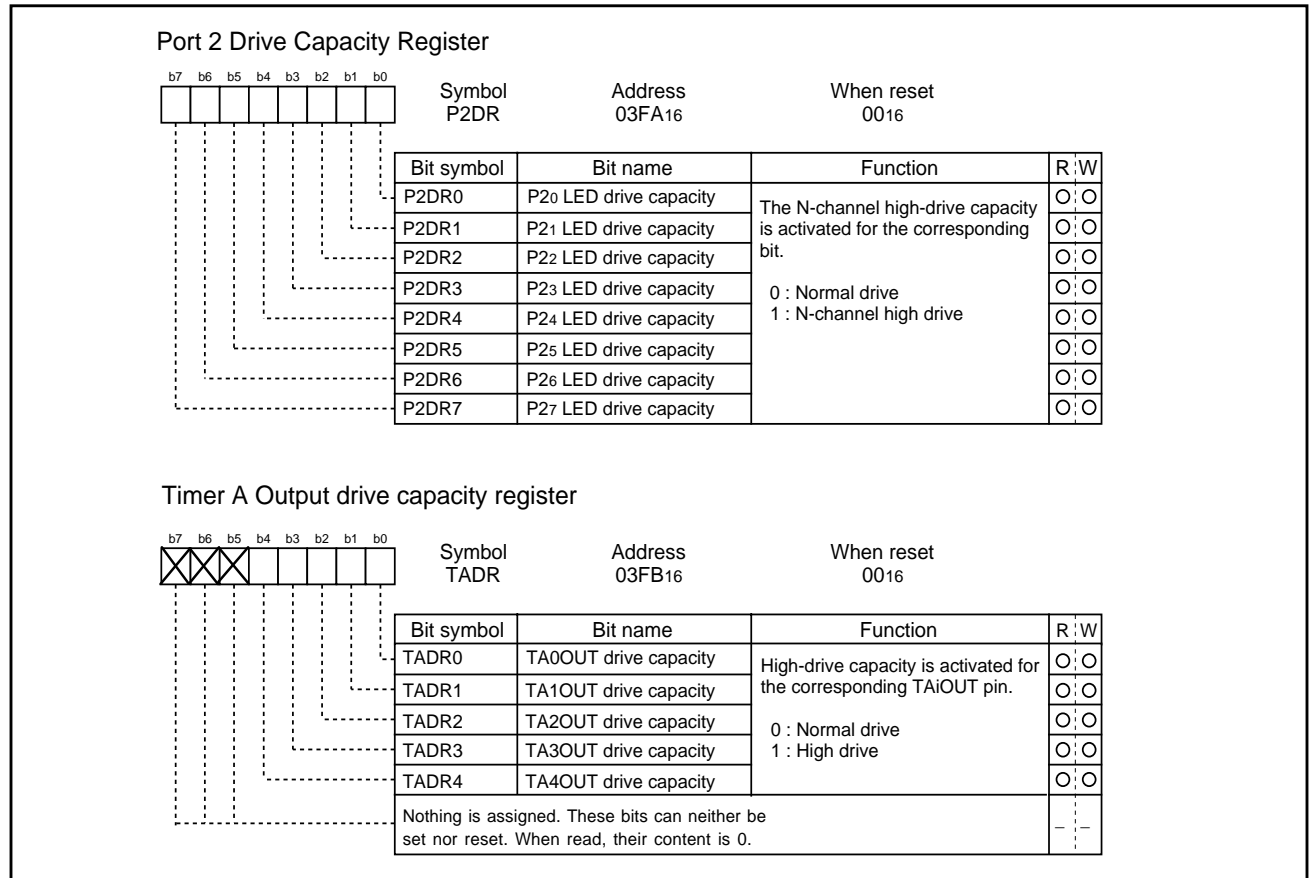


Figure 1.113: Port 2 and Timer A Output drive capacity registers



Usage Precautions

3.0 Usage

3.1 Usage Precautions

3.1.1 A-D Converter

- Write to each bit (except bit 6) of A-D control register 0, to each bit of A-D control register 1, and to bit 0 of A-D control register 2 when A-D conversion is stopped (before a trigger occurs).
In particular, when the Vref connection bit is changed from "0" to "1", start A-D conversion after an elapse of 1 μ s or longer.
- When changing A-D operation mode, select analog input pin again.
- Using one-shot mode or single sweep mode
Read the corresponding A-D register after confirming the A-D conversion is finished. (It is known by A-D conversion interrupt request bit.)
- Using repeat mode, repeat sweep mode 0 or repeat sweep mode 1
Use the undivided main clock as the internal CPU clock.

3.1.2 Built-in PROM version

- All built-in PROM versions
High voltage is required to program to the built-in PROM. Be careful not to apply excessive voltage. Be especially careful during power-on.
- One Time PROM version
One Time PROM versions shipped in blank, of which built-in PROMs are programmed by users, are also provided. For these microcomputers, a programming test and screening are not performed in the assembly process and the following processes. To improve their reliability after programming, we recommend to program and test as flow shown in Figure 115 before use.
Wiring for the Vpp pin of the One-Time PROM version should be as follows (Vpp pin is also used as the CNVss pin):
 - Make the length of wiring between the Vpp pin and Vss pin or Vcc pin the shortest possible.
 - When the wiring length has to be longer, connect an approximately 5K ohm resistor in series from the Vpp pin to the Vss pin or Vcc pin with the shortest possible wiring. This is because the Vpp pin is the power source input pin for the built-in PROM. When programming in the built-in PROM, the impedance of the Vpp pin is low to allow the electric current for wiring flow into the PROM. Because of this, noise can enter easily. If noise enters the Vpp pin, abnormal instruction codes or data are read from the built-in PROM which may cause a program runaway.

3.1.3 Dedicated Input Pins

If a dedicated input pin is connected to a power supply that is different than the supply that Vcc is connected to, a resistor (approximately 1k ohm) should be added between that input pin and the power supply it is connected to, otherwise, if the dedicated input pin voltage is higher than Vcc, latch up could occur.

Usage Precautions

3.1.4 DMAC

When the DMA enable bit (bit 3 of DM0CON and DM1CON) is set to “1”, the DMAC is in an active state.

The DMA request bit (bit 2 of DM0CON and DM1CON) is set to “1” when a request for DMA transfer occurs, regardless of the state of the DMA enable bit.

If the DMAC is active when the request bit becomes “1”, the data transfer begins immediately. The request bit is cleared to “0” when the transfer begins. It is also possible for the DMA request bit to get set to a “1” due to the DMA request cause select bits being changed. Therefore, the DMA request bit should be cleared (“0”) after changing the DMA request cause select bits.

To best judge the state of the DMAC, the DMA enable bit should be read instead of the DMA request bit.

3.1.5 Interrupts

- Reading address 00000₁₆
 - When a maskable interrupt occurs, the CPU reads the interrupt information (the interrupt number and interrupt request level) in the interrupt sequence.
The interrupt request bit of the corresponding interrupt written in address 00000₁₆ is then set to “0”.
Reading address 00000₁₆ by software sets enabled highest priority interrupt source request bit to “0”.
Though the interrupt is generated, the interrupt routine may not be executed.
Do not read address 00000₁₆ by software.
- Setting the stack pointer
 - The value of the stack pointer is initialized to 00000₁₆ immediately after reset. Accepting an interrupt before setting a value in the stack pointer may cause program runaway. Be sure to set a value in the stack pointer before accepting an interrupt.
 - When using the $\overline{\text{NMI}}$ interrupt, initialize the stack pointer at the beginning of a program. Concerning the first instruction immediately after reset, generating any interrupts including the $\overline{\text{NMI}}$ interrupt is prohibited.
- Setting interrupts
 - Changing the Interrupt Priority Level select bit (ILVL) and clearing the Interrupt Request bit (IR) in the Interrupt Control Registers (ICR) while the Interrupt enable flag (I-FLAG) is “1”, may result in unintended operations, such as BRK and other interrupts being generated. It is recommended that the interrupts be disabled by clearing the I-FLAG before setting ILVL or clearing the IR bit. To prevent the I-FLAG from being set before the ICR is rewritten due to the effects of the instruction queue, instructions that equal a minimum of 2 cycles should be inserted between writing to the ICR and setting the I-FLAG (2-NOPs, I MOV, I POP, etc.)
- The $\overline{\text{NMI}}$ interrupt
 - As for the $\overline{\text{NMI}}$ interrupt pin, an interrupt cannot be prohibited. Connect it to the Vcc pin if unused.
 - Do not get into stop mode or wait mode with the $\overline{\text{NMI}}$ pin set to “0”.

3.1.6 Noise

To reduce the possibility of noise problems:

- Connect a bypass capacitor (approximately 0.1 μF) across the Vss pin and the Vcc pin with the shortest possible wiring
- Use circuit traces with a larger diameter than other signal traces for Vss and Vcc.

3.1.7 Stop Mode and Wait Mode

- When returning from stop mode by hardware reset, RESET pin must be set to “L” level until main clock oscillation is stabilized.
- When entering either wait or stop mode, you must first enable any interrupts you want to cancel the wait or stop. Also, make sure to disable any interrupts that you don't want to cancel the wait or stop. If only hardware reset or $\overline{\text{NMI}}$ interrupts are desired to cancel wait or stop, all other interrupt priority levels should be set to “0”.



Usage Precautions

3.1.8 Timer A (timer mode)

- Reading the Timer Ai register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the Timer Ai register with the reload timing gets “FFFF₁₆”. Reading the Timer Ai register after setting a value in the Timer Ai register with a count halted but before the counter starts counting gets a proper value.

3.1.9 Timer A (event counter mode)

- Reading the Timer Ai register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the Timer Ai register with the reload timing gets “FFFF₁₆” by underflow or “0000₁₆” by overflow. Reading the Timer Ai register after setting a value in the Timer Ai register with a count halted but before the counter starts counting gets a proper value.
- When counting is stopped in free-run type, set the timer again.
- When using Free-run type, the timer’s register contents may be unknown when counting starts. Set the timer value immediately after counting has started.

3.1.10 Timer A (pulse width modulation mode)

- The Timer Ai interrupt request bit becomes “1” if setting operation mode of the timer in compliance with any of the following procedures:
 - Selecting PWM mode after reset.
 - Changing operation mode from timer mode to PWM mode.
 - Changing operation mode from event counter mode to PWM mode.

Therefore, to use Timer Ai interrupt (interrupt request bit), set Timer Ai interrupt request bit to “0” after the above listed changes have been made.

- Setting the count start flag to “0” while PWM pulses are being output causes the counter to stop counting. If the TAIOUT pin is outputting an “H” level in this instance, the output level goes to “L”, and the Timer Ai interrupt request bit goes to “1”. If the TAIOUT pin is outputting an “L” level in this instance, the level does not change, and the Timer Ai interrupt request bit does not become “1”.

3.1.11 Timer B (timer mode)

- Reading the Timer Bi register while a count is in progress allows reading, with arbitrary timing, the value of the counter. Reading the Timer Bi register with the reload timing gets “FFFF₁₆”. Reading the Timer Bi register after setting a value in the Timer Bi register with a count halted but before the counter starts counting gets a proper value.

3.1.12 UART2

When using UART2 in clock asynchronous serial I/O mode (UART), use the internal clock only, otherwise, one of the following may occur:

- The interrupt may not be issued at the end of the data transmission when the hardware transfers the data from the transmit buffer to the transmit register.
- Data may be corrupted when the hardware transfers data from the transmit buffer register to the transmit register. This only applies to UART2 asynchronous serial I/O mode and does not apply to UART0 or UART1.

3.1.13 USB

USB SFR refers to registers from 0x0300 to 0x033C. All these registers are physically inside the USB block and are affected by the USB reset. Also, these registers can only be accessed by 8-bit mode. USB related registers 0x00C, 0x03DB-0x3DF are not inside the USB block and are not affected by a USB reset and can be accessed by 8 or 16 bits.



Usage Precautions

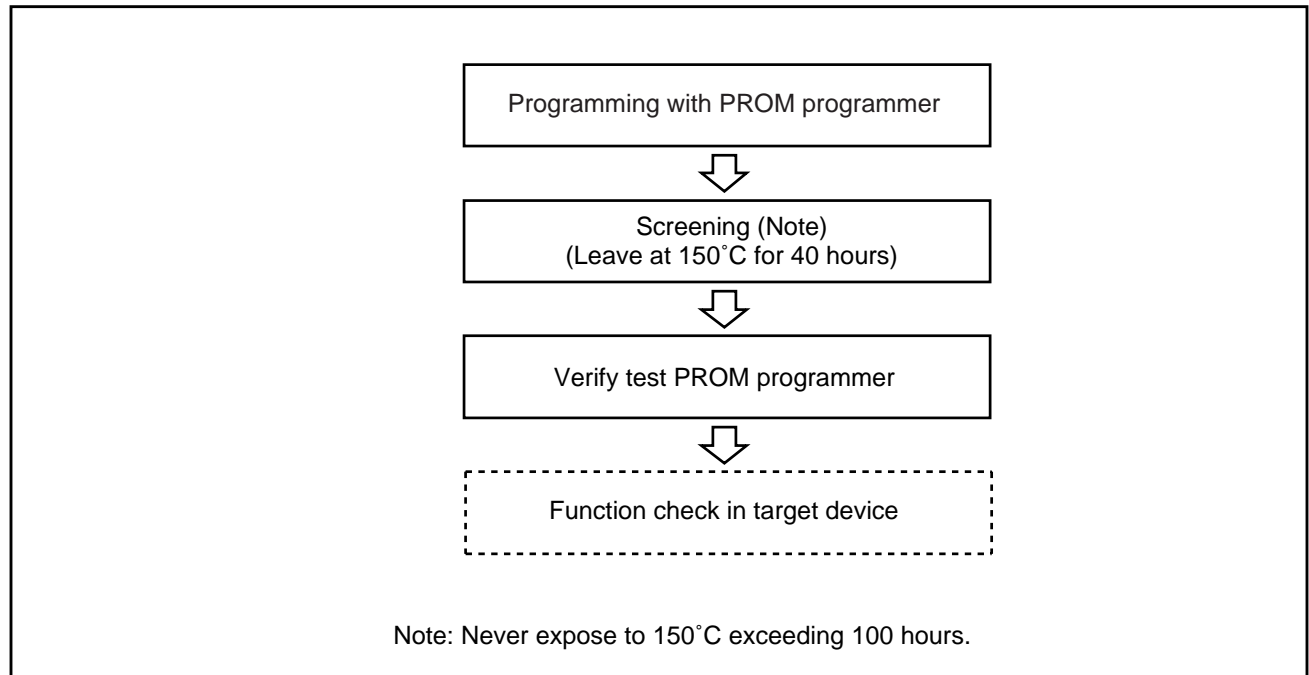


Figure 1.115: Programming and test flow for One-time PROM (OTP) version

Electrical

4.0 Specifications

4.1 Electrical

Table 1.38: Absolute maximum ratings only, not operating conditions

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}	Supply voltage	$V_{CC}=AV_{CC}$	-0.3 to 6.5	V
AV_{CC}	Analog supply voltage	$V_{CC}=AV_{CC}$	-0.3 to 6.5	V
V_I	Input voltage	Port0, Port1, Port2, Port3, Port6, Port7, Port8, Port10, RESET, VREF, XIN	-0.3 to $V_{CC}+0.3$	V
V_I	Input voltage	CNVss	-0.3 to 6.5 (Note 1)	V
V_O	Output voltage	Port0, Port1, Port2, Port3, Port6, Port7, Port8 (except P85), Port10, RESET, VREF, XIN	-0.3 to $V_{CC}+0.3$	V
P_d	Power dissipation	$T_a=25^\circ\text{C}$	760	mW
T_{opr}	Operating ambient temperature		0 to 70	$^\circ\text{C}$
T_{stg}	Storage temperature		-65 to 150	$^\circ\text{C}$

Note 1: When writing to EPROM, CNVss rated value is -0.3 to 13 volts

Table 1.39: Recommended operating conditions

Symbol	Parameter	Standard			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.1	5.0	5.25	V
AV_{CC}	Analog supply voltage		V_{CC}		V
V_{SS}	Supply voltage		0		V
AV_{SS}	Analog supply voltage		0		V
V_{IH}	High input voltage	Port 0, Port1, Port2, Port3, Port6, Port7, Port8, Port10, RESET, VREF, XIN, CNVSS	$0.8V_{CC}$	V_{CC}	V
V_{IL}	Low input voltage	Port0, Port1, Port2, Port3, Port6, Port7, Port8, Port10, RESET, VREF, XIN, CNVSS	0	$0.2V_{CC}$	V
I_{oh} (peak)	High peak output current	Port0, Port1, Port3, Port6, P71, P73, P75, P77, P81 to P87, Port10		-10	mA
		P20 to P27, P70, P72, P74, P76, P80		-20	mA
I_{oh} (avg.)	High avg output current	Port0, Port1, Port3, Port6, P71, P73, P75, P77, P81 to P87, Port10		-5	mA
		P20 to P27, P70, P72, P74, P76, P80		-10	mA
ΣI_{oh} (peak)	High peak output current	P2, P3, P6, P7, P8 ₀ ~P8 ₂		-80	mA
		P0, P1, P8 ₃ ~P8 ₇ , P10		-80	mA
ΣI_{oh} (avg.)	High avg output current	P2, P3, P6, P7, P8 ₀ ~P8 ₂		-40	mA
		P0, P1, P8 ₃ ~P8 ₇ , P10		-40	mA
I_{ol} (peak)	Low peak output current	Port0, Port1, Port3, Port6, P71, P73, P75, P77, P81 to P87, Port10		10	mA
		P20 to P27, P70, P72, P74, P76, P80		20	mA
I_{ol} (avg.)	Low avg output current	Port0, Port1, Port3, Port6, P71, P73, P75, P77, P81 to P87, Port10		5	mA
		P20 to P27, P70, P72, P74, P76, P80		10	mA
ΣI_{ol} (peak)	Low peak output current	P2, P3, P6, P7, P8 ₀ ~P8 ₂		80	mA
		P0, P1, P8 ₃ ~P8 ₇ , P10		80	mA
ΣI_{ol} (avg.)	Low avg output current	P2, P3, P6, P7, P8 ₀ ~P8 ₂		40	mA
		P0, P1, P8 ₃ ~P8 ₇ , P10		40	mA
$f(Xin)$	Main clock input oscillation frequency		1	12	MHz

Note: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

Electrical

Table 1.40: Electrical characteristics (Vcc=4.1~5.25V, Vss=0V, Ta= 0°C~ 70°C, f(Xin) = 12MHz)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min	Typ	Max	
VOH	High output voltage	Port0, Port1, Port2, Port3, Port6, Port71, P73,P75,P77,Port8 (except P85), Port10	IOH = -5mA	3.0			V
VOH	High output voltage	Port 70,P72,P74,P76,P80	IOH = -10mA	3.0			V
VOH	High output voltage	Port0, Port1, Port2, Port3, Port6, Port71, P73,P75,P77,Port8 (except P85), Port10	IOH = -200μA	4.7			V
VOH	High output voltage	High-drive mode Port 2	IOH = -10mA	3.0			
VOH	High output voltage	Xout	high power	IOH = -1mA	3.0		V
			low power	IOH = -0.5mA	3.0		V
VOL	Low output voltage	Port0, Port1, Port2, Port3, Port6, Port71, P73,P75,P77,Port8 (except P85), Port10	IOL = 5mA			2.0	V
VOL	Low output voltage	High-drive mode Port 2	IOL = 10mA			2.0	V
VOL	Low output voltage	Port 70,P72,P74,P76,P80 NOTE 1	IOL= 10mA			2.0	V
VOL	Low output voltage	Port0, Port1, Port2, Port3, Port6, Port71, P73,P75,P77,Port8 (except P85), Port10	IOL = 200μA			0.45	V
VOL	Low output voltage	Xout	high power	IOH = 1mA		2.0	V
			low power	IOH = 0.5mA		2.0	V
VT+-VT-	Hysteresis	TA0in to TA4in, INT0 to INT1, ADTRG, CTS0, CTS1, CLK0, CLK1, TA2out to TA4out, NMI, K10 to K15		0.2		0.8	V
VT+-VT-	Hysteresis	RESET		0.2		1.8	V
Iih	High input current	Port0, Port1, Port2, Port3, Port6, Port7,Port8, Port10, RESET, CNVss	VI = 5V			5.0	μA
Iil	Low input current	Port0, Port1, Port2, Port3, Port6, Port7, Port8, Port10, RESET, CNVss	VI = 0V			-5.0	μA
RPULLUP	Pull-up resistance	Port0, Port1, Port2, Port3, Port6, Port7, Port8, Port10	VI = 0V	30	50	167	kΩ
RXIN	Feedback resistance, Xin				1.0		MΩ
VRAM	RAM retention voltage		When clock is stopped	2.0			V
Icc	Power supply current	Output pins open, other pins tied to Vss	Icc run with USB ON (Mask)			80	mA
			Icc run with USB ON (OTP)			95	mA
			Icc run with USB OFF			50	mA
			Ta=25°C clock stopped			1	μA
			Ta=70°C clock stopped			20	μA
			Ta=25°C wait mode with internal clocks ON			8	mA
			Ta=25°C wait mode with internal clocks OFF			4	mA

Note 1 Only high drive when Timer A is enabled and drive registers set for high drive mode.

Timing

Table 1.41: USB Electrical Characteristics (Vcc=4.1~5.25V, Vss=0V, Ta= 0°C~ 70°C, f(Xin) = 12MHz)

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min	Typ	Max	
VOH	D+, D-	I=18.3 mA, RX=33 Ω, VXcap =3.0 V	2.2			V
VOL	D+, D-	I=18.3 mA, RX=33 Ω, VXcap =3.0 V			0.8	V
Isusp	Suspend current	USB suspend mode, internal clock stopped			175	μA
Xcap	DC-DC converter voltage	DC-DC converter output voltage on Xcap pin	3.0	3.3	3.6	V

Note: See Fig. 122 for recommended configuration.

4.2 Timing

Table 1.42: A-D conversion characteristics (Vcc, Avcc = 4.1~5.25V, Vss=0V, Ta= 0°C~ 70°C, f(Xin) = 12MHz)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min	Typ	Max	
-	Resolution		VREF = VCC			10	Bits
-	Absolute accuracy	Sample and hold function not available	VREF = VCC = 5V			±3	LSB
		Sample and hold function available (10bit)	VREF = VCC = 5V			±3	LSB
		Sample and hold function available (8bit)	VREF = VCC = 5V			±2	LSB
R	Ladder resistance		VREF = VCC	10		40	kΩ
Gonave	Conversion time (10bit)			2.75			μs
tCONV	Conversion time (8bit)			2.34			μs
tsAMP	Sampling time			0.25			μs
VREF	Reference voltage			2			V
VIA	Analog input voltage (min. operating frequency =x)			0		VREF	V
φAD	A-D clock frequency			1		12	MHz

Timing requirements referenced to Vcc = 4.1~5.25V, Vss=0V, Ta= 0°C~70°C unless otherwise specified.

Table 1.43: External clock input

Symbol	Parameter	Standard		Unit
		Min	Max	
tc	External clock input cycle time	83.3		ns
tw(H)	External clock input HIGH pulse width	33		ns
tw(L)	External clock input LOW pulse width	33		ns
tr	External clock rise time		15	ns
tf	External clock fall time		15	ns

Timing

Table 1.44: Timer A input (counter input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TAiIn input cycle time	100		ns
tw(TAH)	TAiIn input HIGH pulse width	40		ns
tw(TAL)	TAiIn input LOW pulse width	40		ns

Table 1.45: Timer A input (gating input in timer mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TAiIn input cycle time	400		ns
tw(TAH)	TAiIn input HIGH pulse width	200		ns
tw(TAL)	TAiIn input LOW pulse width	200		ns

Table 1.46: Timer A input (external trigger input in one-shot timer mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TAiIn input cycle time	200		ns
tw(TAH)	TAiIn input HIGH pulse width	100		ns
tw(TAL)	TAiIn input LOW pulse width	100		ns

Table 1.47: Timer A input (external trigger input in pulse width modulation mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tw(TAH)	TAiIn input HIGH pulse width	100		ns
tw(TAL)	TAiIn input LOW pulse width	100		ns

Table 1.48: Timer A input (up/down input in event counter mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input HIGH pulse width	1000		ns
tw(UPL)	TAiOUT input LOW pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

Table 1.49: A-D trigger input

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(AD)	AD _{TRG} input cycle time (triggerable minimum)	1000		ns
tw(ADL)	$\overline{\text{AD}}_{\text{TRG}}$ input LOW pulse width	125		ns



Timing

Table 1.50: Serial I/O

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(CK)	CLKi input cycle time	200		ns
tw(CKH)	CLKi input HIGH pulse width	100		ns
tw(CKL)	CLKi input LOW pulse width	100		ns
td(C-Q)	TxDi output delay time		80	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	30		ns
th(C-D)	RxDi input hold time	90		ns

Table 1.51: External interrupt INTi inputs

Symbol	Parameter	Standard		Unit
		Min	Max	
tw(INH)	INTi input HIGH pulse width	250		ns
tw(INL)	INTi input LOW pulse width	250		ns

Timing Diagrams- Peripheral/interrupt

4.3 Timing Diagrams- Peripheral/interrupt

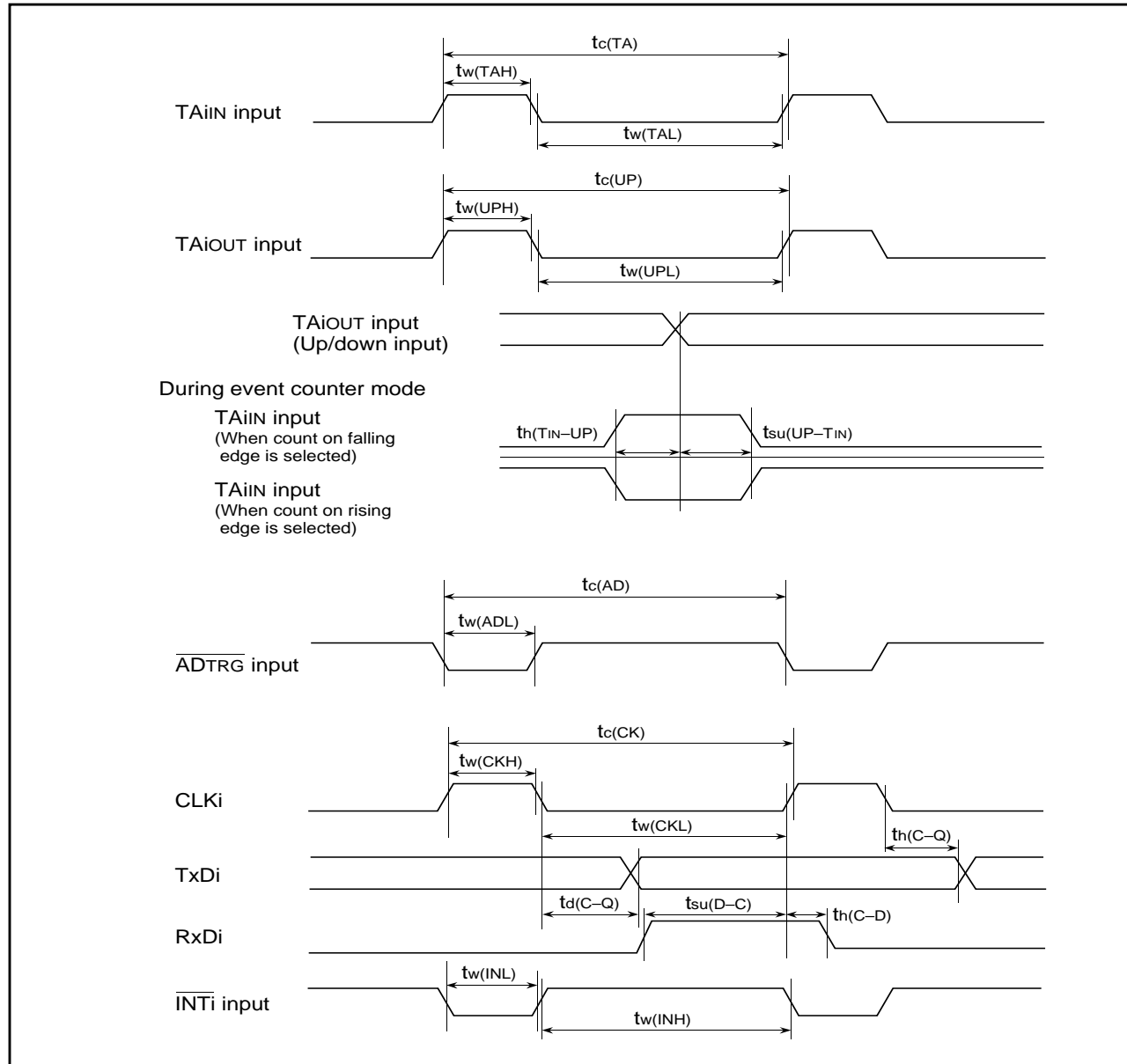


Figure 1.116: Peripheral / Interrupt timing diagram



5.0 Applications

5.1 Frequency Synthesizer Interface and DC-DC Converter

This section presents the recommended method of setting up and using the frequency synthesizer that generates the 48MHz clock needed by the USB FCU and the DC-DC converter that provides power to the D+/D- drivers

5.1.1 Reset of USB Related Registers

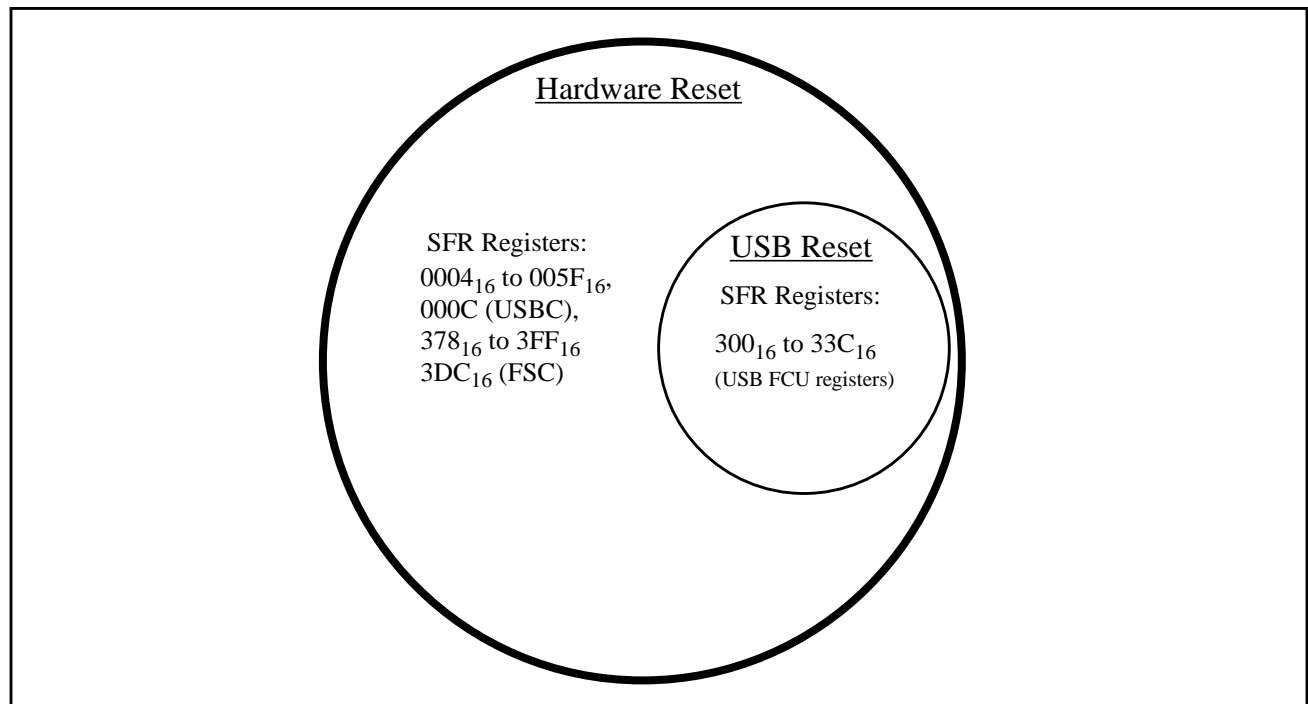


Figure 1.117: SFR Reset Venn Diagram

The special function registers (SFRs) that govern the operation of the frequency synthesizer, DC-DC converter and USB FCU are affected by one or more reset events. The addresses of the special function registers (SFRs) that are affected by Hardware Reset, USB Reset, or both are shown in Figure 1.117.

All resettable SFRs, including SFRs and other registers internal to the USB FCU, are affected by a Hardware Reset, which occurs when the $\overline{\text{RESET}}$ pin is brought low or an undefined opcode is fetched. See Section 2.4 for a complete listing of SFRs and their reset values.

Only registers internal to the USB FCU are reset when a USB Reset sent by the Host/Hub is detected. These USB registers are reset to their default values except for bit 5 of USBIS2 (USB Reset Interrupt Status Flag), which is set to a "1". USB FCU registers are registers from address 300₁₆ to 33C₁₆ and all other registers within the USB FCU, many of which the MCU does not have direct access to (e.g. FIFO address pointers). The USB FIFO registers are empty after USB reset because the FIFO address pointers are reset. However, the physical contents of the FIFOs are not set to all '1's or all '0's. Other SFRs such as USBC, FSC, and CM0, CM1 are not affected by a USB Reset.



5.1.2 Set up of Frequency Synthesizer and DC-DC Converter

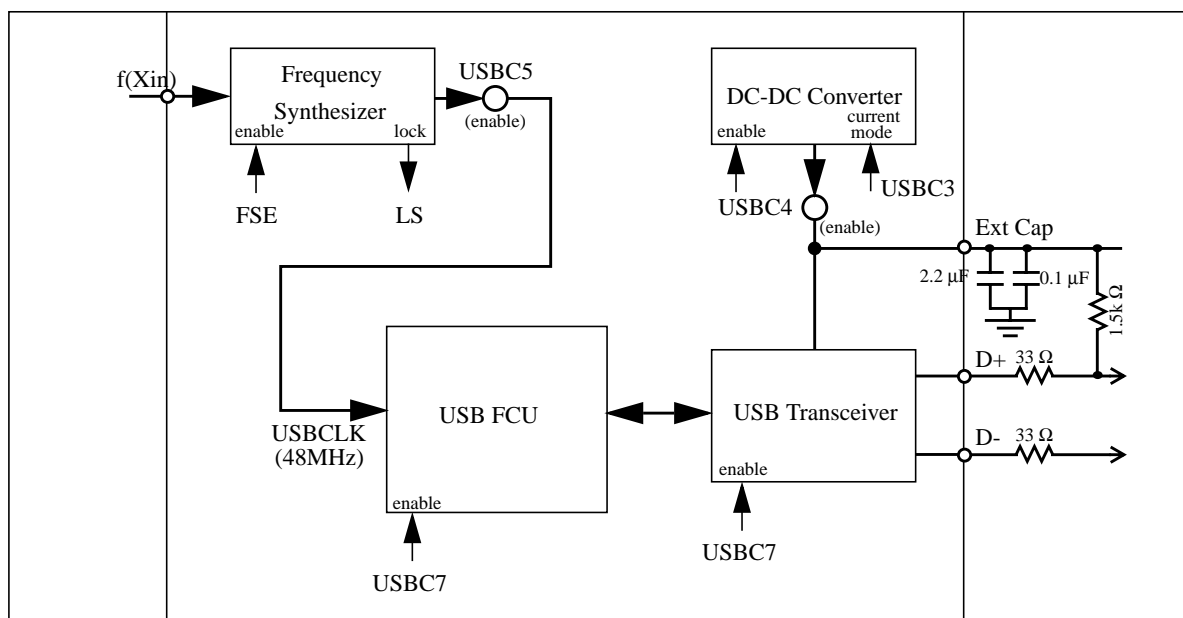


Figure 1.118: PLL, DC-DC Converter and USB Functional Block Diagram

A functional block diagram of the USB system on the M30240 which shows how the control signals affect operation is given in Figure 1.118

5.1.2.1 Set up after Hardware Reset

A Hardware Reset occurs when either the $\overline{\text{RESET}}$ pin is brought low for more than 2 μs or an invalid opcode is fetched by the CPU. The frequency synthesizer (PLL) and DC-DC converter should be set up as follows in the Hardware Reset routine (see Figure 1.119),

- Power up the M30240 and other components on the peripheral device for less than 100 mA operation. The current limit only applies for bus powered devices.
- Configure the PLL for 48MHz $f(\text{VCO})$ operation.
- Enable the PLL by setting FSE (bit 0 of the Frequency Synthesizer Control Register (FSC)) to a "1", then wait for 2 ms.
- Check the lock status bit (LS, bit 7 of FSC).
 - If the bit is a "1", go on.
 - If the bit is a "0", wait 0.1 ms longer and then re-check the bit.
- Enable the DC-DC converter in high current mode by setting USBC4 (bit 4 of the USB Control Register (USBC)) to a "1" and keeping USBC3 (bit 3 of USBC) a "0". High current mode should always be used during normal USB operation. Low current mode should only be used during a USB suspend.
- Wait $(C + 1)\text{ms}$ (where C equals the external capacitance connected to the Ext Cap pin in μF) for the voltage on Ext Cap to reach a steady state voltage of approximately 3.3V. (Since the D+ pullup is connected to the Ext Cap pin, the upstream hub will detect that the peripheral device has been plugged in once the voltage on D+ reaches approximately 2.0 V.)
 - Example: A 2.2 μF capacitor connected to Ext Cap requires 3.2 ms for the voltage on Ext Cap to be stable.



- Enable the USB clock by setting USBC5 (bit 5 of USBC) to a “1”. (If the USB clock and FCU are enabled before the voltage on Ext Cap is stable, a phantom USB Reset may be detected, or the actual USB Reset may not be detected.)
- Wait at least 4 cycles of Φ , then enable the USB FCU by setting USBC7 (bit 7 of USBC) to a “1”.
- Enable other blocks as necessary.

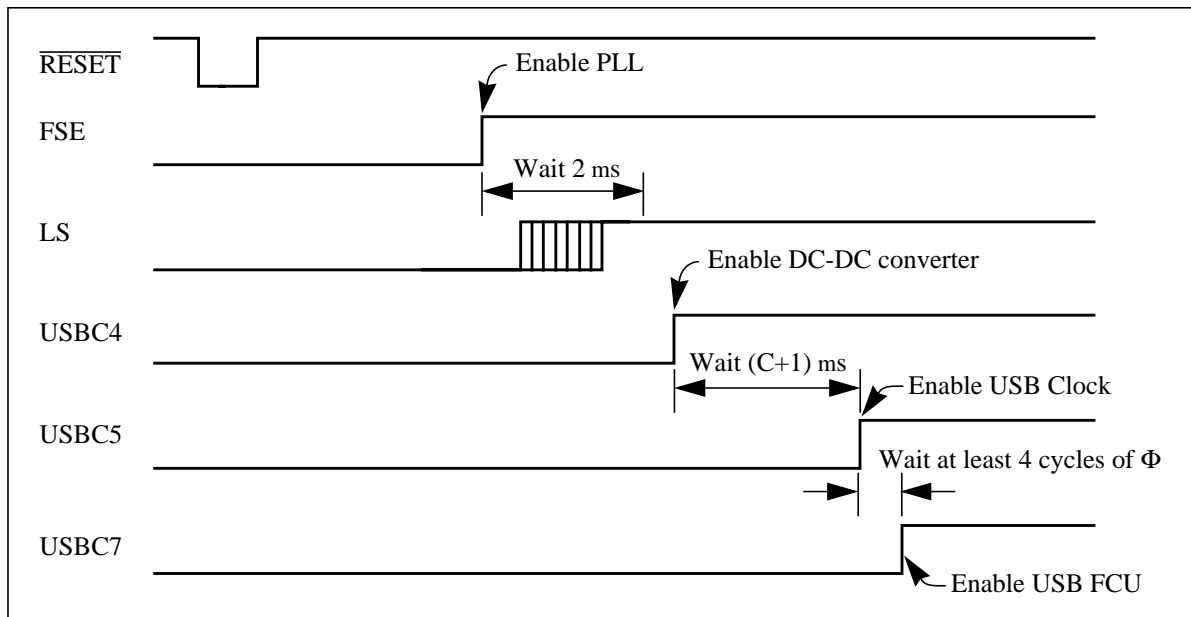


Figure 1.119: PLL and DC-DC Converter Set Up Timing after Hardware Reset

5.1.2.1.1 Precautions after Software Reset

A software reset occurs after writing a ‘1’ to bit ‘3’ of the processor mode register 0 (address 0004₁₆). During software reset, the contents of the internal RAM are preserved as well as all USB, DC-DC converter, and PLL registers. If the PLL is used as the system clock source, it is important to note that after a software reset occurs, any writes to the frequency synthesizer register will cause it to freeze. This can cause erratic device behavior. In order to avoid this, it is recommended that the following procedure be used:

- Prior to software reset, switch device clock source from ‘fsyn to f(Xin)’. Please see the Frequency Synthesizer specification for more details.
- After software reset using firmware, evaluate the condition of the synthesizer control register (FSC register, address 03DC₁₆, bit ‘0’). This bit is not effected by a software reset and can check to see if the PLL is still enabled. If so, any setup routine that involves writing to the PLL registers should not be called. At this point, the clock source can be changed back to fsyn.

5.1.2.2 Set up after USB Reset Signaling Detected

A USB Reset is detected by the USB FCU when an SE0 is present on D+/D- for at least 2.5 μ s. Detection of a USB Reset results in bit 5 of USB Interrupt Status Register 2 (USBIS2) being set to a “1” and the registers within the USB FCU being reset to their default values. Register USBC and the PLL registers are not affected by a USB Reset. A USB Function Interrupt request is also generated when the USB Reset is detected.

No modifications to the frequency synthesizer or DC-DC converter configuration should be made in the USB Function Interrupt routine. However, all USB FCU registers (addresses 300₁₆ to 33C₁₆) must be reconfigured to their pre-enumeration state.



5.1.2.3 Set up after USB Suspend Detected

A USB Suspend occurs if the USB FCU does not detect any bus activity on D+/D- for at least 3 ms. Detection of a suspend results in bit 7 of USBIS2 and bit 0 of USBPM (SUSPEND) being set to a "1". This causes bit 3 of SUSPIC to be set to a "1". Bit 7 of USBIS2 then needs to be cleared by writing a "1" to the bit in order to allow a future suspend event.

The configuration of the frequency synthesizer and DC-DC converter should be changed as follows in the USB Suspend Interrupt routine (if the device is bus powered):

- Change the DC-DC converter from high current mode to low current mode by setting USBC3 (bit 3 of the USBC) to a "1"
- Disable the USB clock by setting USBC5 (bit 5 of USBC) to a "0". Once the USB clock is disabled, registers internal to the USB FCU should not be written to. This includes all USB SFRs from address 0300₁₆ to 033C₁₆. It does not include USBC or FSC.
- Perform other tasks to reduce total current to below 500μA.
- Disable the PLL by setting FSE (bit 0 of FSC) to a "0".
- Make sure the I-FLAG is set to "1".
- Stop the system clock by setting CM10 (bit 0 of CM1) to a "1". Make sure to first enable writing to the system clock control register by setting PRCO (bit 0 of PRCR) to "1". Also, make sure to enable the USB Resume Interrupt (RSMIC register) and clear or execute any pending interrupts prior to stopping the clock so the MCU can wake up once resume signaling is detected. If the clock is stopped using an interrupt routine, make sure to set the priority of the Resume Interrupt (RSMIC) higher than the current interrupt.
- Note that no action may be necessary if the device is self powered.

5.1.2.4 Set up after USB Resume Signaling Detected

A resume occurs when the USB FCU is in the suspend state and detects a non-idle signaling on D+/D-. Detection of a resume results in bit 6 of USBIS2 and bit 1 of USBPM (RESUME) being set to a "1". This causes bit 3 of RSMIC to also be set to "1". If the MCU was in the stop state prior to the detection of the resume, the USB Resume Interrupt request will cause the MCU to wake up from the stop state. Bit 6 of USBIS2 needs to be cleared (by writing a "1" to the bit) in order to allow a future resume event. See section 2.9 "Stop Mode" for details on waking up from the stop state.

The configuration of the frequency synthesizer and DC-DC converter should be changed as follows in the USB Resume Interrupt routine (if the device is bus powered):

- Re-enable the PLL for 48MHz f(VCO) by setting FSE (bit 0 of the FSC) to a "1", then wait for 2 ms.
- Wait for 2 ms.
- Check the lock status bit (LS, bit 7 of FSC).
 - If the bit is a "1", continue.
 - If the bit is a "0", wait 0.1 ms longer and then re-check the bit.
- Enable the USB clock by setting USBC5 (bit 5 of USBC) to a "1".
- Wait for a minimum of 4 cycles.
- Change the DC-DC converter from low current mode to high current mode by setting USBC3 (bit 3 of the USBC) to a "0".
- Enable other blocks as necessary.

Registers internal to the USB FCU should not be written to until the USB clock is re-enabled. This includes all USB SFRs from address 0300₁₆ to 033C₁₆. It does not include USBC or FSC.

Note that the configuration changes described above may not need to be made if the MCU was not placed in a suspend state as described in section 5.1.2.3 Set up after USB Suspend Detected.



Attach/Detach Function

5.1.2.5 PLL Lock Bit

The PLL lock bit is used to indicate when the PLL is first locked. Accordingly, after the PLL is enabled and it has been given 2.0 ms to stabilize, the lock bit status should be checked. Once the lock bit is HIGH, the USB check should be enabled. After this stage, the lock bit is no longer valid and should not be monitored, unless the PLL is re-enabled.

5.2 Attach/Detach Function

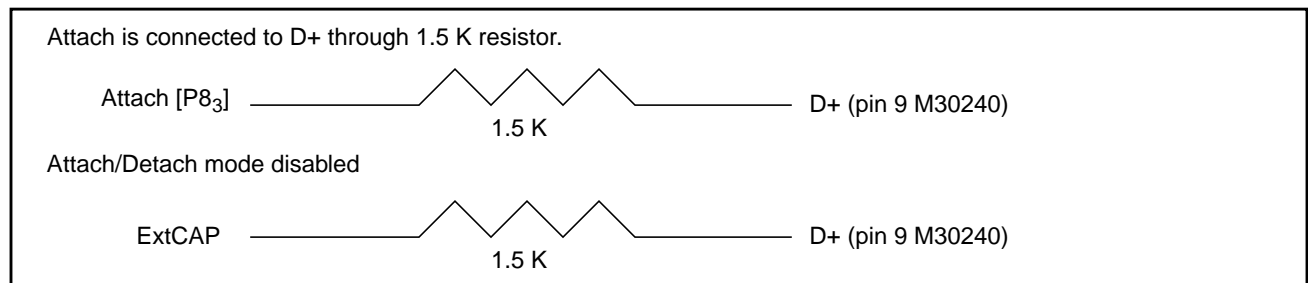
The Attach/Detach Function can be used to attach or detach a USB function from the host without disconnecting the cable. When attaching a USB function, the connect registers should be set to 3 Hex at the same time on or before the DC-DC Converter is enabled. Similarly, when detaching the connect register, it should be set to 1 Hex when powering down the DC-DC Converter.

If you do not set the connect (address 1fh) to HIGH, the system will default to its normal mode.

Note: If the D+ is connected to ExtCAP, this mode will not work.

D+ is connected to ExtCAP through a 1.5 K resistor in compliance with the USB specification. USB Suspend/Resume Function

Hardware connections are shown below



Low Pass Filter Network

5.3 Low Pass Filter Network

All passive components should be in close proximity to pin 78 (LPF), capacitors should be X7R dielectric or better. The recommended values are listed in Table 1.52 . See Figure 1.120 for schematic of the LPF.

Table 1.52: Recommended Values

R = 1000 Ω	10%
C2 = 680 pf	10%
C1 = 0.1 μ f	10%

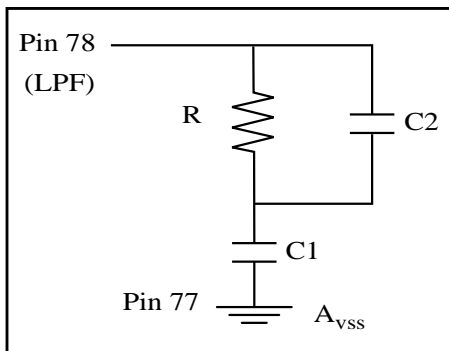


Figure 1.120: LPF Filter Schematic

Analog V_{SS} and Analog V_{CC} , pins 77 and 80 should have isolated connections to the digital V_{SS} and V_{CC} ground planes. Figure 1.121 illustrates the power supply isolation.

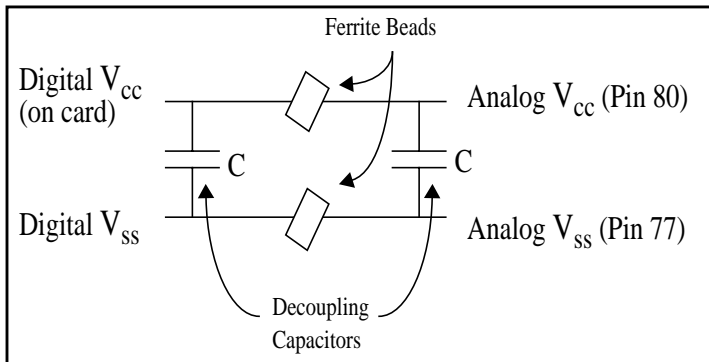


Figure 1.121: Power Supply

USB Transceiver

5.4 USB Transceiver

When using the on-chip voltage converter to supply the necessary 3.3V to the driver circuit, a capacitor network must be connected between Ext. Cap (pin 6) and V_{SS} (pin 13). Two capacitors are required as shown in Figure 1.122. The high frequency 0.1 μF capacitor should be an X7R type or better. The low frequency decoupling capacitor of 2.2 μF should be of tantalum di-electric or better. The start-up time for this value of the capacitor is 3.2 ms, approximately $(1\text{ms}/\mu\text{F}) + 1\text{ms}$.

After enabling the on-chip voltage converter, a certain amount of time must pass before a wait or stop clock instruction is executed. The amount of time is given by $(C+1)\text{ms}$, when C is the value in μF of the external capacitance connected to the Ext. Cap pin. For example, if the external capacitance is 2.2 μF , at least 3.2 ms must elapse from the time that the on-chip voltage converter is enabled until a WAIT instruction or STOP command ($\text{CM}10 = 1$) is executed.

In order to meet the impedance matching requirements of the USB Specification, a 33 Ω resistor must be added to USB D+ (pin 9) and to USB D- (pin 10). In addition, capacitors connected between USB D+ and USB D- or USB D+/D- and V_{SS} may need to be added for rise/fall time matching and edge control. These capacitors should be placed after the 33 Ω resistors. Their configuration and values will depend on the PCB layout. The placement of external components is illustrated in Figure 1.122.

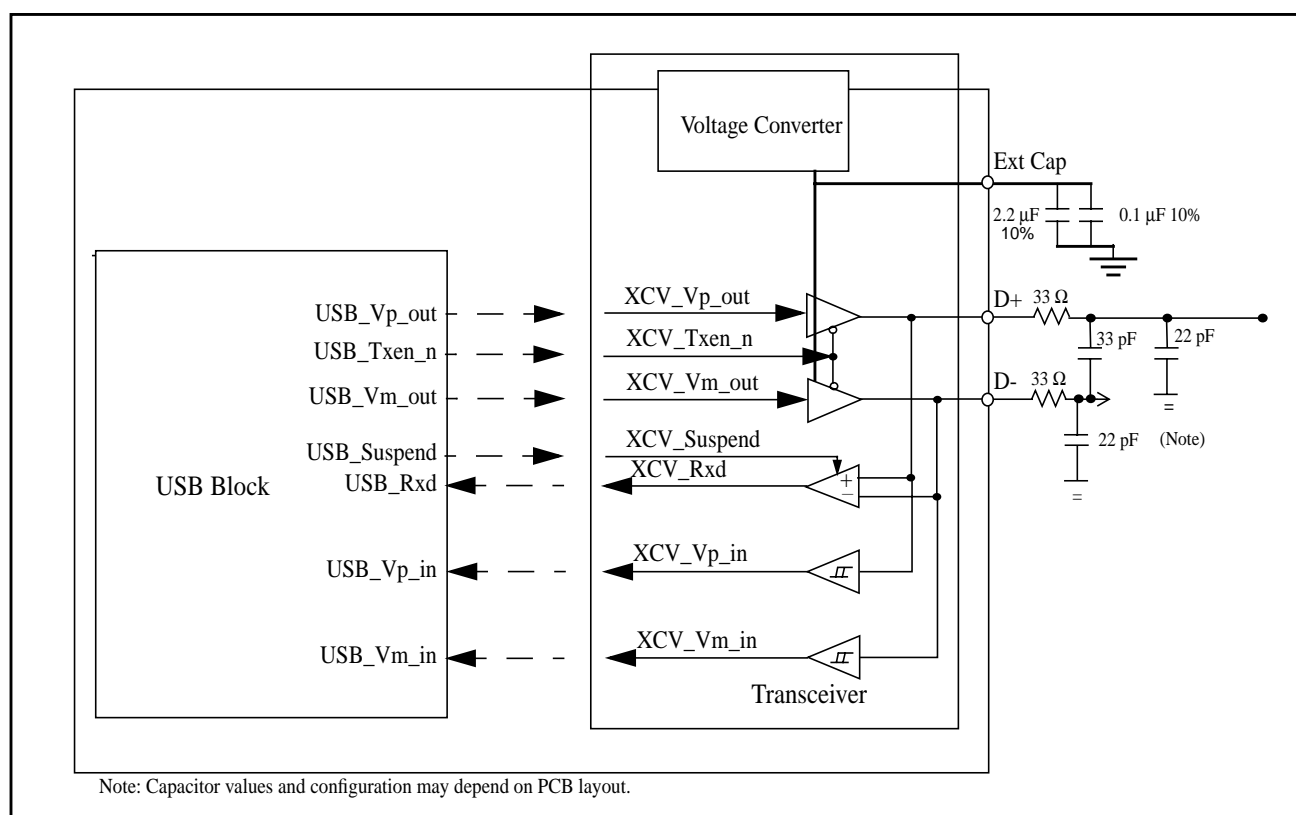


Figure 1.122: Configuration of External USB components

5.5 Programming Notes

5.5.1 Accessing USB IN/OUT CSR Registers

Do not use read-modify-write instruction on these registers because they contain control and status bits that can be changed by both hardware and software. There is a possibility that using a read-modify-write instruction might cause incorrect data to be written back to these registers. See Table 1.53 for a list of bits that may have incorrect data written to them and the value you should write back in order to prevent this from occurring.

Table 1.53: Bits that might have incorrect data

Register name	Bit name	Value to write for “No change”
EP0CS	IN_PKT_RDY (b1)	“0”
	DATA_END (b3)	“0”
	FORCE_STALL (b4)	“1”
EPxICS (x = 1-4)	IN_PKT_RDY (b0)	“0”
	UNDER_RUN (b1)	“1”
EPxOCS (x = 1-4)	OUT_PKT_RDY (b0)	“1”
	OVER_RUN (b1)	“1”
	FORCE_STALL (b4)	“1”
	DATA-ERR (b5)	“1”

The endpoint 1-4 IN CSR’s (EPiICS, i = 1-4) have a bit IN_PKT_RDY (bit 0) that is set to a “1” by the firmware after a packet of data is loaded to the respective endpoint’s FIFO. This signifies that a packet is ready for transmission. If the firmware wants to send a NULL packet to the host, it can simply write a “1” to the IN_PKT_RDY bit without loading data to the FIFO. This bit is cleared by the hardware. If the firmware manipulates (writes) the IN CSR for a purpose other than to signify to the hardware that a data packet is ready for transmission (for instance, set/reset ISO bit, set/reset SEND_STALL bit), it must make sure that a “0” is written back to the IN_PKT_RDY bit. Failure to do so could cause improper operation of the device. Writing a “0” to the IN_PKT_RDY bit has no effect on its state.

The endpoint 1-4 OUT CSRs (EPiICS, i = 1-4) have a bit OUT_PKT_RDY (bit 0) that is set to a “1” by the hardware after a packet of data is received from the host to the respective endpoint’s FIFO. This signifies that a packet is ready for download. This bit is cleared by the firmware by writing a “0” to it after the data packet is unloaded from the FIFO. If the firmware manipulates (writes) the OUT CSR for a purpose other than to signify to the hardware that a data packet has been unloaded (for instance, set/reset ISO bit, set/reset SEND_STALL bit), it must make sure that a “1” is written back to the OUT_PKT_RDY bit. Failure to do so could cause improper operation. Writing a “1” to the OUT_PKT_RDY bit has no effect on its state.



Programming Notes

Below is an example of how to set/reset the ISO bit of the IN CSR register (for initializing the respective endpoint as an isochronous endpoint):

```
[R1L] = [EPIICS].B
OR.B #08H, R1L      ;set ISO bit = 1, write "1" back to UNDER_RUN bit
AND.B #0FEH, R1L   ;write "0" back to IN_PKT_RDY bit
[EPIICS].B = [R1L]
[R1L] = [EPIICS].B
OR.B #02, R1L      ;write "1" back to UNDER_RUN bit
AND.B #0F6H, R1L   ;reset ISO bit = 0, write "0" back to IN_PKT_RDY bit
[EPIICS].B = [R1L]
```

5.5.2 USB Consecutive Set Address

The USB Specification states that the host can send a SET_ADDRESS request for the following cases:

1. During enumeration when the device is in default state. (The host assigns a non-zero address.)
2. When the device is in the address state. (The host can re-assign a new address.)

The device handles case #1 (when the device is in the default state) and case #2 (when the device is in the address state) differently. The following is a segment of code to illustrate the program flow to properly deal with these cases.

```
DEFAULT_STATE:
  If [USBA].B ==0
    [USBA].B = wValue_lo      ;If the device is in default state, update address before STATUS
                              ;completion
    R1L = [EPOCS].B          ;USB ENDPOINT 0 CSR
    OR.B #48H, R1L          ;Set serviced_out_pkt_rdy & data_end
    [EPOCS].B = R1L
    wait for the completion of the
    JMP ADDR_END
  else
    ADDR_STATE
    R1L [EPOCS].B          ;USB ENDPOINT 0 CSR
    OR.B #48H, R1L          ;Set serviced_out_pkt_rdy & data_end
    [EPOCS].B = R1L
    wait for the completion of the
    [USBA].B = wValue_lo    ;If the device is in address state, update address before STATUS
                              ;completion
    ADDR_END
  endif
end of the set_address routine
```

Note: wValue_lo = assigned address from the host in SET-ADDRESS request.