SDR SDRAM E0342M21 (Ver.2.1) February 2004 (K) Japan

## **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM

## DESCRIPTION

M2V64S50ETP is a 4-bank x 524,288-word x 32-bit,

synchronous DRAM, with LVTTL interface. All inputs and outputs are referenced to the rising edge of CLK. The M2V64S50ETP achieve very high speed data rate up to 100MHz (-7), 133MHz (-6), 166MHz(-5), and are suitable for digital consumer products or graphic memory in computer systems.

## FEATURES

- Single 3.3v + 0.3V power supply
- Max. Clock frequency -5:PC166<3-3-3> / -6:PC133<3-3-3> / -7:PC100<2-2-2>
- Fully Synchronous operation referenced to clock rising edge
- Single Data Rate
- 4 bank operation controlled by BA0, BA1 (Bank Address)
- /CAS latency- 2/3 (programmable)
- Burst length- 1/2/4/8/full page (programmable)
- Burst type- sequential / interleave (programmable)
- Random column access
- Auto precharge / All bank precharge controlled by A10
- Auto refresh and Self refresh
- 4096 refresh cycles /64ms (4 banks concurrent refresh) (x32)
- Address Input,
- Row address A0-10 / Column address A0-7 (x32)
- LVTTL Interface
- Package type,

M2V64S50ETP: 0.5mm lead pitch 86-pin TSOP(II) (x32)

-Low Power for the Self Refresh Current

Low Power Version : ICC6  $\leq$  500uA (-5L, -6L, -7L)

#### **Operating Frequencies**

	Max. Frequency @CL=2 *	Max. Frequency @CL=3 *	Standard
M2V64S50ETP -5/-5L	133MHz	166MHz	PC166(CL3)
M2V64S50ETP -6/-6L	100MHz	133MHz	PC133(CL3)
M2V53S50ETP -7/-7L	100MHz	100MHz	PC100(CL2)

\* CL = CAS(Read) Latency

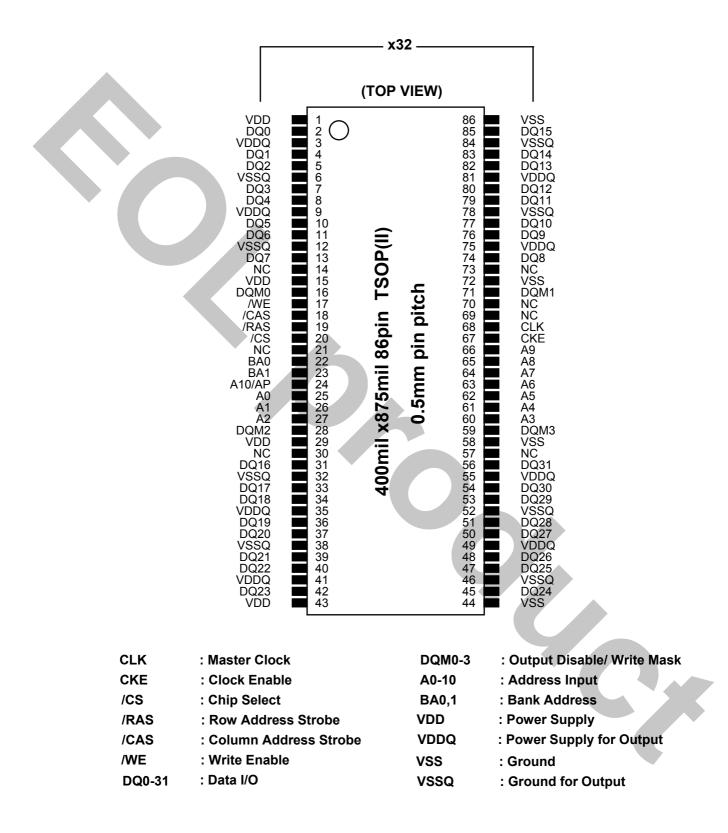
Remark: The -5L/-6L/-7L is ICC6(Self-refresh) low power version. (ICC6 < 500uA)

This Product became EOL in August, 2004.



## **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM

## **PIN CONFIGURATION**



SDR SDRAM E0342M21 (Ver.2.1) February 2004 (K) Japan

## M2V64S50ETP

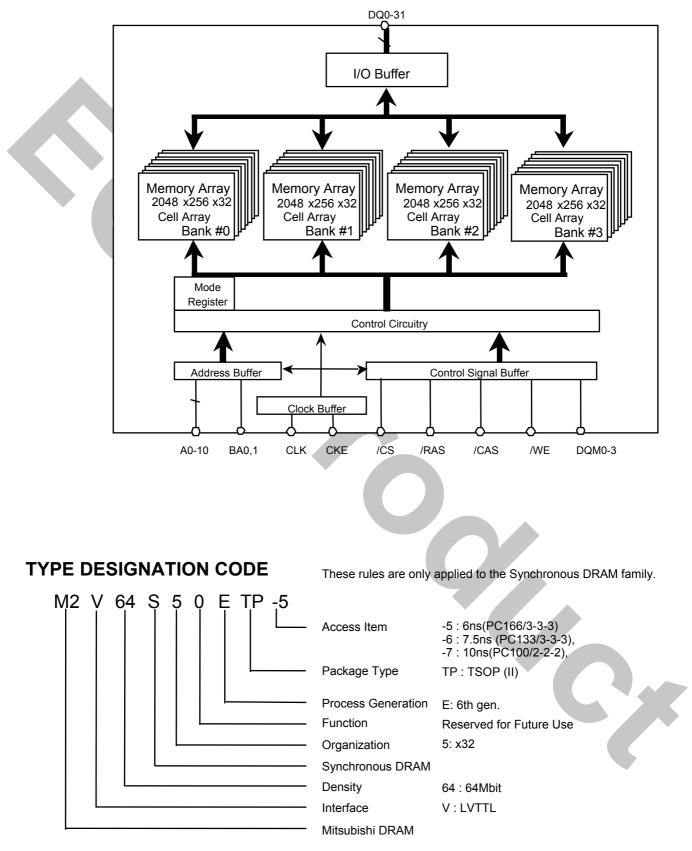
64M Single Data Rate Synchronous DRAM

-	PIN FUNCTIO	N	
	CLK	Input	Master Clock: All other inputs are referenced to the rising edge of CLK.
	СКЕ	Input	Clock Enable: CKE controls internal clock. When CKE is low, internal clock for the following cycle is ceased. CKE is also used to select auto / self refresh. After self refresh mode is started, CKE becomes asynchronous input. Self refresh is maintained as long as CKE is low.
	/CS	Input	Chip Select: When /CS is high, any command are masked except CLK, CKE and DQM
	/RAS, /CAS, /WE	Input	Combination of /RAS, /CAS, /WE defines basic commands.
	A0-11	Input	A0-11 specify the Row / Column Address in conjunction with BA0,1. The Row Address is specified by A0-10(x32). The Column Address is specified by A0-7. A10 is also used to indicate precharge option. When A10 is high at a read / write command, an auto precharge is performed. When A10 is high at a precharge command, all banks are precharged.
	BA0,1	Input	Bank Address: BA0,1 specifies one of four banks to which a command is applied. BA0,1 must be set with ACT, PRE, READ, WRITE commands.
	DQ0-31(x32)	Input / Output	Data In and Data out are referenced to the rising edge of CLK.
	DQM0-3(X32)	Input	Din Mask / Output Disable: When DQM is high in burst write, Din for the current cycle is masked. When DQM is high in burst read, Dout is disabled at the next but one cycle.
	VDD, VSS	Power Supply	Power Supply for the memory array and peripheral circuitry.
	VDDQ, VSSQ	Power Supply	VDDQ and VSSQ are supplied to the Output Buffers only.

SDR SDRAM E0342M21 (Ver.2.1) February 2004 (K) Japan

# 64M Single Data Rate Synchronous DRAM

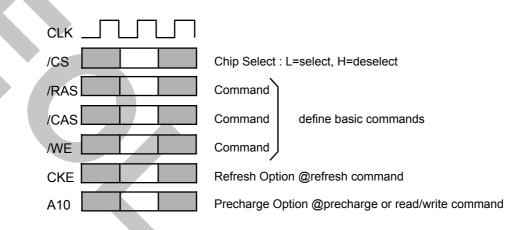
## **BLOCK DIAGRAM**



SDR SDRAM E0342M21 (Ver.2.1) February 2004 (K) Japan

## **BASIC FUNCTIONS**

The M2V64S50ETP provides basic functions, bank (row) activate, burst read / write, bank (row) precharge, and auto / self refresh. Each command is defined by control signals of /RAS, /CAS and /WE at CLK rising edge. In addition to 3 signals, /CS ,CKE and A10 are used as chip select, refresh option, and precharge option, respectively. To know the detailed definition of commands, please see the command truth table.



#### Activate (ACT) [/RAS =L, /CAS =/WE =H]

ACT command activates a row in an idle bank indicated by BA.

#### Read (READ) [/RAS =H, /CAS =L, /WE =H]

READ command starts burst read from the active bank indicated by BA. First output data appears after /CAS latency. When A10 =H at this command, the bank is deactivated after the burst read (auto-precharge, **READA**)

#### Write (WRITE) [/RAS =H, /CAS =/WE =L]

WRITE command starts burst write to the active bank indicated by BA. Total data length to be written is set by burst length. When A10 =H at this command, the bank is deactivated after the burst write (auto-precharge, **WRITEA**).

#### Precharge (PRE) [/RAS =L, /CAS =H, /WE =L]

PRE command deactivates the active bank indicated by BA. This command also terminates burst read /write operation. When A10 =H at this command, all banks are deactivated (precharge all, **PREA**).

#### Auto-Refresh (REFA) [/RAS =/CAS =L, /WE =CKE =H]

REFA command starts auto-refresh cycle. Refresh address are generated internally. After this command, the banks are precharged automatically.

## **M2V64S50ETP**

64M Single Data Rate Synchronous DRAM

#### **COMMAND TRUTH TABLE**

COMMAND	MNEMONIC	CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	BA0,1	A10 /AP	A0-9, 11	Note
Deselect	DESEL	Н	Х	Н	Х	Х	Х	Х	Х	Х	
No Operation	NOP	Н	Х	L	Н	Н	Н	Х	Х	Х	
Row Address Entry & Bank Activate	ACT	Н	х	L	L	Н	Н	V	V	V	
Single Bank Precharge	PRE	Н	х	L	L	Н	L	V	L	х	
Precharge All Banks	PREA	Н	Х	L	L	Н	L	Х	Н	Х	
Column Address Entry & Write	WRITE	Н	х	L	Н	L	L	V	L	V	
Column Address Entry & Write with Auto-Precharge	WRITEA	Т	х	L	Т	L	L	V	Н	V	
Column Address Entry & Read	READ	H	х	L	H	L	Η	V	L	V	
Column Address Entry & Read with Auto-Precharge	READA	H	x	L	Н	L	Н	V	Н	V	
Auto-Refresh	REFA	Н	Н	L	L	L	Н	Х	Х	Х	
Self-Refresh Entry	REFS	Н	L	L	-	L	Н	Х	Х	Х	
Self-Refresh Exit	REFSX	L	н	н	X	X	Х	X	X	X	
Duret Terreinete	трот										
											4
Mode Register Set	MRS	Н	X	L	L	L	L	L	L	V	1
-				=CLΚ α	cycle nu	Imber			C		
	Deselect No Operation Row Address Entry & Bank Activate Single Bank Precharge Precharge All Banks Column Address Entry & Write with Auto-Precharge Column Address Entry & Read Column Address Entry & Read with Auto-Precharge Auto-Refresh Self-Refresh Entry Self-Refresh Exit Burst Terminate Mode Register Set	DeselectDESELNo OperationNOPRow Address Entry & Bank ActivateACTSingle Bank PrechargePREPrecharge All BanksPREAColumn Address Entry & WriteWRITEColumn Address Entry & Write with Auto-PrechargeWRITEAColumn Address Entry & ReadREADColumn Address Entry & ReadREADSelf-Refresh Entry & Reefresh EntryREFASelf-Refresh Entry Burst TerminateREFSXH=High Level, L=Low Level, V=Valid, X	COMMANDMINEMONICn-1DeselectDESELHNo OperationNOPHRow Address Entry & Bank ActivateACTHSingle Bank PrechargePREHPrecharge All BanksPREAHColumn Address Entry & WriteWRITEHColumn Address Entry & WriteWRITEAHColumn Address Entry & ReadREADHColumn Address Entry & ReadREADHColumn Address Entry & ReadREADHSelf-Refresh Entry & Reaf with Auto-PrechargeREFAHSelf-Refresh Entry Burst TerminateREFSHMode Register SetMRSH	COMMANDMNEMONICn-1nDeselectDESELHXNo OperationNOPHXRow Address Entry & Bank ActivateACTHXSingle Bank PrechargePREHXPrecharge All BanksPREAHXColumn Address Entry & WriteWRITEHXColumn Address Entry & Write with Auto-PrechargeREADHXColumn Address Entry & ReadREADHXColumn Address Entry & ReadREADHHSelf-Refresh Entry & REFSHLHSelf-Refresh EntryREFAHLBurst TerminateTBSTHXMode Register SetMRSHX	COMMANDMINEMONICn-1n $ICS$ DeselectDESELHXHNo OperationNOPHXLRow Address Entry & Bank ActivateACTHXLSingle Bank PrechargePREHXLPrecharge All BanksPREAHXLColumn Address Entry & WriteWRITEHXLColumn Address Entry & Write with Auto-PrechargeREADHXLColumn Address Entry & ReadREADHXLColumn Address Entry & ReadREADHXLColumn Address Entry & ReadREADHXLColumn Address Entry & ReadREADAHLLSelf-RefreshREFAHHLLSelf-Refresh Entry & REFSREFAHLLSelf-Refresh Exit Mode Register SetMRSHXLH=High Level, L=Low Level, V=Valid, X=Don't Care, n=CLK orLL	COMMANDMINEMONICn-1n $ICS$ $IRAS$ DeselectDESELHXHXNo OperationNOPHXLHRow Address Entry & Bank ActivateACTHXLLSingle Bank PrechargePREHXLLPrecharge All BanksPREAHXLLColumn Address Entry & WriteWRITEHXLHColumn Address Entry & Write with Auto-PrechargeREADHXLHColumn Address Entry & ReadREADHXLHColumn Address Entry & ReadREADHXLHColumn Address Entry & ReadREADHXLHColumn Address Entry & ReadREADHXLHColumn Address Entry & ReadREADAHXLHMuto-PrechargeREFAHHLLSelf-Refresh EntryREFSHLLLSelf-Refresh Exit Mode Register SetMRSHXLHMode Register SetMRSHXLLLH=High Level, L=Low Level, V=Valid, X=Don't Care, n=CLK cycle nuHLL	COMMANDMINEMIONICn-1nICSIRASICASDeselectDESELHXHXXNo OperationNOPHXLHHRow Address Entry & Bank ActivateACTHXLLHSingle Bank PrechargePREHXLLHPrecharge All BanksPREAHXLLHColumn Address Entry & WriteWRITEHXLHColumn Address Entry & Write with Auto-PrechargeREADHXLHColumn Address Entry & ReadREADHXLHLColumn Address Entry & ReadREADHXLHLColumn Address Entry & ReadREADHXLHLColumn Address Entry & ReadREADAHXLLLColumn Address Entry & ReadREADAHXLLLColumn Address Entry & ReadREFSHLLLLSelf-RefreshREFSHHXXXSelf-Refresh Exit Mode Register SetMRSHXLHHHTerminateTBSTHXLHHHMSHXLLLLLHHXLLHHHXL <td< td=""><td><math display="block">\begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td><td>COMMANDMNEMONICn-1nICSIRASICASIWEBAO,TDeselectDESELHXHXXXXXNo OperationNOPHXLHHHXRow Address Entry &amp; Bank ActivateACTHXLLHHXSingle Bank PrechargePREHXLLHLVPrecharge All BanksPREAHXLLHLXColumn Address Entry &amp; WriteWRITEHXLHLLVColumn Address Entry &amp; WriteREADHXLHLLVColumn Address Entry &amp; ReadREADHXLHLLVColumn Address Entry &amp; ReadREADHXLHLHVColumn Address Entry &amp; ReadREADHXLHLHVColumn Address Entry &amp; ReadREADAHXLHLHVColumn Address Entry &amp; ReadREADAHXLHLHVColumn Address Entry &amp; ReadREFAHXLHLHVColumn Address Entry &amp; ReadREFAHHXLHXXXSelf-Refresh EntryREFAHHHLL<t< td=""><td>COMMANDMNEMONICn-1nICSIRASICASIVEBA0,1IAPDeselectDESELHXHXXXXXXNo OperationNOPHXLHHHXXXRow Address Entry &amp; Bank ActivateACTHXLLHHXXSingle Bank PrechargePREHXLLHHXLPrecharge All BanksPREAHXLLHLXHColumn Address Entry &amp; WriteWRITEHXLHLLVLColumn Address Entry &amp; Write with Auto-PrechargeREADHXLHLLVLColumn Address Entry &amp; ReadREADHXLHLLVLColumn Address Entry &amp; ReadREADHXLHLHVLColumn Address Entry &amp; Read with Auto-PrechargeREADAHXLHLHXXSelf-Refresh Entry Self-Refresh EntryREFSHLLLHXXXSelf-Refresh Exit Burst TerminateTBSTHXLHHXXXHXLHXLHHLILILSelf-Refresh Exit&lt;</td><td><math display="block">\begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td></t<></td></td<>	$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	COMMANDMNEMONICn-1nICSIRASICASIWEBAO,TDeselectDESELHXHXXXXXNo OperationNOPHXLHHHXRow Address Entry & Bank ActivateACTHXLLHHXSingle Bank PrechargePREHXLLHLVPrecharge All BanksPREAHXLLHLXColumn Address Entry & WriteWRITEHXLHLLVColumn Address Entry & WriteREADHXLHLLVColumn Address Entry & ReadREADHXLHLLVColumn Address Entry & ReadREADHXLHLHVColumn Address Entry & ReadREADHXLHLHVColumn Address Entry & ReadREADAHXLHLHVColumn Address Entry & ReadREADAHXLHLHVColumn Address Entry & ReadREFAHXLHLHVColumn Address Entry & ReadREFAHHXLHXXXSelf-Refresh EntryREFAHHHLL <t< td=""><td>COMMANDMNEMONICn-1nICSIRASICASIVEBA0,1IAPDeselectDESELHXHXXXXXXNo OperationNOPHXLHHHXXXRow Address Entry &amp; Bank ActivateACTHXLLHHXXSingle Bank PrechargePREHXLLHHXLPrecharge All BanksPREAHXLLHLXHColumn Address Entry &amp; WriteWRITEHXLHLLVLColumn Address Entry &amp; Write with Auto-PrechargeREADHXLHLLVLColumn Address Entry &amp; ReadREADHXLHLLVLColumn Address Entry &amp; ReadREADHXLHLHVLColumn Address Entry &amp; Read with Auto-PrechargeREADAHXLHLHXXSelf-Refresh Entry Self-Refresh EntryREFSHLLLHXXXSelf-Refresh Exit Burst TerminateTBSTHXLHHXXXHXLHXLHHLILILSelf-Refresh Exit&lt;</td><td><math display="block">\begin{array}{ c c c c c c c c c c c c c c c c c c c</math></td></t<>	COMMANDMNEMONICn-1nICSIRASICASIVEBA0,1IAPDeselectDESELHXHXXXXXXNo OperationNOPHXLHHHXXXRow Address Entry & Bank ActivateACTHXLLHHXXSingle Bank PrechargePREHXLLHHXLPrecharge All BanksPREAHXLLHLXHColumn Address Entry & WriteWRITEHXLHLLVLColumn Address Entry & Write with Auto-PrechargeREADHXLHLLVLColumn Address Entry & ReadREADHXLHLLVLColumn Address Entry & ReadREADHXLHLHVLColumn Address Entry & Read with Auto-PrechargeREADAHXLHLHXXSelf-Refresh Entry Self-Refresh EntryREFSHLLLHXXXSelf-Refresh Exit Burst TerminateTBSTHXLHHXXXHXLHXLHHLILILSelf-Refresh Exit<	$\begin{array}{ c c c c c c c c c c c c c c c c c c c$

SDR SDRAM E0342M21 (Ver.2.1) February 2004 (K) Japan

L

## M2V64S50ETP

64M Single Data Rate Synchronous DRAM

#### **FUNCTION TRUTH TABLE (1/4)** /WE Current State /CS /RAS /CAS Address Command Action IDLE Н NOP Х Х Х Х DESEL Х NOP NOP L Н Н Н н н L Х TBST ILLEGAL\*2 L **READ / WRITE** ILLEGAL\*2 L Н L Х BA, CA, A10 L L Н Н BA. RA ACT Bank Active, Latch RA BA, A10 L PRE / PREA NOP\*4 L Н L L L REFA Auto-Refresh\*5 L Н Х Op-Code, MRS L Mode Register Set\*5 L L L Mode-Add ROW ACTIVE X Х DESEL Н Х Х NOP Н Х L Н Н NOP NOP Η L Н L Х TBST NOP Begin Read, Latch CA, L Н L Н BA, CA, A10 READ / READA Determine Auto-Precharge WRITE / Begin Write, Latch CA, BA, CA, A10 L Н L L Determine Auto-Precharge WRITEA Н H BA, RA L L ACT Bank Active / ILLEGAL\*2 L L Н L BA, A10 PRE / PREA Precharge / Precharge All L L L Н Х REFA ILLEGAL Op-Code, L L L L MRS ILLEGAL Mode-Add DESEL NOP (Continue Burst to END) READ Н Х Х Х Х Н Н Н Х NOP NOP (Continue Burst to END) L L Н Н L Х TBST **Terminate Burst** Terminate Burst, Latch CA, READ / READA L Н L Н BA, CA, A10 Begin New Read, Determine Auto-Precharge\*3 Terminate Burst, Latch CA, WRITE / L BA, CA, A10 L Н L Begin Write, Determine Auto-**WRITEA** Precharge\*3 Bank Active / ILLEGAL\*2 L L Н Н BA, RA ACT Н BA, A10 PRE / PREA L L L Terminate Burst, Precharge L Н L L Х REFA ILLEGAL Op-Code, L L L MRS ILLEGAL



Mode-Add

SDR SDRAM E0342M21 (Ver.2.1) February 2004 (K) Japan

## M2V64S50ETP

64M Single Data Rate Synchronous DRAM

## **FUNCTION TRUTH TABLE (2/4)**

		<u> </u>			T/		
Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
WRITE	Н	Х	Х	Х	Х	DESEL	NOP (Continue Burst to END)
	L	Н	Н	Н	Х	NOP	NOP (Continue Burst to END)
	L	Н	Н	L	Х	TBST	Terminate Burst
	L	Н	L	Н	BA, CA, A10	READ / READA	Terminate Burst, Latch CA, Begin Read, Determine Auto- Precharge*3
	L	I	L	L	BA, CA, A10	WRITE / WRITEA	Terminate Burst, Latch CA, Begin Write, Determine Auto- Precharge*3
	L	L	H	Н	BA, RA	ACT	Bank Active / ILLEGAL*2
	F	L	Н	L	BA, A10	PRE / PREA	Terminate Burst, Precharge
	L	L	L	Н	Х	REFA	ILLEGAL
	L	-	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ with	Н	х	x	Х	x	DESEL	NOP (Continue Burst to END)
AUTO	L	Н	Н	Н	x	NOP	NOP (Continue Burst to END)
PRECHARGE	L	Н	н	Ļ	Х	TBST	ILLEGAL
	L	Н	L	Н	BA, CA, A10	READ / READA	ILLEGAL for same Bank *6
	L	Н	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL for same Bank *6
	L	L	Н	Н	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	Н	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	Н	Х	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE with	Н	Х	Х	Х	Х	DESEL	NOP (Continue Burst to END)
AUTO	L	Н	Н	Н	Х	NOP	NOP (Continue Burst to END)
PRECHARGE	L	Н	Н	L	Х	TBST	ILLEGAL
	L	Н	L	Н	BA, CA, A10	READ / READA	ILLEGAL for same Bank *7
	L	н	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL for same Bank *7
	L	L	Н	Н	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	Н	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	н	Х	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL



SDR SDRAM E0342M21 (Ver.2.1) February 2004 (K) Japan

## M2V64S50ETP

64M Single Data Rate Synchronous DRAM

## **FUNCTION TRUTH TABLE (3/4)**

/RAS X H H L L L L X H H H	/CAS X H H L H L X H H	/WE       X       H       L       H       L       H       L       H       H	Address X X X BA, CA, A10 BA, RA BA, A10 X Op-Code, Mode-Add X	Command DESEL NOP TBST READ / WRITE ACT PRE / PREA REFA MRS DESEL	Action NOP (Idle after tRP) NOP (Idle after tRP) ILLEGAL*2 ILLEGAL*2 NOP*4 (Idle after tRP) ILLEGAL ILLEGAL
H H L L L X H H H	H H L H L X H	H L X H L L X	X X BA, CA, A10 BA, RA BA, A10 X Op-Code, Mode-Add X	NOP TBST READ / WRITE ACT PRE / PREA REFA MRS	NOP (Idle after tRP) ILLEGAL*2 ILLEGAL*2 ILLEGAL*2 NOP*4 (Idle after tRP) ILLEGAL ILLEGAL
H H L L L X H H H	H L H L X H	L X H L L X	X BA, CA, A10 BA, RA BA, A10 X Op-Code, Mode-Add X	TBST READ / WRITE ACT PRE / PREA REFA MRS	ILLEGAL*2 ILLEGAL*2 ILLEGAL*2 NOP*4 (Idle after tRP) ILLEGAL ILLEGAL
H L L L X H H H	L H L L X H	X H L L X	BA, CA, A10 BA, RA BA, A10 X Op-Code, Mode-Add X	READ / WRITE ACT PRE / PREA REFA MRS	ILLEGAL*2 ILLEGAL*2 NOP*4 (Idle after tRP) ILLEGAL ILLEGAL
L L L X H H H	H H L X H	H L H L X	BA, RA BA, A10 X Op-Code, Mode-Add X	ACT PRE / PREA REFA MRS	ILLEGAL*2 NOP*4 (Idle after tRP) ILLEGAL ILLEGAL
L L X H H H	H L X H	L H L X	BA, A10 X Op-Code, Mode-Add X	PRE / PREA REFA MRS	NOP*4 (Idle after tRP) ILLEGAL ILLEGAL
L L X H H H	L L X H	H L X	X Op-Code, Mode-Add X	REFA MRS	ILLEGAL
L X H H	L X H	L X	Op-Code, Mode-Add X	MRS	ILLEGAL
X H H H	X H	Х	Mode-Add X		
нн	Н			DESEL	NOR (Row Active after tRCD
H H		Н		02022	NOP (ROW ACTIVE after IRCD
Н	н		Х	NOP	NOP (Row Active after tRCD
		L	Х	TBST	ILLEGAL*2
	L	х	BA, CA, A10	READ / WRITE	ILLEGAL*2
L	Н	н	BA, RA	ACT	ILLEGAL*2
L	Н	L	BA, A10	PRE / PREA	ILLEGAL*2
L	L	н	х	REFA	ILLEGAL
L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Х	Х	Х	Х	DESEL	NOP
Н	Н	Н	Х	NOP	NOP
Н	Н	L	Х	TBST	ILLEGAL*2
Н	L	х	BA, CA, A10	READ / WRITE	ILLEGAL*2
L	Н	Н	BA, RA	ACT	ILLEGAL*2
L	Н	L	BA, A10	PRE / PREA	ILLEGAL*2
L	L	Н	Х	REFA	ILLEGAL
L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
	H H L L	H H H L L H L H L L	H     H       H     L       X       L     H       H     L       L     H       L     H       L     H	HHLXHLXBA, CA, A10LHHBA, RALHLBA, A10LLHX	HHLXTBSTHLXBA, CA, A10READ / WRITELHHBA, RAACTLHLBA, A10PRE / PREALLHXREFA

SDR SDRAM E0342M21 (Ver.2.1) February 2004 (K) Japan

## **M2V64S50ETP**

64M Single Data Rate Synchronous DRAM

FUNCTIO	<u>N TR</u>	<u>UTH </u>	TABL	E (4/	4)		
Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
RE-	н	Х	Х	Х	Х	DESEL	NOP (Idle after tRFC)
FRESHING	L	Н	Н	Н	Х	NOP	NOP (Idle after tRFC)
	L	Н	Н	L	Х	TBST	ILLEGAL
	L	Н	L	Х	BA, CA, A10	READ / WRITE	ILLEGAL
	L	L	Н	Н	BA, RA	ACT	ILLEGAL
	L	L	Н	L	BA, A10	PRE / PREA	ILLEGAL
	L	L	L	Н	Х	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
MODE	Н	X	X	х	Х	DESEL	NOP (Idle after tRSC)
REGISTER	L	Н	Н	Н	Х	NOP	NOP (Idle after tRSC)
SETTING	L	н	Н	L	Х	TBST	ILLEGAL
	L	н	L	Х	BA, CA, A10	READ / WRITE	ILLEGAL
	L	L	Н	Н	BA, RA	ACT	ILLEGAL
	L	L	Н	L	BA, A10	PRE / PREA	ILLEGAL
	L	L	L	H	x	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

**ABBREVIATIONS:** 

H=High Level, L=Low Level, X=Don't Care

BA=Bank Address, RA=Row Address, CA=Column Address, NOP=No Operation

NOTES:

- 1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
- 2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
- 3. Must satisfy bus contention, bus turn around, write recovery requirements.
- 4. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
- 5. ILLEGAL if any bank is not idle.
- 6. Refer to Read with Auto-Precharge in page 16
- 7. Refer to Write with Auto-Precharge in page 17

ILLEGAL = Device operation and/or data-integrity are not guaranteed.

2

SDR SDRAM E0342M21 (Ver.2.1) February 2004 (K) Japan

\_ \_ \_ \_ \_ \_ \_ \_ \_

\_....

## M2V64S50ETP

64M Single Data Rate Synchronous DRAM

FUNCTION	I TRI	JTH .	TABL	_E fo	r CKI	Ε		
Current State	CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	Add	Action
SELF-	н	х	Х	Х	Х	Х	Х	INVALID
REFRESH*1	L	Н	Н	Х	Х	Х	Х	Exit Self-Refresh (Idle after tRFC)
	L	Н	L	Н	Н	Н	Х	Exit Self-Refresh (Idle after tRFC)
	L	Н	L	Н	Н	L	Х	ILLEGAL
	L	Н	L	Н	L	Х	Х	ILLEGAL
	L	Н	L	L	Х	Х	Х	ILLEGAL
	L	L	Х	Х	Х	Х	Х	NOP (Maintain Self-Refresh)
POWER	Н	Х	Х	Х	Х	Х	Х	INVALID
DOWN	L	Н	X	X	Х	Х	Х	Exit Power Down to Idle
	L	L	Х	Х	Х	Х	Х	NOP (Maintain Power Down)
ALL BANKS	н	Н	X	Х	Х	Х	Х	Refer to Function Truth Table
IDLE*2	Н	L	L	L	L	Н	Х	Enter Self-Refresh
	Н	L	Н	Х	Х	Х	Х	Enter Power Down
	Н	L	L	Н	H	Н	Х	Enter Power Down
	Н	L	L	Н	н	L	Х	ILLEGAL
	Н	L	L	Н	L	X	Х	ILLEGAL
	Н	L	L	L	X	X	X	ILLEGAL
	L	Х	Х	Х	X	Х	Х	Refer to Current State =Power Down
ANY STATE	Н	Н	Х	Х	Х	Х	X	Refer to Function Truth Table
other than	Н	L	Х	Х	Х	Х	X	Begin CLK Suspend at Next Cycle*3
listed above	L	Н	Х	Х	Х	Х	X	Exit CLK Suspend at Next Cycle*3
	L	L	Х	Х	Х	х	Х	Maintain CLK Suspend

#### ABBREVIATIONS:

H=High Level, L=Low Level, X=Don't Care

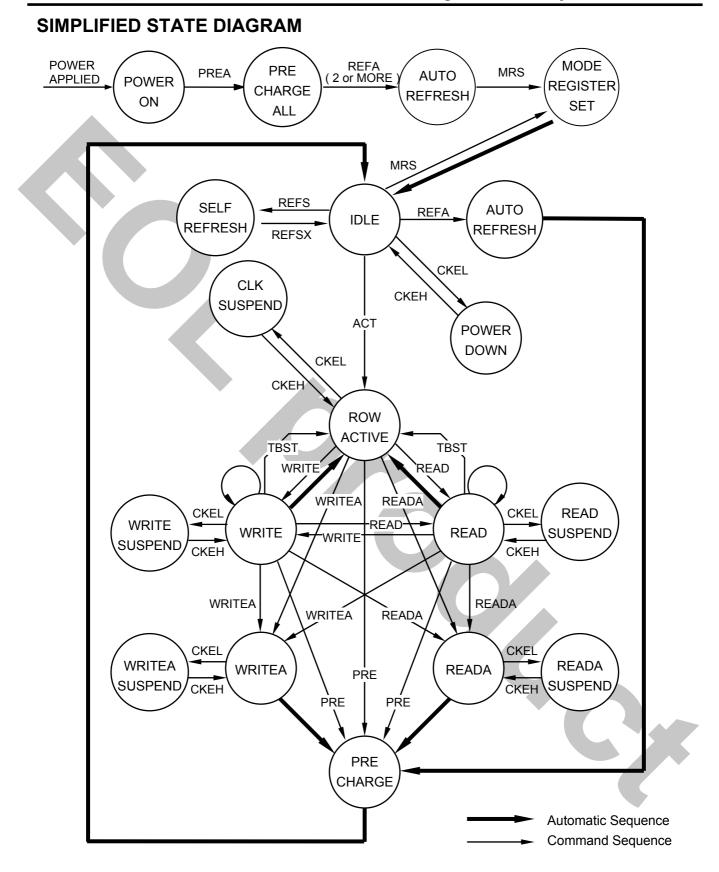
NOTES:

- 1. CKE Low to High transition will re-enable CLK and other inputs **asynchronously** A minimum setup time must be satisfied before any command other than EXIT.
- 2. Self-Refresh can be entered only from the All Banks Idle State.
- 3. Must be legal command.

SDR SDRAM E0342M21 (Ver.2.1) February 2004 (K) Japan

## M2V64S50ETP

64M Single Data Rate Synchronous DRAM



## POWER ON SEQUENCE

Before starting normal operation, the following power on sequence is necessary to prevent a SDRAM from damaged or malfunctioning.

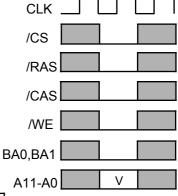
- 1. Apply power and start clock. Attempt to maintain CKE high, DQM high and NOP or DESEL condition at the inputs.
- 2. Maintain stable power, stable clock, and NOP or DESEL input conditions for a minimum of 100us.
- 3. Issue precharge commands for all banks. (PRE or PREA)
- 4. After all banks become idle state (after tRP), issue 2 or more auto-refresh commands.
- 5. Issue a mode register set command to initialize the mode register.

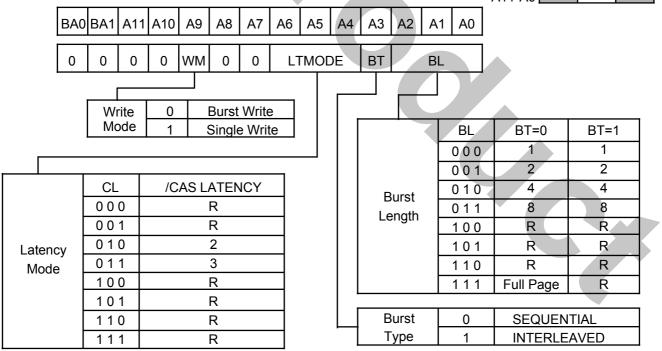
After these sequence, the SDRAM is idle state and ready for normal operation.

#### MODE REGISTER

Burst Length, Burst Type, /CAS Latency and Write Mode can be programmed By setting the mode register (MRS) with BA0=BA1=0. The mode register stores these data until the next MRS command, which may be issued when all banks are in idle state. After tRSC from a MRS command, the SDRAM is ready for new command.

Unused bit A7-A8,A10(x32) have to be programmed to "0".

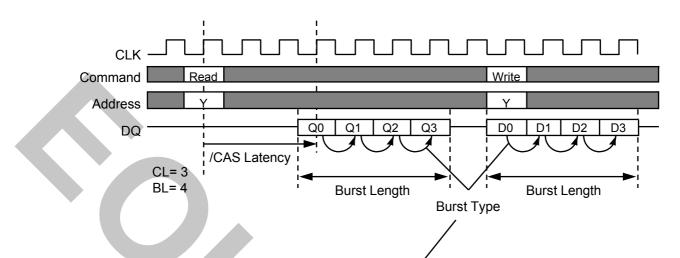




R: Reserved for Future Use

SDR SDRAM E0342M21 (Ver.2.1) February 2004 (K) Japan

## **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM



Initia	al Ado	lress	BL							Colu	mn A		ssing							
A2	A1	A0					Sequ	uentia	al	_			-		Interl	eave	b			
0	0	0		0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
0	0	1		1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6	
0	1	0		2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5	
0	1	1		3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4	
1	0	0	8	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	
1	0	1		5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2	
1	1	0		6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1	
1	1	1		7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0	
-	0	0		0	1	2	3					0	1	2	3					
-	0	1		1	2	3	0					1	0	3	2					
-	1	0	4	2	3	0	1					2	3	0	1					
-	1	1		3	0	1	2					3	2	1	0					
-	-	0		0	1							0	1							
-	-	1	2	1	0							1	0							

## **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM

## **OPERATIONAL DESCRIPTION**

#### BANK ACTIVATE

One of four banks is activated by an ACT command. A bank is selected by BA0-1. A row is selected by A0-10(x32). Multiple banks can be active state concurrently by issuing multiple ACT commands. Minimum activation interval between one bank and another bank is tRRD.

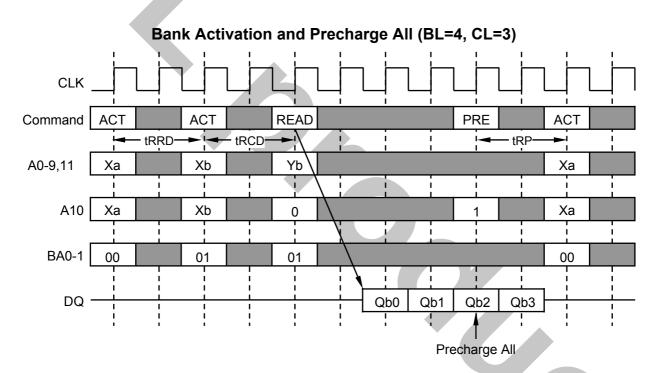
#### PRECHARGE

An open bank is deactivated by a PRE command.

A bank to be deactivated is designated by BA0-1.

When multiple banks are active, a precharge all command (PREA, PRE + A10=H) deactivates all of open banks at the same time. BA0-1 are "Don't Care" in this case.

Minimum delay time of an ACT command after a PRE command to the same bank is tRP.



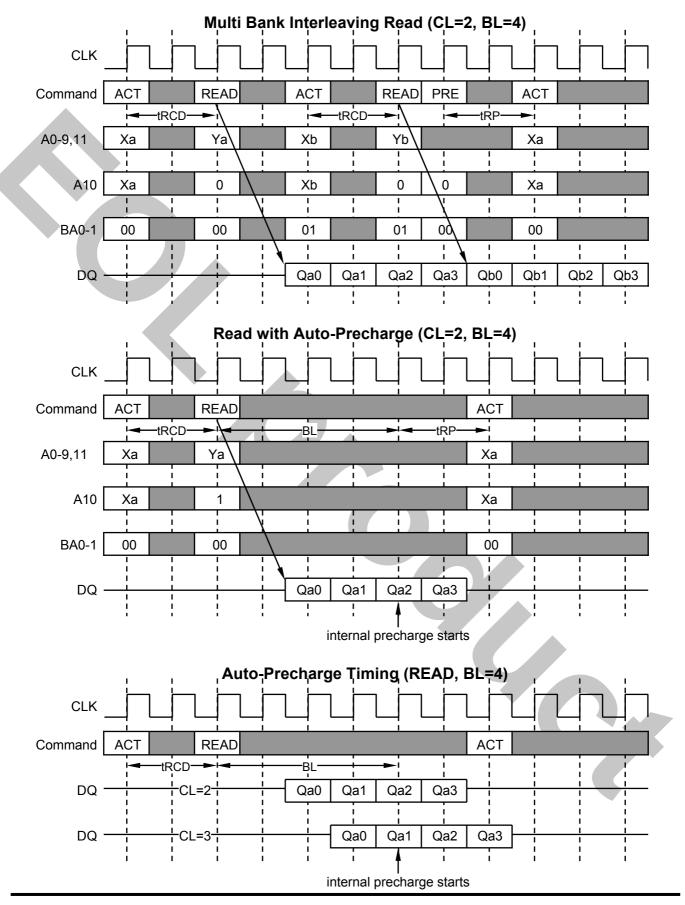
#### READ

A READ command can be issued to any active bank. The start address is specified by A0-7. 1st output data is available after the /CAS Latency from the READ. The consecutive data length is defined by the Burst Length. The address sequence of the burst data is defined by the Burst Type. Minimum delay time of a READ command after an ACT command to the same bank is tRCD. When A10 is high at a READ command, auto-precharge (READA) is performed. Any command (READ, WRITE, PRE, ACT,TBST) to the same bank is inhibited till the internal precharge is complete. The internal precharge starts at the BL after READA. The next ACT command can be issued after (BL + tRP) from the previous READA. In any case, tRCD+BL > tRASmin must be met.

SDR SDRAM E0342M21 (Ver.2.1) February 2004 (K) Japan

# M2V64S50ETP

64M Single Data Rate Synchronous DRAM



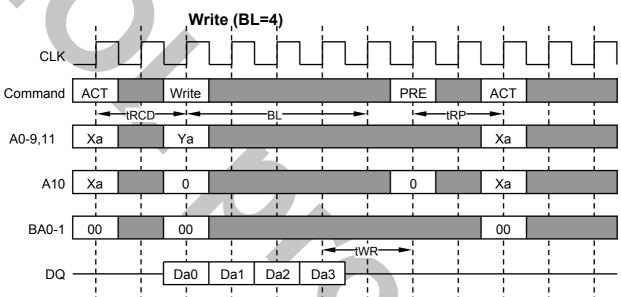
**ΕLΡΙDΛ** 

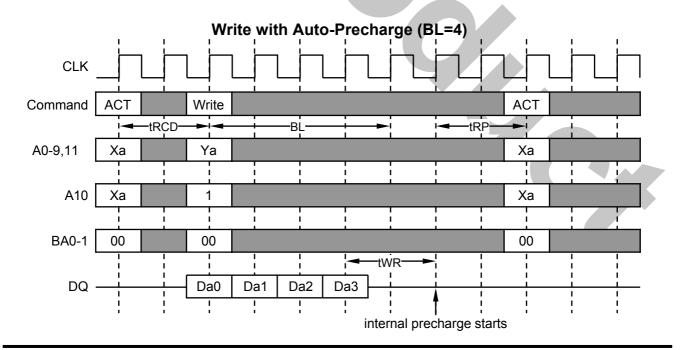
SDR SDRAM E0342M21 (Ver.2.1) February 2004 (K) Japan

## **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM

#### WRITE

A WRITE command can be issued to any active bank. The start address is specified by A0-7. 1st input data is set at the same cycle as the WRITE. The consecutive data length to be written is defined by the Burst Length. The address sequence of burst data is defined by the Burst Type. Minimum delay time of a WRITE command after an ACT command to the same bank is tRCD. From the last input data to the PRE command, the write recovery time (tWR) is required. When A10 is high at a WRITE command, auto-precharge (WRITEA) is performed. Any command (READ, WRITE, PRE, ACT, TBST) to the same bank is inhibited till the internal precharge is complete. The internal precharge starts at tWR after the last input data cycle. The next ACT command can be issued after (BL + tWR -1 +tRP) from the previous WRITEA. In any case, tRCD + BL + tWR -1 > tRASmin must be met.



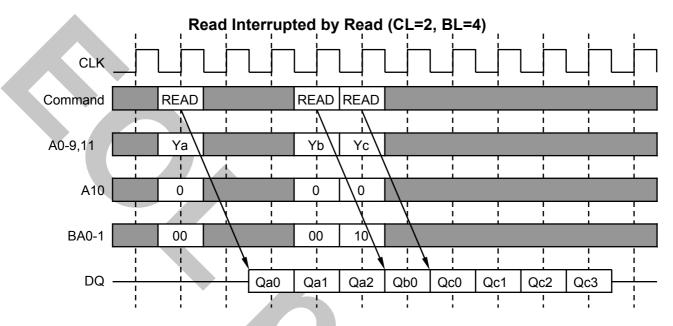


## M2V64S50ETP 64M Single Data Rate Synchronous DRAM

## BURST INTERRUPTION

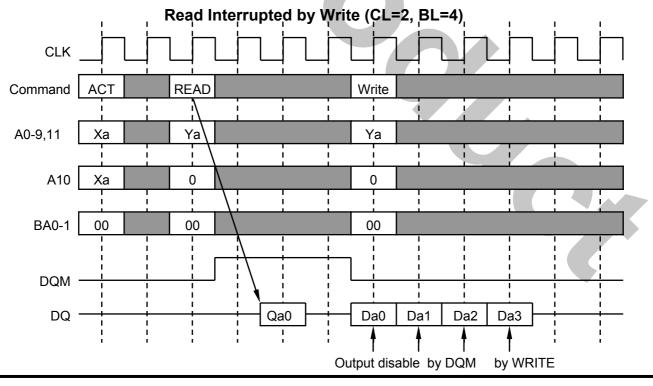
#### Read Interrupted by Read

Burst read operation can be interrupted by new read of any active bank. Random column access is allowed. READ to READ interval is minimum 1 CLK.



#### **Read Interrupted by Write**

Burst read operation can be interrupted by write of any active bank. Random column access is allowed. In this case, the DQ should be controlled adequately by using the DQM to prevent the bus contention. The output is disabled automatically 2 cycle after WRITE assertion.

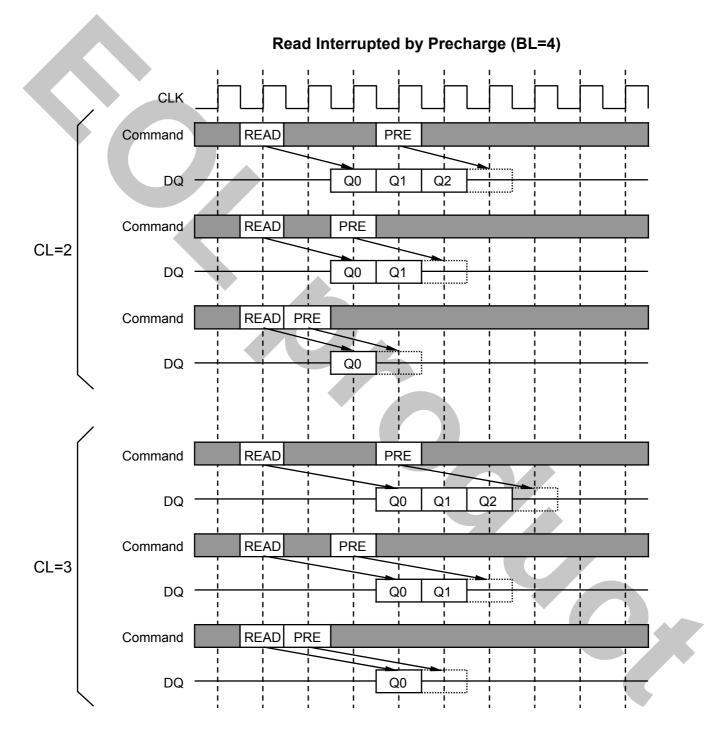


**ΕLΡΙDΛ** 

#### **Read Interrupted by Precharge**

A burst read operation can be interrupted by a precharge of **the same bank**. READ to PRE interval is minimum 1 CLK.

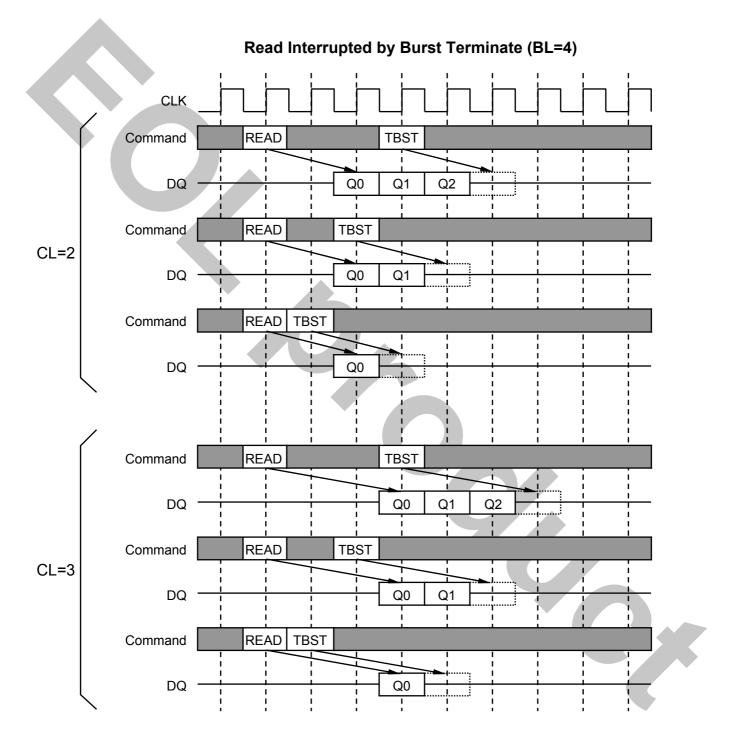
A PRE command to output disable latency is equivalent to the /CAS Latency.



## **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM

#### Read Interrupted by Burst Terminate

Similarly to the precharge, a burst terminate command can interrupt the burst read operation and disable the data output. The terminated bank remains active. READ to TBST interval is minimum 1 CLK. A TBST command to output disable latency is equivalent to the /CAS Latency.

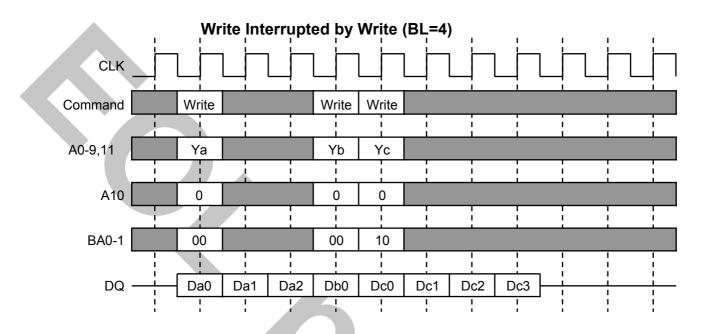


SDR SDRAM E0342M21 (Ver.2.1) February 2004 (K) Japan

## **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM

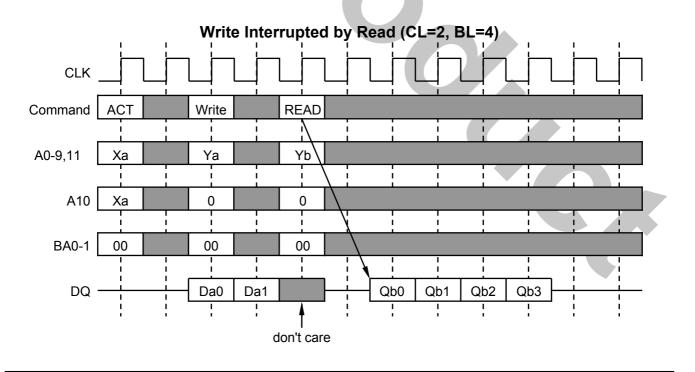
#### Write Interrupted by Write

Burst write operation can be interrupted by new write of any active bank. Random column access is allowed. WRITE to WRITE interval is minimum 1 CLK.



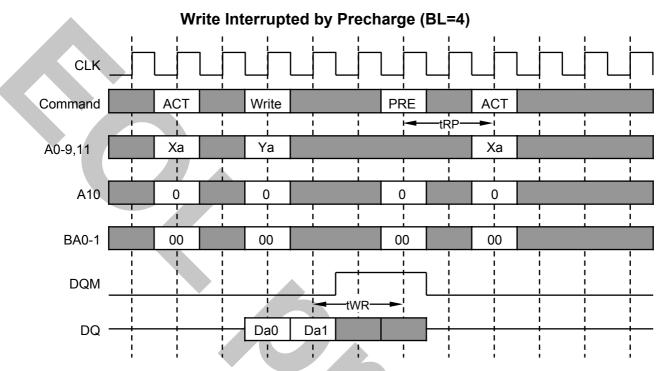
#### Write Interrupted by Read

Burst write operation can be interrupted by read of any active bank. Random column access is allowed. WRITE to READ interval is minimum 1 CLK. The input data on DQ at the interrupting READ cycle is "Don't Care".



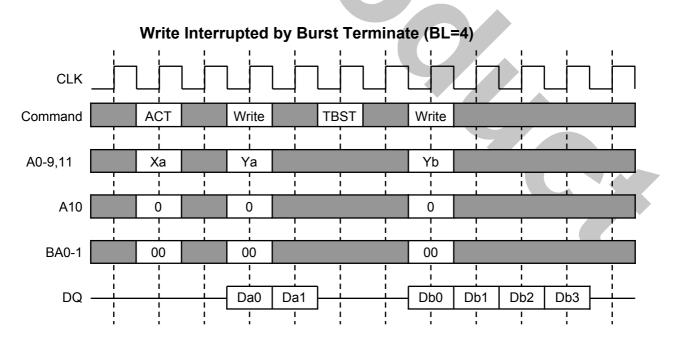
#### Write Interrupted by Precharge

Burst write operation can be interrupted by precharge of **the same bank**. Write recovery time (tWR) is required from the last data to PRE command. During write recovery, data inputs must be masked by DQM.



#### Write Interrupted by Burst Terminate

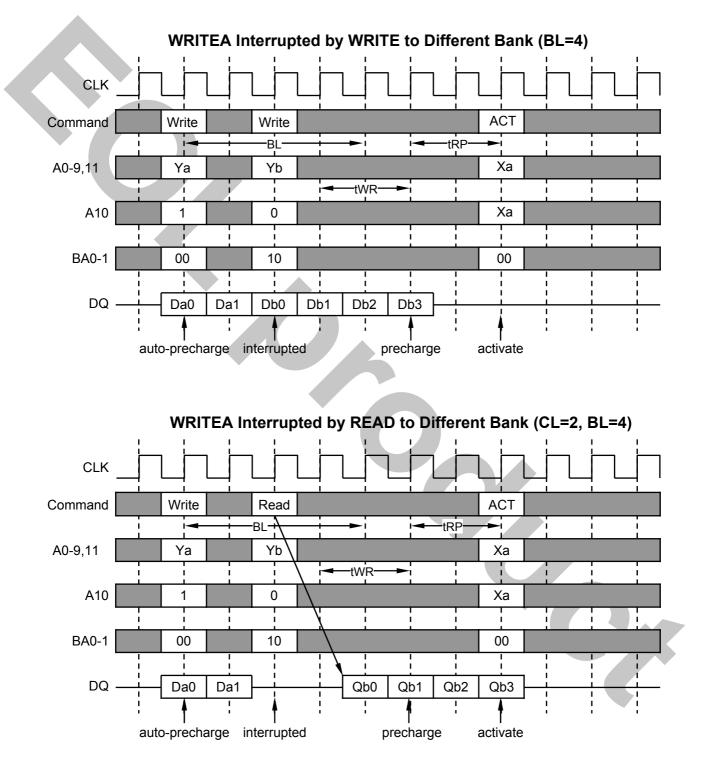
Burst terminate command can terminate burst write operation. In this case, the write recovery time is not required and the bank remains active. WRITE to TBST interval is minimum 1 CLK.



## **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM

#### Write with Auto-Precharge Interrupted by Write / Read to Different Bank

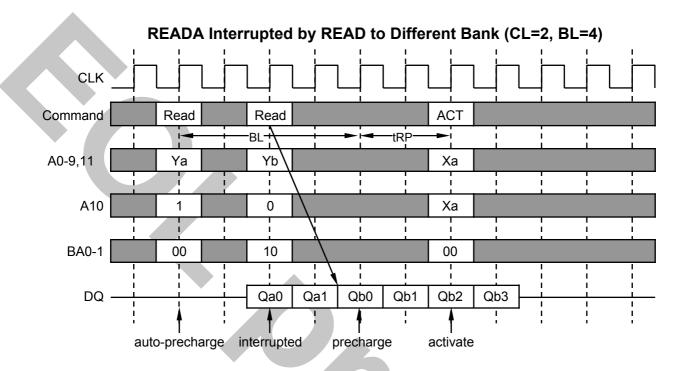
Burst write with auto-precharge can be interrupted by write or read to **different bank**. Next ACT command can be issued after (BL+tWR-1+tRP) from the WRITEA. Auto-precharge interruption by a command to the same bank is inhibited.



## **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM

#### Read with Auto-Precharge Interrupted by Read to Different Bank

Burst read with auto-precharge can be interrupted by read to **different bank**. Next ACT command can be issued after (BL+tRP) from the READA. Auto-precharge interruption by a command to the same bank is inhibited.



#### Full Page Burst

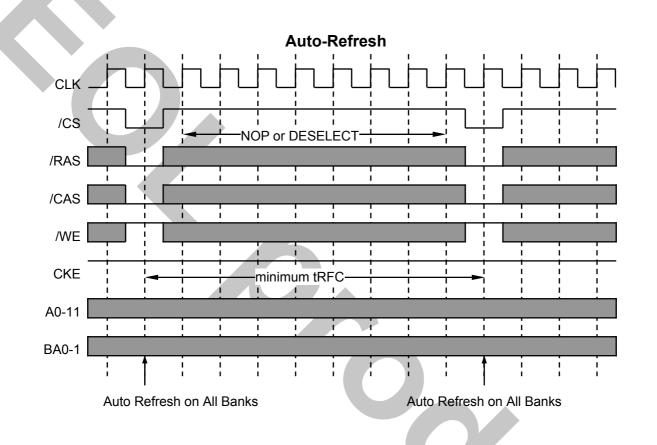
Full page burst length is available for only the sequential burst type. Full page burst read / write is repeated until a Precharge or a Burst Terminate command is issued. In case of the full page burst, a read / write with auto-precharge command is illegal.

SDR SDRAM E0342M21 (Ver.2.1) February 2004 (K) Japan

## **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM

#### AUTO REFRESH

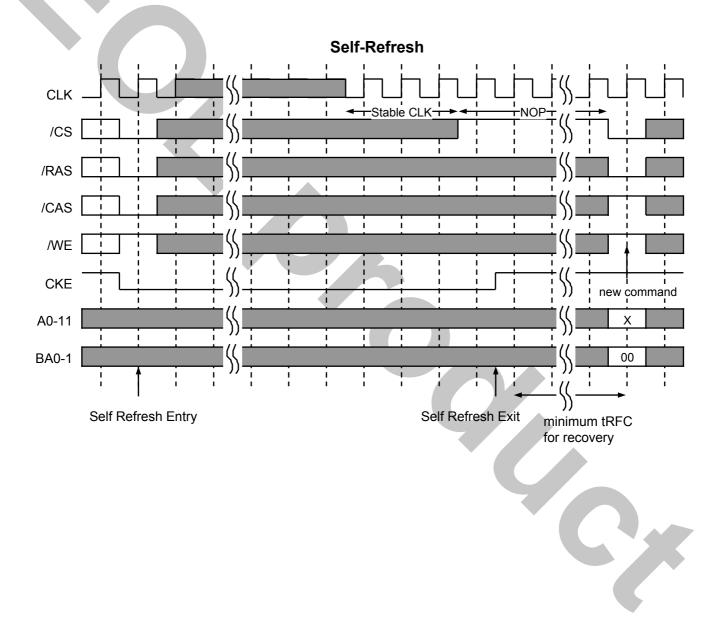
Single cycle of auto-refresh is initiated with a REFA (/CS= /RAS= /CAS= L, /WE= /CKE= H) command. The refresh address is generated internally. 4096 REFA cycles within 64ms refresh 64Mbit memory cells. The auto-refresh is performed on 4 banks concurrently. Before performing an auto-refresh, all banks must be in idle state. Auto-refresh to auto-refresh interval is minimum tRFC. Any command must not be issued before tRFC from the REFA command.



## M2V64S50ETP 64M Single Data Rate Synchronous DRAM

#### SELF REFRESH

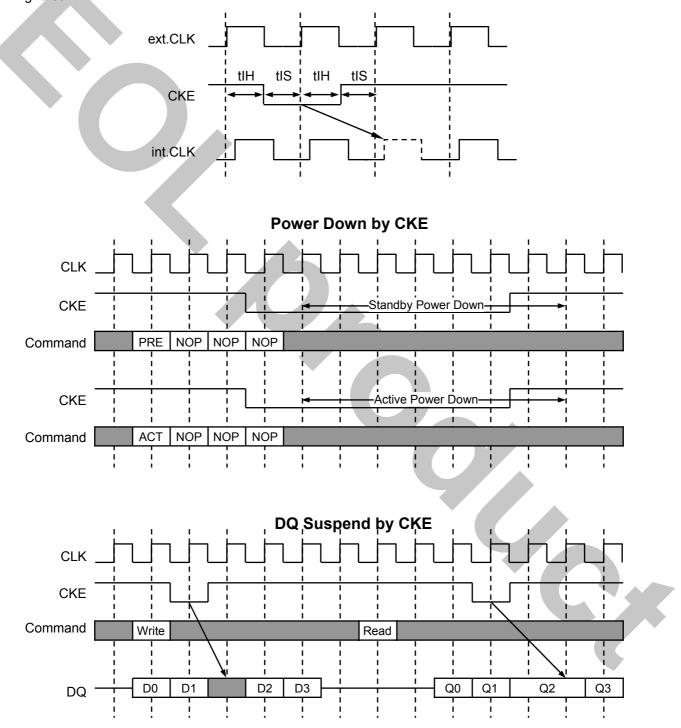
Self-refresh mode is entered by issuing a REFS command (/CS= /RAS= /CAS= L, /WE= H, CKE= L). Once the self-refresh is initiated, it is maintained as long as CKE is kept low. During the self-refresh mode, CKE is asynchronous and the only enabled input. All other inputs including CLK are disabled and ignored, so that power consumption due to synchronous inputs is saved. To exit the self-refresh, supplying stable CLK inputs, asserting DESEL or NOP command and then asserting CKE=H. After tRFC from the 1st CLK edge following CKE=H, all banks are in idle state and a new command can be issued, but DESEL or NOP commands must be asserted till then.



## M2V64S50ETP 64M Single Data Rate Synchronous DRAM

#### **CLK SUSPEND and POWER DOWN**

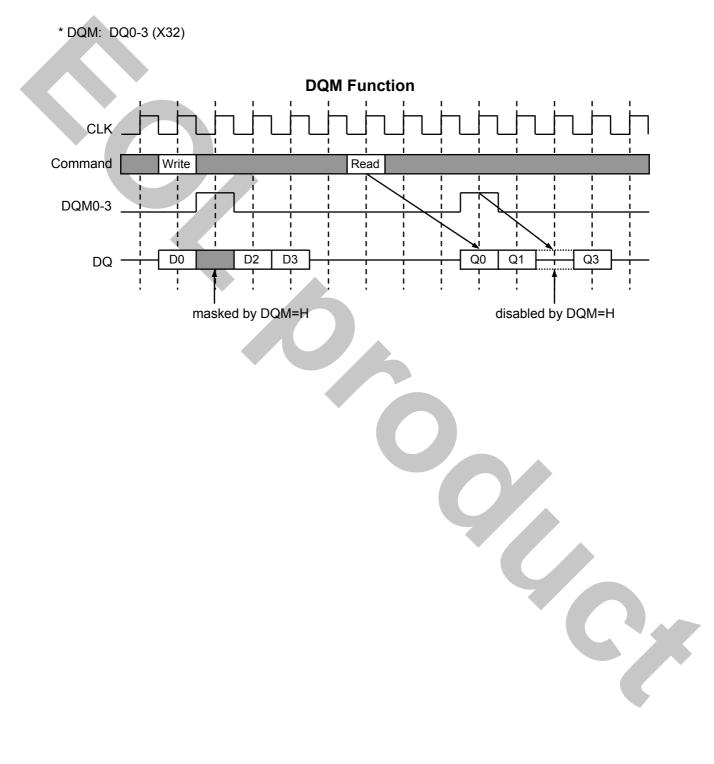
CKE controls the internal CLK at the following cycle. Figure below shows how CKE works. By negating CKE, the next internal CLK is suspended. The purpose of CLK suspend is power down, output suspend or input suspend. CKE is a synchronous input except during the self-refresh mode. CLK suspend can be performed either when the banks are active or idle. A command at the suspended cycle is ignored.



SDR SDRAM E0342M21 (Ver.2.1) February 2004 (K) Japan

#### **DQM CONTROL**

DQM\* is a dual functional signal defined as the data mask for writes and the output disable for reads. During writes, DQM masks input data word by word. DQM to Data In latency is 0. During reads, DQM forces output to Hi-Z word by word. DQM to output Hi-Z latency is 2.



## M2V64S50ETP

64M Single Data Rate Synchronous DRAM

## **ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
VDD	Supply Voltage	with respect to VSS	-0.5 to 4.6	V
VDDQ	Supply Voltage for Output	with respect to VSSQ	-0.5 to 4.6	V
VI	Input Voltage	with respect to VSS	-0.5 to VDD+0.5	V
vo	Output Voltage	with respect to VSSQ	-0.5 to VDD+0.5	V
Ю	Output Current		50	mA
Pd	Power Dissipation	TA=25 °C	1000	mW
Topr	Operating Temperature		0 to 70	°C
Tstg	Storage Temperature		-65 to 150	°C

## **RECOMMENDED OPERATING CONDITIONS**

(TA=0 to 70°C, unless otherwise noted)

Symbol	Parameter		Limits		Unit
Symbol	Palalletei	Min.	Тур.	Max.	Unit
VDD	Supply Voltage	3.0	3.3	3.6	V
VSS	Supply Voltage	0	0	0	V
VDDQ	Supply Voltage for Output	3.0	3.3	3.6	V
VSSQ	Supply Voltage for Output	0	0	0	V
VIH	High-Level Input Voltage all inputs	2.0		VDD+0.3	V
VIL	Low-Level Input Voltage all inputs	-0.3		0.8	V

### CAPACITANCE

(TA=0 to 70°C, VDD = VDDQ = 3.3V+0.3V, VSS = VSSQ = 0V, unless otherwise noted)

Symbol	Parameter	Test Condition	Lin	nits	Unit	T
Symbol	Faiamelei	Test Condition	Min.	Max.	Unin	
CI(A)	Input Capacitance,address pin		2.0	4.0	pF	k
CI(C)	Input Capacitance,control pin	VI=1.4V f=1MHz	2.0	4.0	pF	
CI(K)	Input Capacitance,CLK pin	VI=25mVrms	2.0	4.0	pF	
CI/O	Input Capacitance,I/O pin		3.0	6.0	pF	



## M2V64S50ETP

64M Single Data Rate Synchronous DRAM

## AVERAGE SUPPLY CURRENT from VDD

(TA=0 to 70°C, VDD = VDDQ = 3.3V+0.3V, VSS = VSSQ = 0V, Output Open, unless otherwise noted)

	Descrite	Test One little	Li	mits(ma	ax)	Unit	Note	
Symbol	Parameter	Test Conditions		-5	-6	-7	Unit	Note
lcc1	Operating Current (1bank)	tCLK=min, tRC=min, BL=1		110	100	90	mA	1
lcc2P	Idle Standby Current	tCLK=min, CKE <vilmax< td=""><td>2.0</td><td>mA</td><td>2</td></vilmax<>			2.0	mA	2	
Icc2PS	in Power Down Mode	tCLK=L, CKE <vilmax< td=""><td>1.0</td><td>mA</td><td>2</td></vilmax<>			1.0	mA	2	
Icc2N	Idle Standby Current	tCLK=min, CKE>VIHmin, /CS>VIHmin			10			2,3
Icc2NS	in Normal Mode	tCLK=L, CKE>VIHmin		5		mA	2,4	
Icc3N	Active Standby Current	tCLK=min, CKE>VIHmin, /CS	tCLK=min, CKE>VIHmin, /CS> VIHmin				mA	3,5
Icc3NS	in Normal Mode	tCLK=L, CKE>VIHmin			10		mA	4,5
Icc4	Burst Operating Current	tCLK=min, BL=4, gapless dat	a	130	110	90	mA	5
Icc5	Auto-Refresh Current	tCLK=min, tRFC=min	140	120	100	mA		
loof	Solf Defreeb Current			1.0		mA		
lcc6	Self-Refresh Current	CKE<0.2v	-5L / -6L / -7L		0.5		mA	6

Notes 1. addresses are changed 3 times during tRC, only 1 bank is active & all other banks are idle

2. all banks are idle

3. input signals are changed one time during 3 x tCLK

4. input signals are stable

5. all banks are active

6. Low Power Version(-5L/-6L/-7L)

## AC OPERATING CONDITIONS AND CHARACTERISTICS

(TA=0 to 70°C, VDD = VDDQ = 3.3V+0.3V, VSS = VSSQ = 0V, unless otherwise noted)

Symbol	Parameter	Test Conditions	Lin	Unit	
Symbol		Test Conditions	Min.	Max.	Unit
VOH(DC)	High-Level Output Voltage (DC)	IOH=-2mA	2.4		V
VOL(DC)	Low-Level Output Voltage (DC)	IOL= 2mA		0.4	V
IOZ	Off-state Output Current	Q floating Vo=0 to VDDQ	-10	10	uA
IL	Input Current	VIH=0 to VDDQ+0.3V, other input pins=0V	-10	10	uA

## M2V64S50ETP 64M Single Data Rate Synchronous DRAM

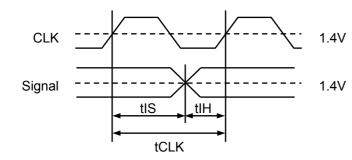
## AC TIMING REQUIREMENTS

(TA=0 to 70°C, VDD = VDDQ = 3.3V+0.3V, VSS = VSSQ = 0V, unless otherwise noted)

Input Pulse Levels : 0.8V to 2.0V

Input Timing Measurement Level : 1.4V

			Limits							
Symbol	Parameter	-5		-6		-7		Unit	Note	
			Min.	Max.	Min.	Max.	Min.	Max.		
tCLK	CLK cycle time	CL=2	7.5		10		10		ns	
ICEN	CER Cycle une	CL=3	7.5		7.5		10		ns	
tCH	CLK High pulse width		2.5		2.5		3		ns	
tCL	CLK Low pulse width		2.5		2.5		3		ns	
tT	Transition time of CLK		1	10	1	10	1	10	ns	
tIS			1.5		1.5		2		ns	
tIH			0.8		0.8		1		ns	
tRC	Row Cycle time	>	60		67.5		70		ns	
tRFC	CD Row to Column Delay AS Row Active time		66		75		80		ns	
tRCD			15		20		20		ns	
tRAS			45	120000	45	120000	50	120000	ns	
tRP			15		20		20		ns	
tWR	Write Recovery time		15		15		20		ns	
tRRD	ACT to ACT Delay time		15		15		20		ns	
tRSC	Mode Register Set Cycl	e time	10		10		10		ns	
tREF	Refresh Interval time			64		64		64	ms	



AC timing is referenced to the input signal crossing through 1.4V.

## M2V64S50ETP 64M Single Data Rate Synchronous DRAM

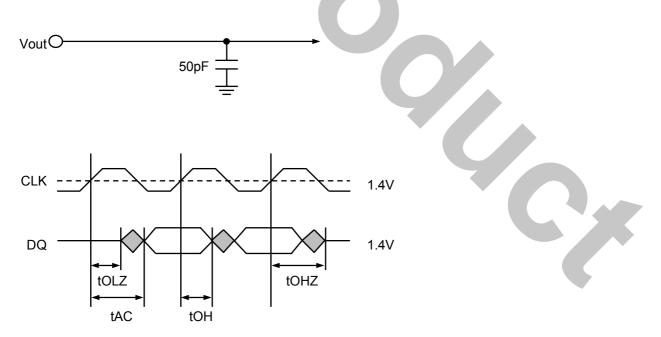
## SWITCHING CHARACTERISTICS

(	(TA=0 to 70°C, VDD = VDDQ = 3.3V+0.3V, VSS	S = VSSQ = 0V unless otherwise noted)

		Parameter		Limits						
	Symbol			-5		-6		-7		Unit
				Min.	Max	Min.	Max	Min.	Max	
	tAC Access Time from CLK	Access Time from CLK	CL=2		5.4		6		6	ns
		Access third from OEK	CL=3		5.4		5.4		6	ns
	tOH	Output Hold Time from CLK	CL=2	3		3		3		ns
			CL=3	3		3		3		ns
	tOLZ	Delay Time, Output Low impedance from CLK		0		0		0		ns
	tOHZ	Delay Time, Output High impedance from CLK	CL=2	3	5.4	3	6	3	6	ns
			CL=3	3	5.4	3	5.4	3	6	ns

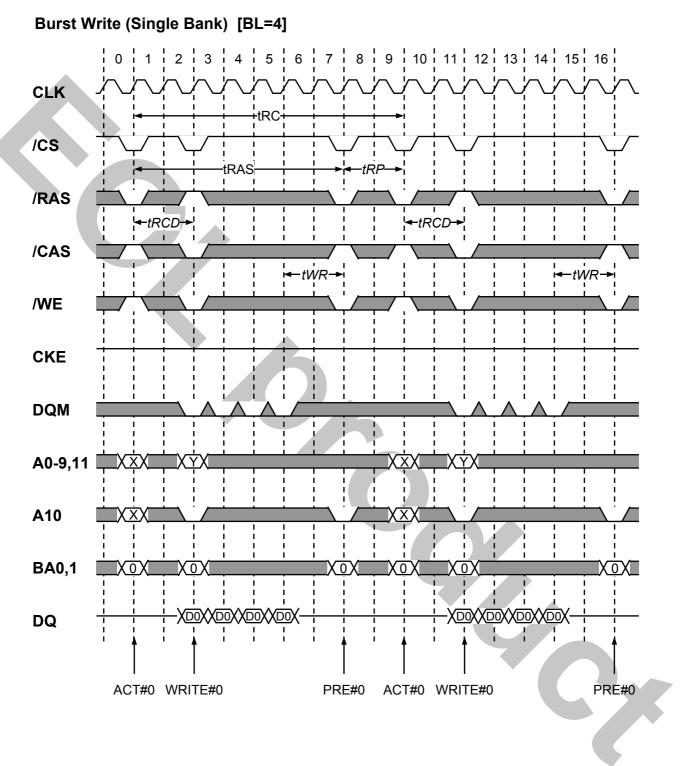
Note. If tr (CLK rising time) is > 1ns, (tr/2 - 0.5ns) should be added to the parameters.

#### **Output Load Condition**



## **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM

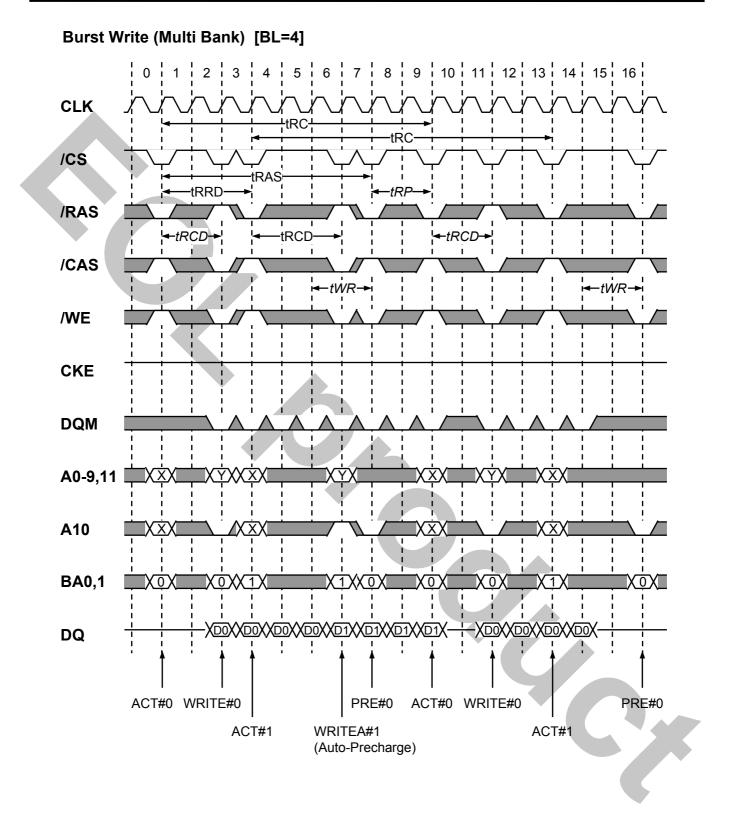
## **TIMING CHARTS**



Italic parameter shows minimum case

**ΕLΡΙDΛ** 

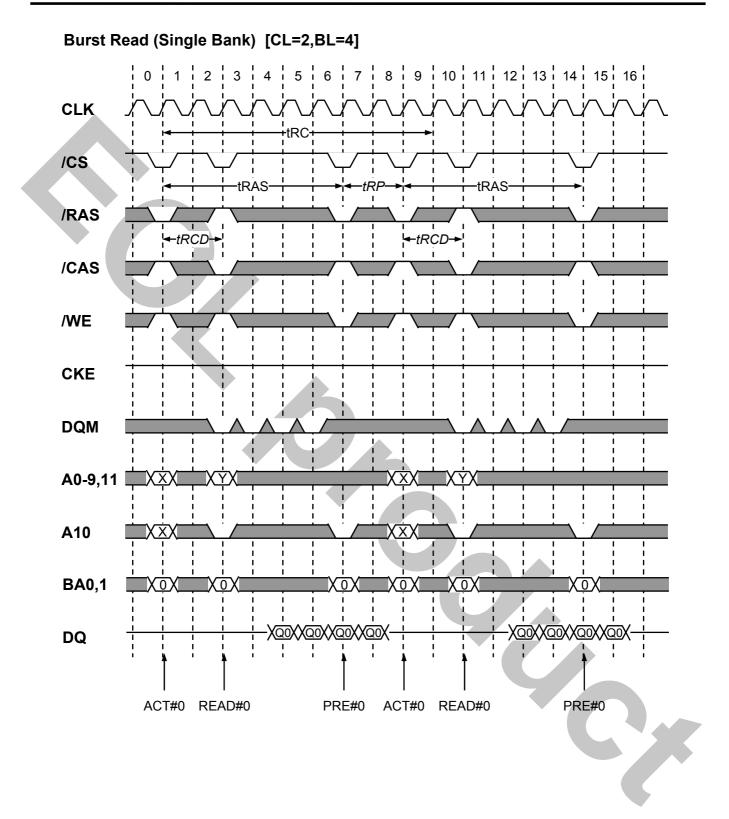
## **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM



Italic parameter shows minimum case

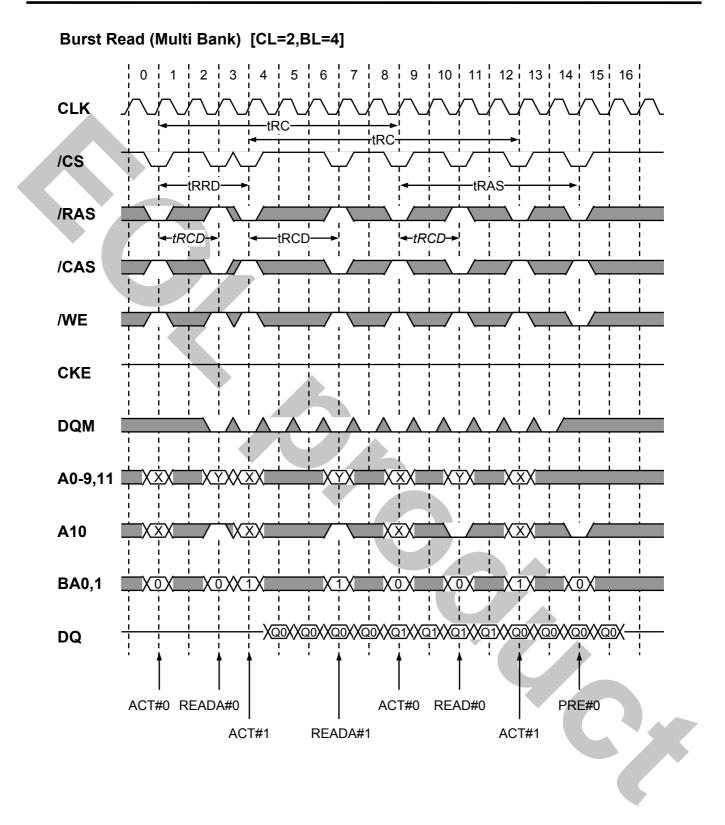
**ΕLΡΙDΛ** 

## **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM



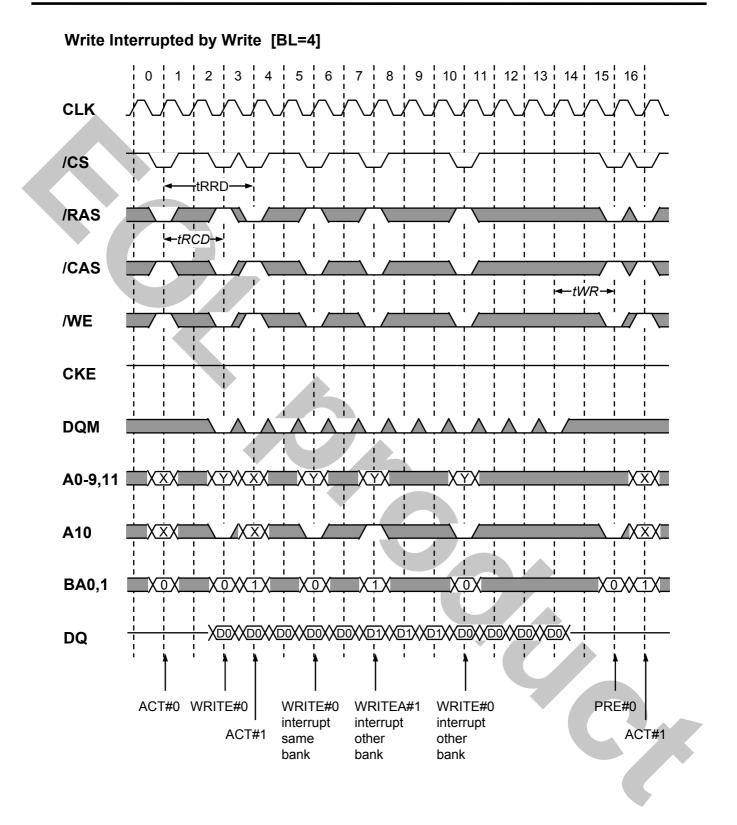
Italic parameter shows minimum case

## **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM

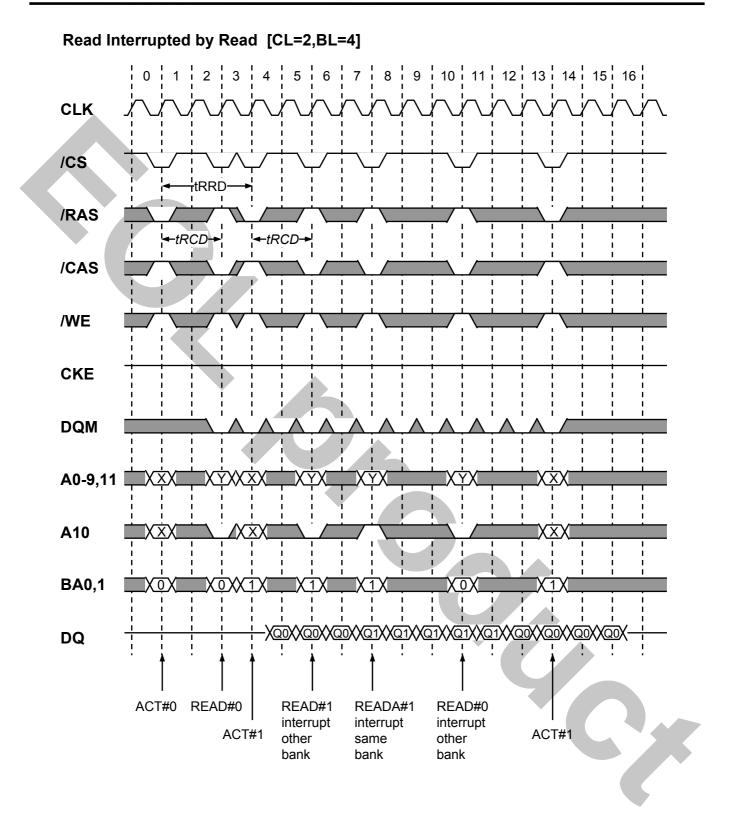


Italic parameter shows minimum case

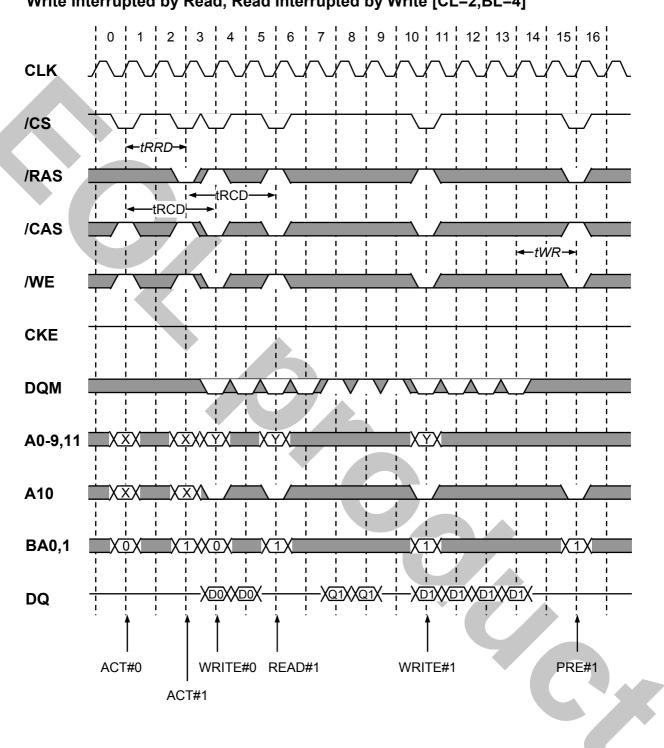
# **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM



# **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM

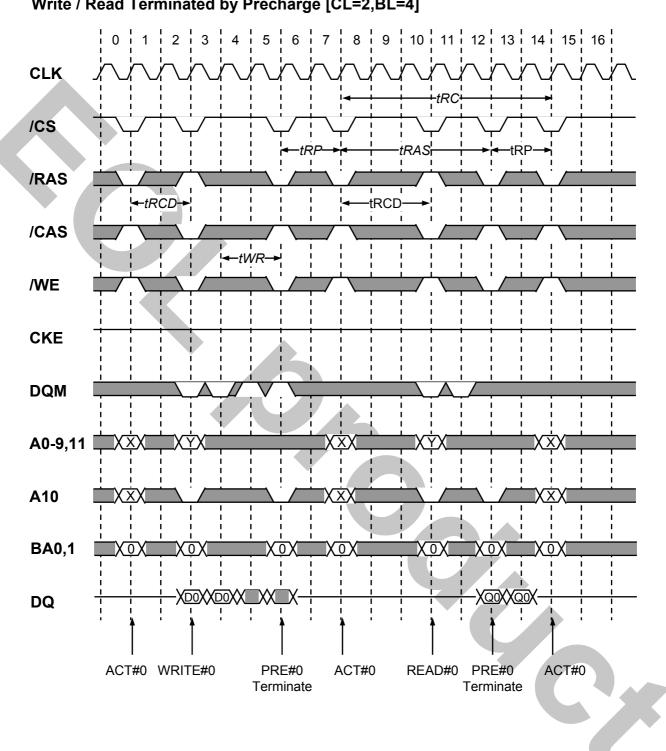


# **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM



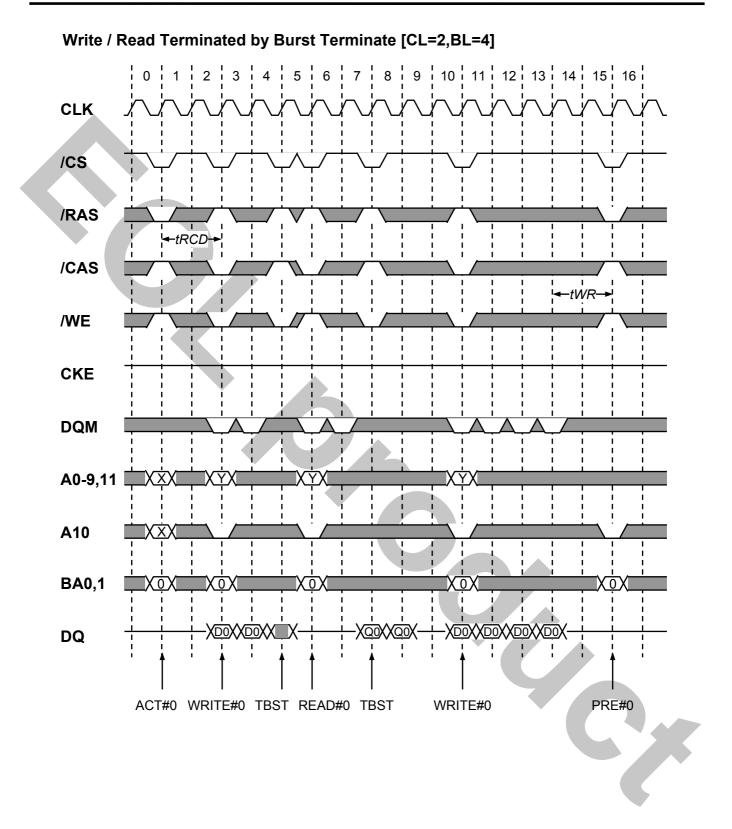
## Write Interrupted by Read, Read Interrupted by Write [CL=2,BL=4]

# **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM

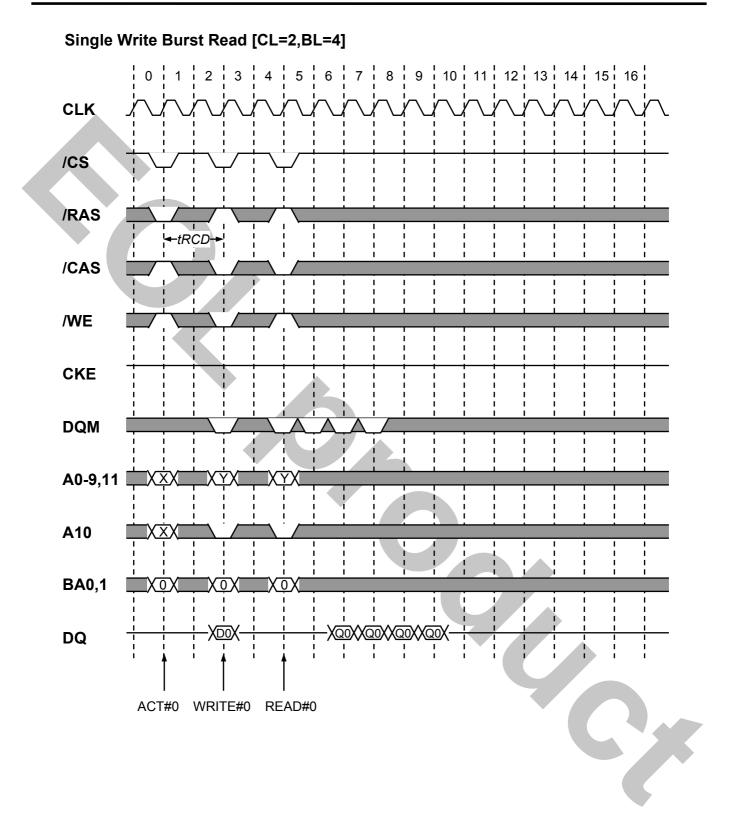


Write / Read Terminated by Precharge [CL=2,BL=4]

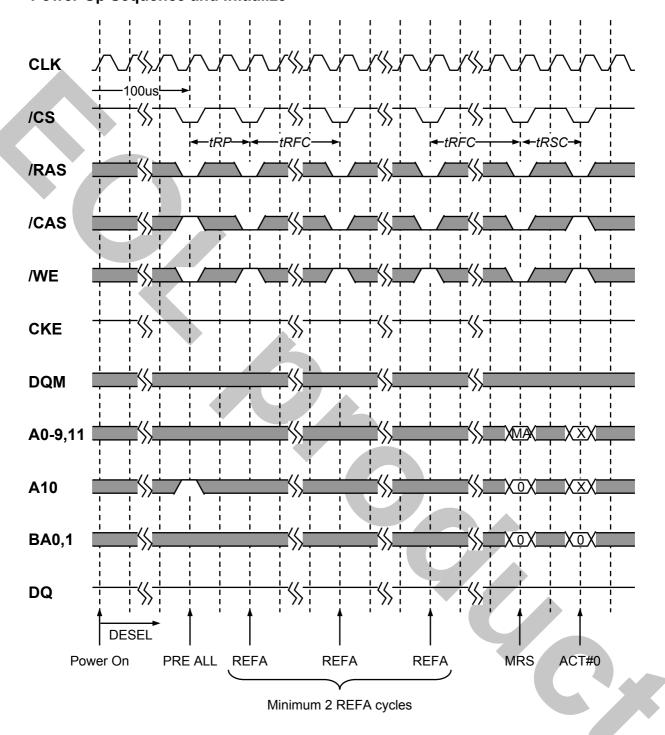
# **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM



## **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM



## **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM

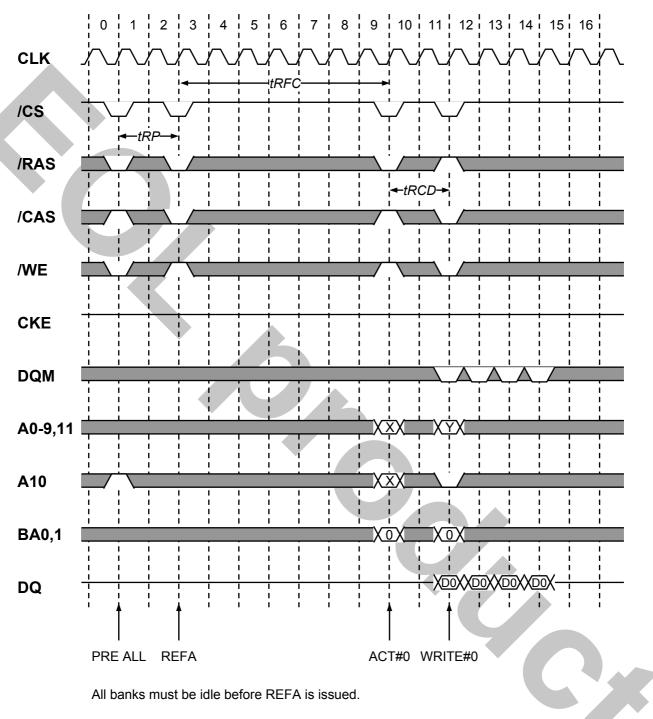


Power-Up Sequence and Initialize

SDR SDRAM E0342M21 (Ver.2.1) February 2004 (K) Japan

## **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM

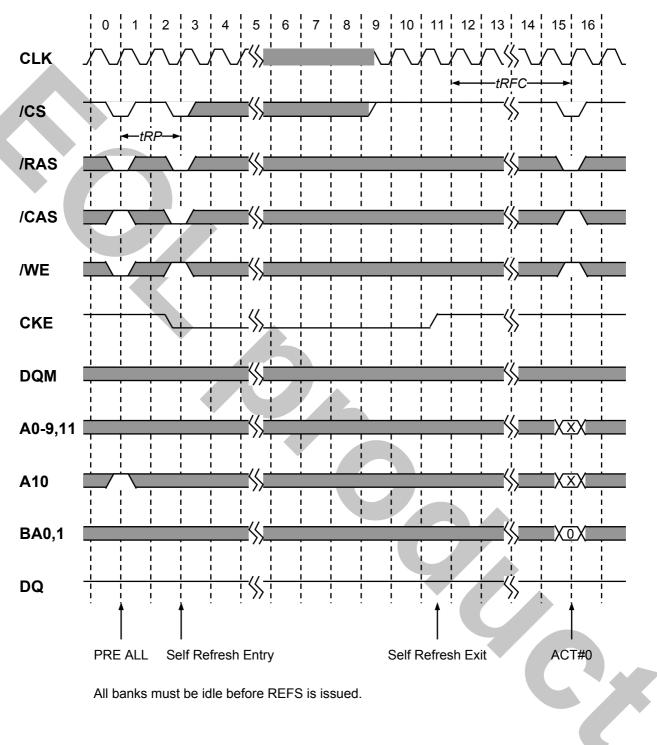




SDR SDRAM E0342M21 (Ver.2.1) February 2004 (K) Japan

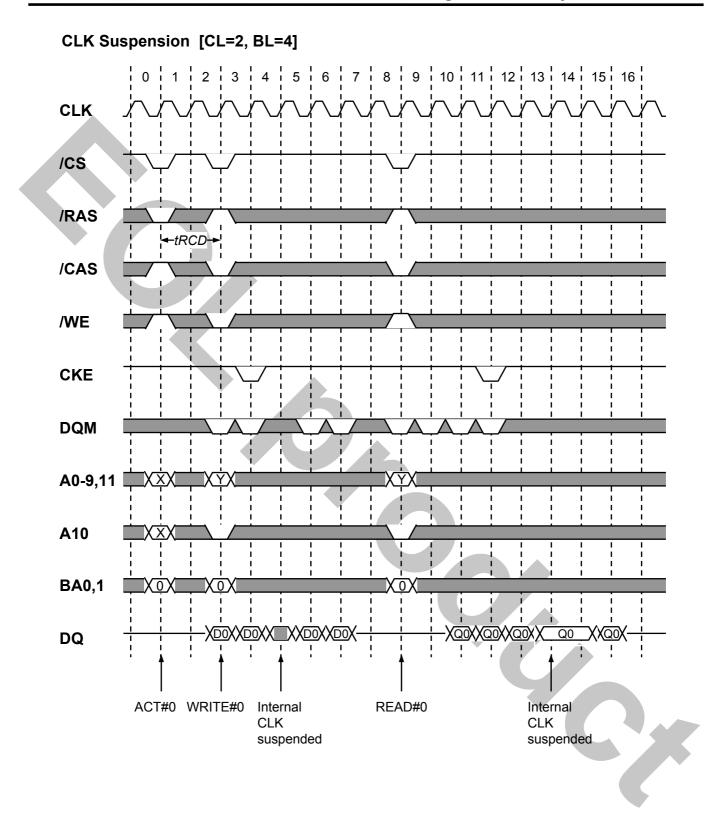
## **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM





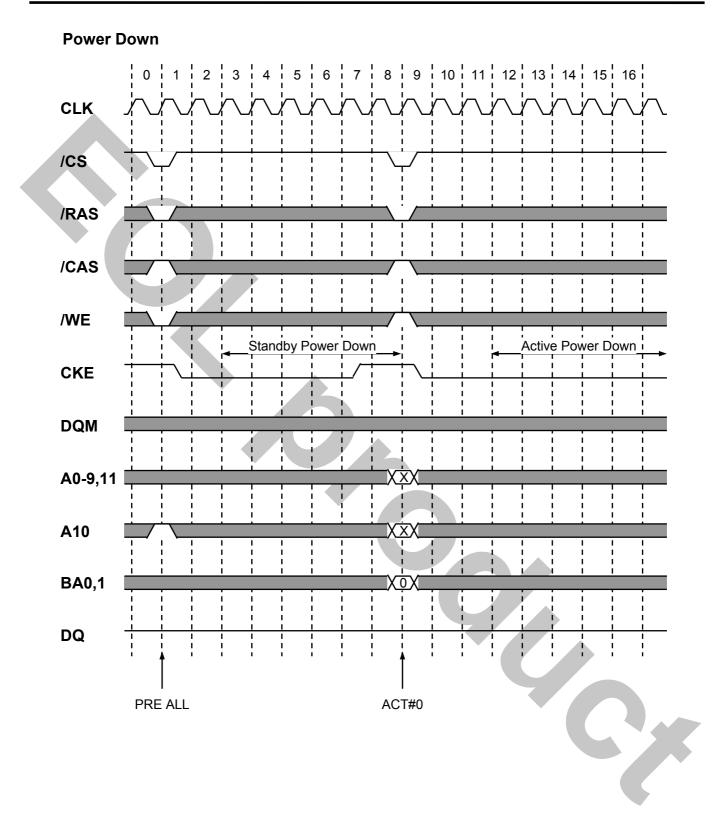
SDR SDRAM E0342M21 (Ver.2.1) February 2004 (K) Japan

## **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM



SDR SDRAM E0342M21 (Ver.2.1) February 2004 (K) Japan

# **M2V64S50ETP** 64M Single Data Rate Synchronous DRAM



#### NOTES FOR CMOS DEVICES -

### **①** PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

### 2 HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

### **③** STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

The information in this document is subject to change without notice. Before using this document, confirm that this is the latest version.

No part of this document may be copied or reproduced in any form or by any means without the prior written consent of Elpida Memory, Inc.

Elpida Memory, Inc. does not assume any liability for infringement of any intellectual property rights (including but not limited to patents, copyrights, and circuit layout licenses) of Elpida Memory, Inc. or third parties by or arising from the use of the products or information listed in this document. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of Elpida Memory, Inc. or others.

Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of the customer's equipment shall be done under the full responsibility of the customer. Elpida Memory, Inc. assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.

#### [Product applications]

Elpida Memory, Inc. makes every attempt to ensure that its products are of high quality and reliability. However, users are instructed to contact Elpida Memory's sales office before using the product in aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment, medical equipment for life support, or other such application in which especially high quality and reliability is demanded or where its failure or malfunction may directly threaten human life or cause risk of bodily injury.

#### [Product usage]

Design your application so that the product is used within the ranges and conditions guaranteed by Elpida Memory, Inc., including the maximum ratings, operating supply voltage range, heat radiation characteristics, installation conditions and other related characteristics. Elpida Memory, Inc. bears no responsibility for failure or damage when the product is used beyond the guaranteed ranges and conditions. Even within the guaranteed ranges and conditions, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Elpida Memory, Inc. products does not cause bodily injury, fire or other consequential damage due to the operation of the Elpida Memory, Inc. product.

#### [Usage environment]

This product is not designed to be resistant to electromagnetic waves or radiation. This product must be used in a non-condensing environment.

If you export the products or technology described in this document that are controlled by the Foreign Exchange and Foreign Trade Law of Japan, you must follow the necessary procedures in accordance with the relevant laws and regulations of Japan. Also, if you export products/technology controlled by U.S. export control regulations, or another country's export control laws or regulations, you must follow the necessary procedures in accordance with such laws or regulations.

If these products/technology are sold, leased, or transferred to a third party, or a third party is granted license to use these products, that third party must be made aware that they are responsible for compliance with the relevant laws and regulations.

M01E0107