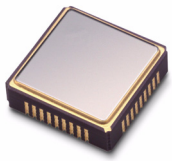
## GENERAL DESCRIPTION



The M2006-12A is a VCSO (Voltage Controlled SAW Oscillator) based clock generator PLL designed for clock frequency translation and jitter attenuation. Clock multiplication ratios (including forward and inverse FEC) are pin-selected from pre-programming look-up tables. Includes Hitless Switching and Phase Build-out to enable SONET (GR-253) / SDH (G.813) MTIE and TDEV compliance during reference clock reselection. Hitless Switching (HS) engages when a 4ns or greater clock phase change is detected.

*This phase-change triggered implementation of HS is not recommended when using an unstable reference (more than 1ns jitter pk-to-pk) or when the resulting phase detector frequency is less than 5MHz.*

## FEATURES

- ***Reduced intrinsic output jitter* and *improved power supply noise rejection* compared to M2006-12**
- **Similar to the M2006-02A - and pin-compatible - but *adds Hitless Switching and Phase Build-out functions***
- **Includes APC pin for Phase Build-out function (for absorption of the input phase change)**
- **Pin-selectable PLL divider ratios support forward and inverse FEC ratio translation**
- **Input reference and VCSO frequencies up to 700MHz (Specify VCSO frequency at time of order)**
- **Low phase jitter of 0.25 ps rms typical (12kHz to 20MHz or 50kHz to 80MHz)**
- **Commercial and Industrial temperature grades**
- **Single 3.3V power supply**
- **Small 9 x 9 mm SMT (surface mount) package**

## PIN ASSIGNMENT (9 x 9 mm SMT)

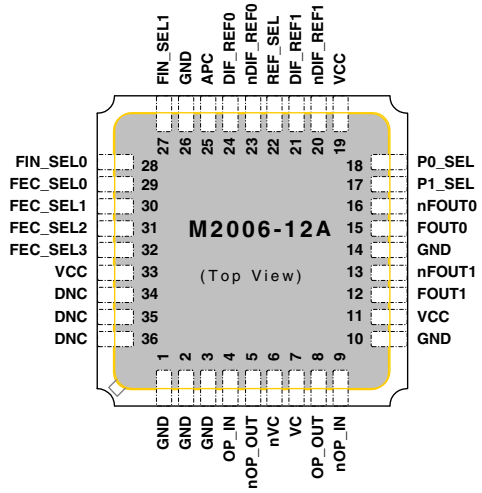



***Figure 1: Pin Assignment***

### Example I/O Clock Combinations

**Using M2006-12A-622.0800**

| PLL Ratio | Input Clock (MHz) | Output Clock (MHz) |
|---|---|---|
| 1/1 | 622.08, 155.52, 77.76, or 19.44 | 622.08 or 155.52 |
| 237/255 (inverse FEC) | 669.3266, 167.3316, 83.6658, or 20.9165 | |

**Table 1: Example I/O Clock Combinations Using M2006-12A-622.0800**

**Using M2006-12A-669.3266**

| PLL Ratio | Input Clock (MHz) | Output Clock (MHz) |
|---|---|---|
| 237/255 (FEC rate) | 622.08, 155.52, 77.76, or 19.44 | 669.3266 or 167.3316 |
| 1/1 | 669.3266, 167.3316, 83.6658, or 20.9165 | |

**Table 2: Example I/O Clock Combinations Using M2006-12A-669.3266**

## SIMPLIFIED BLOCK DIAGRAM

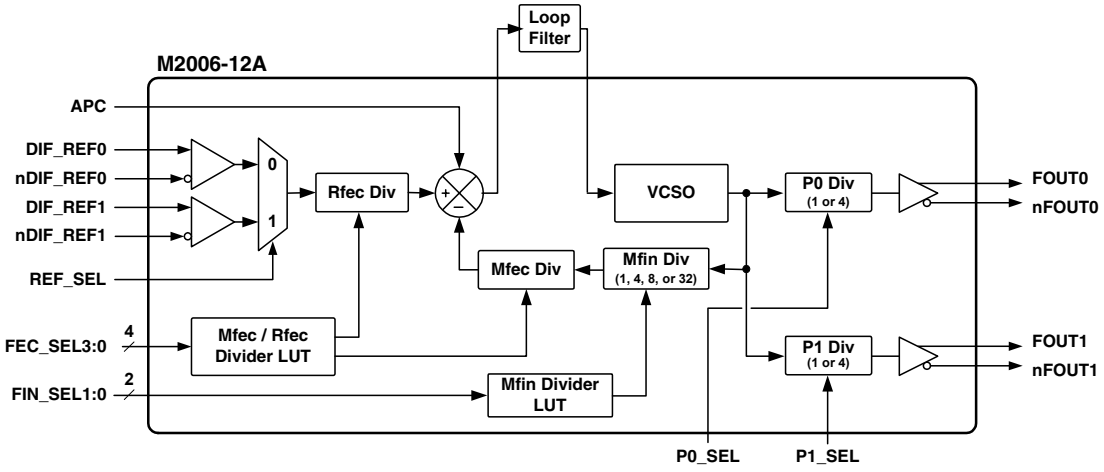



***Figure 2: Simplified Block Diagram***

## DETAILED BLOCK DIAGRAM

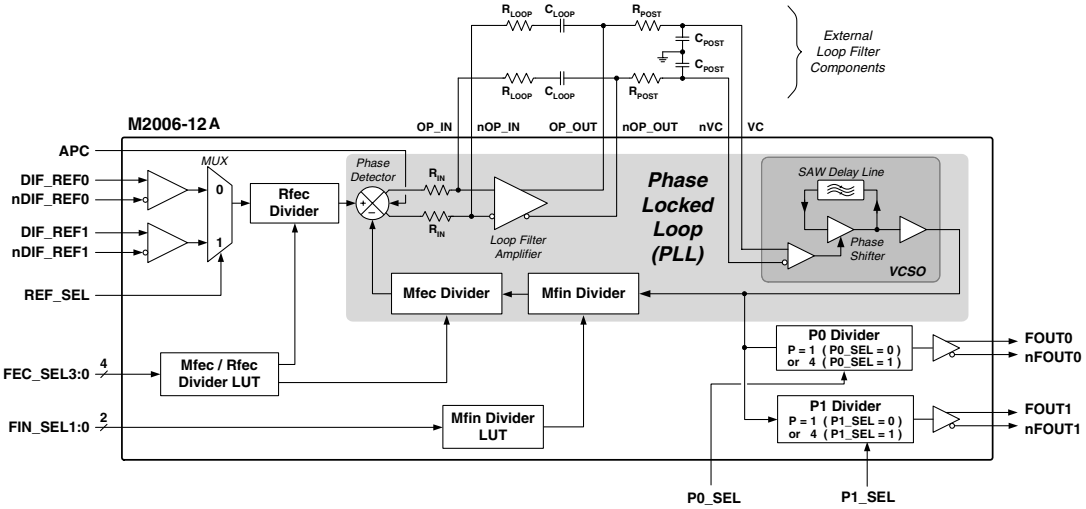



*Figure 3: Detailed Block Diagram*

## PIN DESCRIPTIONS

| Number | Name | I/O | Configuration | Description |
|---|---|---|---|---|
| 1, 2, 3, 10, 14, 26 | GND | Ground | | Power supply ground connections. |
| 4<br>9 | OP_IN<br>nOP_IN | Input | | External loop filter connections. See Figure 4. |
| 5<br>8 | nOP_OUT<br>OP_OUT | Output | | |
| 6<br>7 | nVC<br>VC | Input | | |
| 11, 19, 33 | VCC | Power | | Power supply connection, connect to +3.3V. |
| 12, 13<br>15, 16 | FOUT1, nFOUT1<br>FOUT0, nFOUT0 | Output | No internal terminator | Clock output pairs. Differential LVPECL. |
| 17<br>18 | P1_SEL<br>P0_SEL | Input | Internal pull-down resistor[1] | P Divider controls. LVCMOS/LVTTL.<br>(For P0_SEL, P1_SEL, see Table 6 on pg. 3. |
| 20<br>21 | nDIF_REF1<br>DIF_REF1 | Input | Internal pull-UP resistor[1]<br>Internal pull-down resistor[1] | Reference clock input pair 1.<br>Differential LVPECL or LVDS. |
| 22 | REF_SEL | Input | Internal pull-down resistor[1] | Reference clock input selection. LVCMOS/LVTTL:<br>Logic 1 selects DIF_REF1, nDIF_REF1.<br>Logic 0 selects DIF_REF0, nDIF_REF0. |
| 23<br>24 | nDIF_REF0<br>DIF_REF0 | Input | Internal pull-UP resistor[1]<br>Internal pull-down resistor[1] | Reference clock input pair 0.<br>Differential LVPECL or LVDS. |
| 25 | APC | Input | Internal pull-down resistor[1] | Automatic Phase Compensation (phase build-out). LVCMOS/LVTTL:<br>Logic 1 - Device absorbs input phase transients.<br>Logic 0 - Device doesn't absorb transients. |
| 27<br>28 | FIN_SEL1<br>FIN_SEL0 | Input | Internal pull-down resistor[1] | Input clock frequency selection. LVCMOS/LVTTL.<br>(For FIN_SEL1:0, see Table 4 on pg. 3. |
| 29<br>30<br>31<br>32 | FEC_SEL0<br>FEC_SEL1<br>FEC_SEL2<br>FEC_SEL3 | Input | Internal pull-UP resistor[1] | FEC PLL divider ratio selection. LVCMOS/ LVTTL.<br>(For FEC_SEL3:0, see Table 5 on pg. 3.) |
| 34, 35, 36 | DNC | | Do Not Connect. | Internal nodes. Connection to these pins can cause erratic device operation. |

**Table 3: Pin Descriptions**

## PLL DIVIDER LOOK-UP TABLES

### Mfin Divider Look-Up Table (LUT)

The FIN_SEL1:0 pins select the feedback divider value "Mfin" (for Frequency Input).

| FIN_SEL1:0 | Mfin Value | M2006-12A-622.0800 Sample Ref. Freq. (MHz) † |
|---|---|---|
| 1 1 | 1 * | 622.08 |
| 1 0 | 4 | 155.52 |
| 0 1 | 8 | 77.76 |
| 0 0 | 32 | 19.44 |

**Table 4: Mfin Divider Look-Up Table (LUT)**

Note *: *Do not use with FEC_SEL3:0=1100 or 1101* or an excessive phase detector frequency will result.
Note †: Example with M2006-12A-622.0800 and "Non-FEC ratio" selection made from Table 5 (FEC_SEL2=1).

### FEC PLL Ratio Dividers Look-up Table (LUT)

The FEC_SEL3:0 pins select the FEC feedback and reference divider values Mfec and Rfec.

| FEC_SEL3:0 | Mfec | Rfec[1] | Description |
|---|---|---|---|
| 0 0 0 0 | 236 | 255 | Inverse FEC ratio |
| 0 0 0 1 | 79 | 85 | Inverse FEC ratio, equivalent to 237/255 |
| 0 0 1 0 | 14 | 15 | Inverse FEC ratio, equivalent to 238/255 |
| 0 0 1 1 | 239 | 255 | Inverse FEC ratio |
| 0 1 0 0 | 236 | 236 | Non-FEC ratio, complements 0000 or 1000 [2] |
| 0 1 0 1 | 79 | 79 | Non-FEC ratio, complements 0001 or 1001 [2] |
| 0 1 1 0 | 14 | 14 | Non-FEC ratio, complements 0010 or 1010 [2] |
| 0 1 1 1 | 239 | 239 | Non-FEC ratio, complements 0011 or 1011 [2] |
| 1 0 0 0 | 255 | 236 | FEC ratio (OTU3) |
| 1 0 0 1 | 85 | 79 | FEC ratio, equivalent to 255/237 (OTU2) |
| 1 0 1 0 | 15 | 14 | FEC ratio, equivalent to 255/238 (OTU1) |
| 1 0 1 1 | 255 | 239 | FEC ratio |
| 1 1 0 0 | 1 | 1 | Non-FEC ratio [3] *Do not use these two settings with FIN_SEL1:0=11* |
| 1 1 0 1 | 2 | 2 | |
| 1 1 1 0 | 4 | 4 | Non-FEC ratio [3] |
| 1 1 1 1 | 8 | 8 | |

**Table 5: FEC PLL Ratio Dividers Look-up Table (LUT)**

Note 1: The phase detector frequency (Fpd, which is calculated as Fref/Rfec) should be above 1.5 MHz to prevent spurs on the output clock. To ensure the PLL remains locked when using a recovered clock (such as in loop timing mode), the phase detector frequency should ideally be about 20MHz, or at least less than 50 MHz.
Note 2: These table selections use the same or similar Mfec divider values as the complementary selections noted. This allows the use of the same loop filter component values and yields the same PLL loop bandwidth and damping factor values for complementary selections. Complementary selections can be actively switched in a given application.
Note 3: In non-FEC applications, these settings can be used to optimize phase detector frequency or to actively change PLL loop bandwidth.

### Post-PLL Dividers

The M2006-12A also features two post-PLL dividers, one for each output pair. The "P1" divider is for FOUT1 and nFOUT1; the "P0" divider is for FOUT0 and nFOUT0.

Each divides the VCSO frequency to produce one of two output frequencies (1/4 or 1/1 of the VCSO frequency). The P1_SEL and P0_SEL pins each select the value for their corresponding divider.

| P1_SEL, P0_SEL | P Value | M2006-12A-622.0800 Sample Output Frequency (MHz) |
|---|---|---|
| 1 | 4 | 155.52 |
| 0 | 1 | 622.08 |

**Table 6: P Divider Selector, Values, and Frequencies**

## FUNCTIONAL DESCRIPTION

The M2006-12A is a PLL (Phase Locked Loop) based clock generator that generates output clocks synchronized to one of two selectable input reference clocks.

An internal high "Q" SAW filter provides low jitter signal performance and controls the output frequency of the VCSO (Voltage Controlled SAW Oscillator).

Configurable FEC feedback and reference dividers (the "Mfec Divider" and "Rfec Divider") provide the multiplication ratios necessary to accomodate clock translation for both forward and inverse Forward Error Correction.

In addition, a configurable feedback divider (labeled "Mfin Divider") provides the broader division options needed to accomodate various reference clock frequencies.

For example, the **M2006-12A-622.0800** *(see "Ordering Information"* on pg. 10*)* has a 622.08MHz VCSO frequency:

- The inverse FEC PLL ratios (at top of Table 5) enable the **M2006-12A-622.0800** to accept "base" input reference frequencies of: 663.7255, 666.5143, 669.3266, 672.1627, and 622.08MHz.
- The Mfin feedback divider enables the actual input reference clock to be the "base" input frequency divided by 1, 4, 8, or 32. Therefore, for the base input frequency of 622.08MHz, the actual input reference clock frequencies can be: 622.08, 155.52, 77.76, and 19.44MHz. (See Table 4 on pg. 3.)

### The PLL

The PLL uses a phase detector and configurable dividers to synchronize the output of the VCSO with selected reference clock.

The “Mfin Divider” and “Mfec Divider” divide the VCSO frequency, feeding the result into the phase detector.

The selected input reference clock is divided by the “Rfec Divider”. The result is fed into the other input of the phase detector.

The phase detector compares its two inputs. It then outputs pulses to the loop filter as needed to increase or decrease the VCSO frequency and thereby match and lock the divider output’s frequency and phase to those of the input reference clock.

Due to the narrow tuning range of the VCSO (±200ppm), appropriate selection of all of the following are required for the PLL be able to lock: VCSO center frequency, input frequency, and divider selections.

*See also “Maintaining PLL Lock:” on pg. 4.*

### Relationship Among Frequencies and Dividers

The VCSO center frequency must be specified at time of order. The relationship between the VCSO (Fvcso) frequency, the Mfin divider, the Mfec divider, the Rfec divider, and the input reference frequency (Fin) is:

$$Fvcso = Fin \times Mfin \times \frac{Mfec}{Rfec}$$

As an example, for the **M2006-12A-622.0800**, the non-FEC and inverse-FEC PLL ratios in Table 5 enable use with these corresponding input reference frequencies:

| M2006-12A-622.0800 VCSO Clock Frequency (MHz) ÷ | FEC Ratio | M2006-12A-622.0800 Base Input Ref. = Frequency (MHz) [1] |
|---|---|---|
| 622.08 | 1 / 1 | 622.0800 |
| | 238 / 255 | 666.5143 |
| | 237 / 255 | 669.3266 |
| | 236 / 255 | 672.1627 |

**Table 7: Example FEC PLL Rations and Input Reference Frequencies**

Note 1: Input reference clock (“Fin”) can be the base frequency shown divided by “Mfin” (as shown in Table 4 on pg. 3).

**Maintaining PLL Lock:**

The narrow tuning range of the VCSO requires that the input reference frequency must remain suitable for the current look-up table selection. For example, when switching between “Inverse FEC ratio” and “Non-FEC ratio” look-up table selections (see Table 5 on pg. 3), the input reference frequency must change accordingly in order for the PLL to lock.

*An out-of-lock condition due to an inappropriate configuration will typically result in the VCSO operating at its lower or upper frequency rail, which is approximately 200ppm above or below the nominal VCSO center frequency.*

See also *“Hitless Switching (HS)”* (next) for an additional issue with regard to phase locking.

### Hitless Switching (HS)

The M2006-12A includes a proprietary Hitless Switching (HS) feature that prevents an excessive phase transient of the output clocks upon input reference rearrangement. Upon the occurance of an input reference phase change, or phase transient, PLL bandwidth is lowered by the HS function. This limits the rate of phase change in the output clocks. With proper configuration of the external loop filter, the output clocks will comply with MTIE (maximum time interval error) specifications for GR-253 (SONET) and ITU G.813 (SDH) during input reference clock change, depending on the magnitude of the resulting phase change.

The HS function uses a phase error detector at the phase detector to detect a clock phase change. During normal operation with a stable reference clock, the PLL will be frequency locked and phase locked, resulting in very little error at the phase detector (<1 ns). Upon the selection of a new input reference clock at a different clock phase, a phase error will occur at the phase detector. The HS function is triggered with a phase error greater than 4 ns, upon which a narrow PLL bandwidth is applied. When the PLL locks to within 2 ns error at the phase detector, wide bandwidth (normal) operation is resumed.

The HS function is not suitable for situations in which an unstable reference is used. Under normal conditions the reference clock jitter should not induce phase jitter at the phase detector beyond 2 ns. (This includes when subjecting the system to jitter tolerance compliance testing.) Because of this, the M2006-12A is not recommended for use with some Stratum DPLL clock sources, or with unstable recovered network clocks intended for loop timing configuration. It is also not recommended for complex FEC ratios where the phase detector is operated at less 1 MHz. For these applications the M2006-02A is suggested. The M2006-02A is identical to the M2006-12A except that it does not include the HS function (nor the APC pin and phase build-out function, which are discussed in the following section).

### Automatic Phase Compensation (APC) Pin

The M2006-12A also includes a phase build-out function that can be selectively enabled by asserting the APC input (pin 25) to logic 1. The phase build-out function works in conjunction with the HS function. When the APC pin is asserted, the phase build-out function enables the PLL to absorb most of the phase change of the input clock which reduces re-lock time and the generation of wander. (Wander is created in this case by the generation of extra output clock cycles.)

When the APC pin is asserted, the phase build-out function is triggered by same >4 ns phase transient (at the phase detector) that triggers the HS function. Once triggered, a new VCSO clock edge is selected for the phase comparator feedback input. (The clock edge selected is the one closest in phase to the new input clock phase.) The residual phase detector phase error following reselection is approximately 3-to-4 ns. The narrow bandwidth selected by HS minimizes VCSO drifting and switch transients during the process.

It is recommended that the APC pin remain low when the phase detector frequency is less than 4 MHz. Otherwise, the M2006-12A may have difficulty locking to reference upon power-up.

### Outputs

The M2006-12A provides a total of two differential LVPECL output pairs: FOUT1 and FOUT0. Because each output pair has its own P divider, the FOUT1 pair and the FOUT0 can output the two different frequencies at the same time. For example, FOUT1 can output 155.52MHz while FOUT0 outputs 622.08MHz.

*Any unused output should be left unconnected (floating) in the system application. This will minimize output switching current and therefore minimize noise modulation of the VCSO.*

### External Loop Filter

To provide stable PLL operation, and thereby a low jitter output clock, the M2006-12A requires the use of an external loop filter. This is provided via the provided filter pins (see Figure 4).

Due to the differential signal path design, the implementation requires two identical complementary RC filters as shown here.

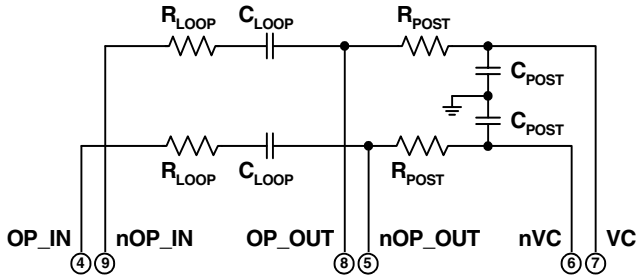



***Figure 4: External Loop Filter***

*See Example External Loop Filter Component Values table.*

PLL bandwidth is affected by loop filter component values, “Mfec” and “Mfin” values, and the “PLL Loop Constants” listed in AC Characteristics on pg. 8.

The various “Non-FEC ratio” settings can be used to actively change PLL loop bandwidth in a given application. See “FEC PLL Ratio Dividers Look-up Table (LUT)” on pg. 3.

### PLL Simulator Tool Available

A free PC software utility is available on the ICS website (www.icst.com). The M2000 Timing Modules PLL Simulator is a downloadable application that simulates PLL jitter and wander transfer characteristics. This enables the user to set appropriate external loop component values in a given application.

*Go to the SAW PLL Simulator Software web page at www.icst.com/products/calculators/m2000filterSWdesc.htm*

### Example External Loop Filter Component Values[1]

*VCSO Parameters: $K_{VCO}$ = 800kHz/V, $R_{IN}$ = 50kΩ, VCSO Bandwidth = 700kHz.*

| Device Configuration | | | | Example External Loop Filter Component Values | | | | Nominal Performance Using These Values | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $F_{Ref}$ (MHz) | $F_{VCSO}$ (MHz) | FIN_SEL1:0 pins | FEC_SEL3:0 pins | R loop | C loop | R post | C post | PLL Loop Bandwidth | Damping Factor | Passband Peaking (dB) |
| 19.44 | 622.08 | 0 0 | 1 1 0 0 | 11.5kΩ | 2.2µF | 34kΩ | 470pF | 1kHz | 6.0 | 0.05 |
| 77.76 | | 0 1 | 1 1 1 0 | | | | | | | |
| 155.52 | | 1 0 | 1 1 1 1 | | | | | | | |
| 622.08 | | 1 1 | 0 1 1 0 | 5.11kΩ | 4.7µF | | | | 6.0 | 0.06 |
| 167.3317 | | 1 0 | 0 0 0 1 | 113.0kΩ | 0.22µF | | | | 6.0 | 0.06 |
| 669.3266 | | 1 1 | | 28.0kΩ | 1.0µF | | | | 6.3 | 0.05 |
| 155.52 | 669.3266 | 1 0 | 1 0 0 1 | 121.0kΩ | 0.22µF | | | | 6.0 | 0.05 |
| 622.08 | | 1 1 | | 30.1kΩ | 1.0µF | | | | 6.5 | 0.05 |

**Table 8: Example External Loop Filter Component Values**

Note 1: $K_{VCO}$ , VCSO Bandwidth, M Divider Value, and External Loop Filter Component Values determine Loop Bandwidth, Damping Factor, and Passband Peaking. For PLL Simulator software, go to www.icst.com.

## ABSOLUTE MAXIMUM RATINGS[1]

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_I$ | Inputs | -0.5 to $V_{CC}$ +0.5 | V |
| $V_O$ | Outputs | -0.5 to $V_{CC}$ +0.5 | V |
| $V_{CC}$ | Power Supply Voltage | 4.6 | V |
| $T_S$ | Storage Temperature | -45 to +100 | °C |

**Table 9: Absolute Maximum Ratings**

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in Recommended Conditions of Operation, DC Characteristics, or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## RECOMMENDED CONDITIONS OF OPERATION

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Positive Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $T_A$ | Ambient Operating Temperature | | | | | |
| | | Commercial | 0 | | +70 | °C |
| | | Industrial | -40 | | +85 | °C |

**Table 10: Recommended Conditions of Operation**

## ELECTRICAL SPECIFICATIONS

### DC Characteristics

*Unless stated otherwise, $V_{CC}$ = 3.3V ±5%, $T_A$ = 0 °C to +70 °C (commercial), $T_A$ = -40 °C to +85 °C (industrial), $F_{VCSO}$ = $F_{OUT}$ = 622-675MHz, LVPECL outputs terminated with 50Ω to $V_{CC}$ - 2V*

| | Symbol | Parameter | | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|
| Power Supply | $V_{CC}$ | Positive Supply Voltage | | 3.135 | 3.3 | 3.465 | V | |
| | $I_{CC}$ | Power Supply Current | | | 175 | 225 | mA | |
| All Differential Inputs | $V_{P-P}$ | Peak to Peak Input Voltage | DIF_REF0, nDIF_REF0, DIF_REF1, nDIF_REF1 | 0.15 | | | V | |
| | $V_{CMR}$ | Common Mode Input | | 0.5 | | $V_{cc}$ - .85 | V | |
| | $C_{IN}$ | Input Capacitance | | | | 4 | pF | |
| Differential Inputs with Pull-down | $I_{IH}$ | Input High Current (Pull-down) | DIF_REF0, DIF_REF1 | | | 150 | µA | $V_{CC}$ = $V_{IN}$ = 3.456V |
| | $I_{IL}$ | Input Low Current (Pull-down) | | -5 | | | µA | |
| | $R_{pulldown}$ | Internal Pull-down Resistance | | | 50 | | kΩ | |
| Differential Inputs with Pull-up | $I_{IH}$ | Input High Current (Pull-up) | nDIF_REF0, nDIF_REF1 | | | 5 | µA | $V_{IN}$ = 0 to 3.456V |
| | $I_{IL}$ | Input Low Current (Pull-up) | | -150 | | | µA | |
| | $R_{pullup}$ | Internal Pull-up Resistance | | | 50 | | kΩ | |
| All LVCMOS / LVTTL Inputs | $V_{IH}$ | Input High Voltage | APC, REF_SEL, FIN_SEL1, FIN_SEL0, FEC_SEL3, FEC_SEL2, FEC_SEL1, FEC_SEL0, P1_SEL, P0_SEL | 2 | | $V_{cc}$ + 0.3 | V | |
| | $V_{IL}$ | Input Low Voltage | | -0.3 | | 0.8 | V | |
| | $C_{IN}$ | Input Capacitance | | | | 4 | pF | |
| LVCMOS / LVTTL Inputs with Pull-down | $I_{IH}$ | Input High Current (Pull-down) | REF_SEL, FIN_SEL1, FIN_SEL0, P1_SEL, P0_SEL | | | 150 | µA | $V_{CC}$ = $V_{IN}$ = 3.456V |
| | $I_{IL}$ | Input Low Current (Pull-down) | | -5 | | | µA | |
| | $R_{pulldown}$ | Internal Pull-down Resistance | | | 50 | | kΩ | |
| LVCMOS / LVTTL Inputs with Pull-up | $I_{IH}$ | Input High Current (Pull-up) | FEC_SEL3, FEC_SEL2, FEC_SEL1, FEC_SEL0 | | | 5 | µA | $V_{CC}$ = 3.456V $V_{IN}$ = 0 V |
| | $I_{IL}$ | Input Low Current (Pull-up) | | -150 | | | µA | |
| | $R_{pullup}$ | Internal Pull-up Resistance | | | 50 | | kΩ | |
| Differential Outputs | $V_{OH}$ | Output High Voltage | FOUT0, nFOUT0, FOUT1, nFOUT1 | $V_{cc}$ - 1.4 | | $V_{cc}$ - 1.0 | V | |
| | $V_{OL}$ | Output Low Voltage | | $V_{cc}$ - 2.0 | | $V_{cc}$ - 1.7 | V | |
| | $V_{P-P}$ | Peak to Peak Output Voltage [1] | | 0.4 | | 0.85 | V | |

Note 1: Single-ended measurement. See Figure 5, Output Rise and Fall Time, on pg. 8.

**Table 11: DC Characteristics**

## ELECTRICAL SPECIFICATIONS (CONTINUED)

### AC Characteristics

*Unless stated otherwise, $V_{CC}$ = 3.3V ±5%, $T_A$ = 0 °C to +70 °C (commercial), $T_A$ = -40 °C to +85 °C (industrial), $F_{VCSO}$ = $F_{OUT}$ = 622-675MHz, LVPECL outputs terminated with 50Ω to $V_{CC}$ - 2V*

| | Symbol | Parameter | | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Input Frequency Range | $F_{IN}$ | Input Frequency | DIF_REF0, nDIF_REF0, DIF_REF1, nDIF_REF1 | 10 | | 700 | MHz | |
| Output Frequency | $F_{FOUT}$ | Output Frequency Range | FOUT0, nFOUT0, FOUT1, nFOUT1 | 100 | | 700 | MHz | |
| | APR | VCSO Pull-Range | Commercial | ±120 | ±200 | | ppm | |
| | | | Industrial | ±50 | ±150 | | ppm | |
| PLL Loop Constants [1] | $K_{VCO}$ | VCO Gain | | | 800 | | kHz/V | |
| | $R_{IN}$ | Internal Loop Resistor | | | 50 | | kΩ | |
| | $BW_{VCSO}$ | VCSO Bandwidth | | | 700 | | kHz | |
| Phase Noise and Jitter | Φn | Single Side Band Phase Noise @622.08MHz | 1kHz Offset | | -72 | | dBc/Hz | Fin=19.44 MHz Mfin=32, Mfec=1, Rfec=1 |
| | | | 10kHz Offset | | -94 | | dBc/Hz | |
| | | | 100kHz Offset | | -123 | | dBc/Hz | |
| | J(t) | Jitter (rms) @622.08MHz | 12kHz to 20MHz | | 0.25 | 0.5 | ps rms | |
| | | | 50kHz to 80MHz | | 0.25 | 0.5 | ps rms | |
| | $t_{PW}$ | Output Duty Cycle [2] FOUT0, nFOUT0, FOUT1, nFOUT1 | P0, P1 = 1 | 40 | 50 | 60 | % | |
| | | | P0, P1 = 4 | 45 | 50 | 55 | % | |
| | $t_R$ | Output Rise Time [2] | FOUT0, nFOUT0, FOUT1, nFOUT1 | 200 | 450 | 500 | ps | 20% to 80% |
| | $t_F$ | Output Fall Time [2] | | 200 | 450 | 500 | ps | 20% to 80% |

**Table 12: AC Characteristics**

Note 1: Parameters needed for PLL Simulator software; see PLL Simulator Tool Available on pg. 5.
Note 2: See Parameter Measurement Information on pg. 8.

## PARAMETER MEASUREMENT INFORMATION

### Output Rise and Fall Time

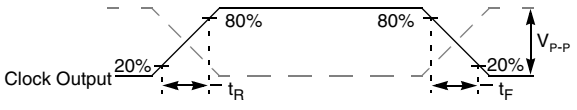



***Figure 5: Output Rise and Fall Time***

### Output Duty Cycle

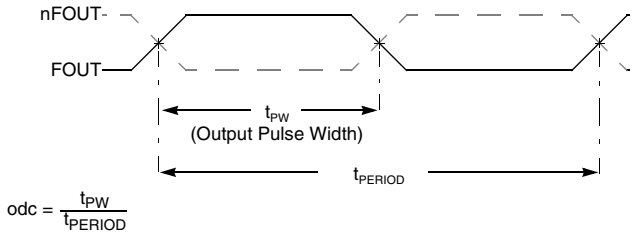
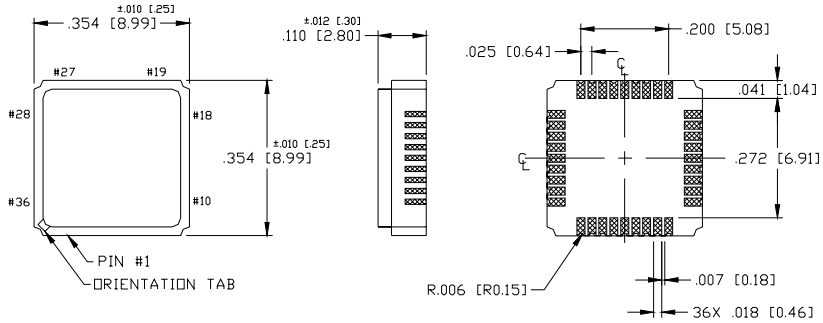



***Figure 6: Output Duty Cycle***

## DEVICE PACKAGE - 9 x 9mm CERAMIC LEADLESS CHIP CARRIER

**Mechanical Dimensions:**




*Refer to the SAW PLL application notes web page at www.icst.com/products/appnotes/SawPllAppNotes.htm for application notes, including recommended PCB footprint, solder mask, and furnace profile.*

NOTES:

1. DIMENSIONS ARE IN INCHES, DIMENSIONS IN [ ] ARE MM.
2. UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE ±.005 [.13]

***Figure 7: Device Package - 9 x 9mm Ceramic Leadless Chip Carrier***

## ORDERING INFORMATION

**Part Numbering Scheme**

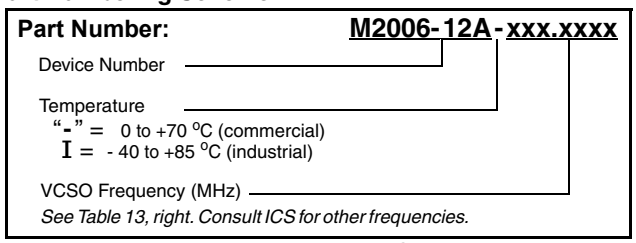



***Figure 8: Part Numbering Scheme***

**Standard VCSO Output Frequencies (MHz)***

*Consult ICS for the availablity of other VCSO frequencies*

| | |
|---|---|
| 622.0800 | 669.3120 |
| 625.0000 | 669.3266 |
| 627.3296 | 669.6429 |
| 644.5313 | 670.8386 |
| 666.5143 | 672.1600 |
| 669.1281 | 690.5692 |

**Table 13: Standard VCSO Output Frequencies (MHz)**

Note *: Fout can equal Fvcso divided by: 1 or 4

*Consult ICS for the availability of other PLL frequencies.*

**Example Part Numbers**

| PLL Frequency (MHz) | Temperature | Order Part Number |
|---|---|---|
| 622.08 | commercial | **M2006-12A-622.0800** |
| | industrial | **M2006-12AI622.0800** |
| 625.00 | commercial | **M2006-12A-625.0000** |
| | industrial | **M2006-12AI625.0000** |
| 669.3266 | commercial | **M2006-12A-669.3266** |
| | industrial | **M2006-12AI669.3266** |
| 669.6429 | commercial | **M2006-12A-669.6429** |
| | industrial | **M2006-12AI669.6429** |

**Table 14: Example Part Numbers**