SHARP

SPEC No.	
ISSUE :	Sep. 2 1999

To : EDI

SPECIFICATIONS

Product Type LZ9G Series 1600 Gates Gate Array

Model No. LZ9GF16

※ This specifications contains 22 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

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●When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).
- Office electronics
- Instrumentation and measuring equipment
- Machine tools
- Audiovisual equipment
- Home appliances
- Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
- Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- Mainframe computers
- Traffic control systems
- Gas leak detectors and automatic cutoff devices
- Rescue and security equipment
- Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.
- Aerospace equipment
- Communications equipment for trunk lines
- Control equipment for the nuclear power industry
- Medical equipment related to life support, etc.

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●Please direct all queries regarding the products covered herein to a sales representative of the company.

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1. Introduction

This data sheet is to introduce the specification of LZ9GF16, timing control IC for TFT-LCD module.

The functions and the uses

Timing control IC for 5" size and 5.6" size TFT-LCD module

Horizontal frequency driver(NTSC:600 divided frequency /PAL:604 divided frequency) and phase comparator circuit for the PLL circuit are built in.

By adding voltage Controlled Oscillator(VCO) and Low Pass Filter(LPF) to this IC to make the PLL circuit, following signals synchronized with input composite sync. Signal(SYNI) and vertical sync. Signal(VIN) conforming to NTSC or PAL are generated.

1) Driving signal for source driver	: CLD, SPD
2) Control signal for source driver	: CTR, DIS
3) Driving signal for gate driver	: CLS, SPS
4) Control signal for gate driver	: LOWO
5) Control signal for gate driver power supply making	: GPS
6) Polarity alternating signal for common electrode driving signal	: FRPT
7) Polarity alternating signal for video signal	: FRPV
8) Control signal for the backlight PWM brightness control	: CHK

Illustration of control circuit	: See fig. 1-a ~ 1-c
Input/Output signal timing chart for above cases	: See fig. 2-a ~ 2-j

2. Feature

Process		: CMOS
Wafer substrate		: P-type silicon substrate
Package	(pin & type)	: 48QFP (0.75mm pin pitch)
	(material)	: Plastics
Operating Temperature		: -30°C ~ +85°C
Propagation delay time		: 0.9ns/gate

(Condition : 2-input NAND, Fanout=2, wire length=2mm, supply voltage=5V, Operating temperature Topr=25°C)

*REMARK

Not designed or rated as radiation hardened.
You cannot rewrite the program.

3. Pin Assignment

PIN No.	I/O	Signal Name	PIN No.	I/O	Signal Name
1	ICS	VIN	25	01M	SPD
2	ORZ	CVOP	26	02M	CLD
3	ICS	CVIN	27	OSCO	OSCO
4	ORZ	DVOP	28	OSCB	OSCI
5	ORZ	FRPT	29	ORZ	SAMO
6	ORZx2	GPS	30	-	V_{DD}
7	-	GND	31	-	GND
8	IOCU2M	EXCL	32	ICU	TESTI
9	ICS	SYNI	33	ICS	LOWI
10	IOCURZ	HSY	34	IOCURZ	FRPV
11	IOCURZ	VSY	35	ICU	RESH
12	ORZ	DIS	36	TO1M	PDP
13	01M	TESTO	37	ICS	RESV
14	ICU	NTPC	38	ICU	TESTI
15	ICU	VRVC	39	ICU	TESTI
16	ICU	HRVC	40	ORZ	IHR
17	ORZ	CHK	41	ORZx2	HR
18	ICU	TESTI	42	ICU	CLOC
19	ORZ	TESTO	43	ICU	CLKC
20	ORZ	VR	44	ICU	TESTI
21	ORZ	SPS	45	ICU	SAMC
22	ORZ	CLS	46	ICS	BLKI
23	ORZ	LOWO	47	ORZ	BLKO
24	ORZ	CTR	48	ORZ	SYNO

ICU : Input buffer CMOS level with PULL UP resistance R=250kΩ
ICS : Schmitt-trigger Input buffer CMOS level
01M : Output buffer I_{OL}=0.8mA
02M : Output buffer I_{OL}=1.6mA
ORZ : Slew rate controlled Output buffer I_{OL}=80μA
ORZx2 : Slew rate controlled Output buffer I_{OL}=160μA .
* ORZ×2 buffer is connected two ORZ buffer in parallel.
TO1M : Tri-state Output buffer I_{OL}=0.8mA
IOCU2M : Bidirecional buffer CMOS level with PULL UP resistance R=250kΩ, I_{OL}=1.6mA
IOCURZ : Slew rate controlled Bidirecional buffer CMOS level with PULL UP resistance R=250kΩ, I_{OL}=80μA
OSCB : Oscillator Bidirecional buffer with oscillation stop control I_{OL}=3.2mA
OSCO : Oscillator Output buffer I_{OL}=1.6mA
V_{DD} : Power supply pin
GND : Earth pin

4. Explanation of Input / Output signal

PIN No.	Signal Name	Explanation	I/O
1	VIN	Vertical sync. Signal input (Positive)	I
2	CVOP	Vertical sync. Signal Output for Count Down circuit	0
3	CVIN	Vertical sync. Signal input for Count Down circuit	I
4	DVOP	Vertical sync. Signal output for digital separator circuit (Positive)	0
5	FRPT	Polarity alternating signal output for common electrode driving signal	0
6	GPS	Logic pals output for gate driver power supply making	0
7	GND	Ground	-
8	EXCL	Input / Output for outside Clock signal	I/0
9	SYNI	Composite sync. signal input	I
10	HSY	Internal horizontal sync. signal output (Negative)	I/0
11	VSY	Internal vertical sync. signal output (Negative)	I/0
12	DIS	Control signal output for source driver	0
13	TESTO	Monitor signal output for test	0
14	NTPC	Terminal for display mode change NTSC or PAL 【Note1】	I
15	VRVC	Input for the Vertical scanning direction setting 【Note2】	I
16	HRVC	Input for the horizontal scanning direction setting 【Note3】	I
17	CHK	Output for signal of backlight brightness control	0
18	TESTI	Input terminal for test 【Note4】	I
19	TESTO	Monitor signal output for test	0
20	IVR	Scanning setting input for gate driver	0
21	SPS	Resetting signal output for gate driver	0
22	CLS	Clock signal output for gate driver	0
23	LOWO	Control signal output for gate driver	0
24	CTR	Control signal output for source driver	0
25	SPD	Starting signal output for source driver	0
26	CLD	Clock signal output for source driver	0
27	OSCO	Output for clock oscillator circuit	0
28	OSCI	Input for clock oscillator circuit	I
29	SAMO	Control signal output for source driver	0
30	V_{DD}	Power supply voltage	-
31	GND	Ground	-
32	TESTI	Input terminal for test 【Note4】	I
33	LOWI	Input for initial reset signal	I
34	FRPV	Polarity alternating signal output for video signal	0
35	RESH	Horizontal counter resetting input 【Note5】	I
36	PDP	Output for phase comparative signal of PLL circuit	0
37	RESV	Vertical counter resetting input 【Note6】	I
38	TESTI	Input terminal for test 【Note4】	I
39	TESTI	Input terminal for test 【Note4】	I
40	IHR	Horizontal scanning setting output for source driver	0
41	HR	Horizontal scanning setting output for source driver	0
42	CLOC	Input for EXCL signal output setting 【Note7】	I
43	CLKC	Input for EXCL, HSY and VSY signal input / output setting 【Note8】	I
44	TESTI	Input terminal for test 【Note4】	I
45	SAMC	Terminal for sampling mode setting 【Note9】	I
46	BLKI	Input for phase comparative signal of PLL circuit. Input for delay signal of BLKO	I
47	BLKO	Output for phase comparative signal of PLL circuit Signal shall be inputted to BLKI through delay circuit 【Note10】	0
48	SYNO	Composite sync. signal output for vertical sync. separator signal (Positive)	0

【Note1】 NTPH=H : NTSC method
NTPC=L : MBK-PAL method

【Note2】 VRVC=H : Normally (Positive scanning)
VRVC=L : Reversal (Negative scanning)

【Note3】 HRVC=H : Normally (Positive scanning)
HRVC=L : Reversal (Negative scanning)
(Refer : 9, Scanning direction setting)

【Note4】 Normal state : H level

【Note5】 RESH=H : Normally
RESH=L : forcible reset

【Note6】 RESV=H : Normally
RESV=L : forcible reset

【Note7】 CLOC=H : L level output
CLOC=L : H level output

【Note8】 CLKC=H : EXCL, HSY, VSY terminals become output mode
CLKC=L : EXCL, HSY, VSY terminals become input mode

【Note9】 SAMC=H : It is the independent data-sampling timing at RGB
SAMC=L : It is the simultaneous data-sampling timing at RGB dots

【Note10】 Horizontal display position is changed by delay time

5. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	-0.3～+6.0	V
Input voltage	V_I	-0.3～V_{DD}+0.3	V
Output voltage	V_O	-0.3～V_{DD}+0.3	V
Oerating temperature	Topr	-30～+85	℃
Storage temperature	Tstg	-55～+150	℃

6. Electrical Specification

6-1 Operating conditions

Parameter	Symbol	min	typ	max	Unit
Supply voltage	V_{DD}	4.5	5.0	5.5	V
Operating temperature	Topt	-30	-	+85	℃

【Note】 Input/Output terminal of TESTI, TESTO should be used under the following conditions.

Signal Name	I/O	Used condition
TESTI	I	Fixed H level
TESTO	O	Connected GND by 0.1μF capacitor

6-2 Electrical characteristics

(V_{DD}=+5V±10%, Topr=-30～+85℃)

Parameter	Symbol	Test condition	min	typ	max	unit	#
Input "High" voltage	V_{IH}		3.5			V	1
Input "Low" voltage	V_{IL}				1.5	V	
Input "High" voltage	V_{T+}	Schmitt-trigger Input buffer			3.7	V	2
Input "Low" voltage	V_{T-}		1.0			V	
Hysteresis voltage	V_{T+} - V_{T-}		0.2			V	
Input "High" current	$\lvert I_{IH1} \rvert$	V_I=V_{DD}			1.0	μA	3
Input "Low" current	$\lvert I_{IL1} \rvert$	V_I=0V			1.0	μA	
Input "High" current	$\lvert I_{IH2} \rvert$	V_I=V_{DD}			2.0	μA	4
Input "Low" current	$\lvert I_{IL2} \rvert$	V_I=0V	5.0		75.0	μA	
Output "High" voltage	V_{OH1}	I_{OH}=-1.6mA	4.0			V	5
Output "Low" voltage	V_{OL1}	I_{OL}= 1.6mA			0.4	V	
Output "High" voltage	V_{OH2}	I_{OH}=-0.8mA	4.0			V	6
Output "Low" voltage	V_{OL2}	I_{OL}= 1.6mA			0.4	V	
Output "High" voltage	V_{OH3}	I_{OH}=-0.4mA	4.0			V	7
Output "Low" voltage	V_{OL3}	I_{OL}= 0.8mA			0.4	V	
Output "High" voltage	V_{OH4}	I_{OH}=-80μA	4.0			V	8
Output "Low" voltage	V_{OL4}	I_{OL}= 80μA			0.4	V	
Output "High" voltage	V_{OH5}	I_{OH}=-160μA	4.0			V	9
Output "Low" voltage	V_{OL5}	I_{OL}= 160μA			0.4	V	
Output "Low" voltage	V_{OL6}	I_{OL}= 3.2mA			0.4	V	10
Output leakage current	$\lvert I_{OZ} \rvert$	High impedance			1.0	μA	11

#1: Applied to input pins (ICU) and Bidirecional pins (OSCB, IOCU2M, IOCURZ) input mode
#2: Applied to input pins (ICS)
#3: Applied to input pins (ICS) and Bidirecional pin (OSCB) input mode
#4: Applied to input pins (ICU) and Bidirecional pins (IOCU2M, IOCURZ) input mode
#5: Applied to output pin (OSCO)
(OSCO : under the condition the input level of OSCB (input mode) = V_{DD} or 0V)
#6: Applied to output pin (O2M) and Bidirecional pin (IOCU2M) output mode
#7: Applied to output pins (O1M, TO1M)
#8: Applied to output pins (ORZ) and Bidirecional pins (IOCURZ) output mode
#9: Applied to output pins (ORZx2)
#10: Applied to Bidirecional pin (OSCB) output mode
#11: Applied to output pin (TO1M)

7. Condition for signal input

7-1 In case of using PLL circuit (CLKC=H)

Clock input : OSCI

Parameter	Symbol	min	typ	max	unit	remarks
Input frequency	$1/T_O$		9.4		MHz	
Duty ratio	T_{OL}/T_{OH}	40/60	50/50	60/40	%	

Composite (Horizontal) sync. signal (Positive) : SYNI

Input condition	remarks
Base on NTSC(M) system	NTPC=H
Base on PAL(B, G) system	NTPC=L

Horizontal sync. signal : VIN

Parameter		Symbol	min	typ	max	unit	remarks
Input frequency	NTSC	f_{VIN}	$f_{SYN}/284$	$f_{SYN}/264$	$f_{SYN}/258$	kHz	NTPC=H
	PAL	$f_H(P)$	$f_{SYN}/344$	$f_{SYN}/312$	$f_{SYN}/304$	kHz	NTPC=L
Pulse width		T_{VH}	65		600	μs	
HSY-VIN phase differnce		T_{HV}	16		58	μs	【Note1】

【Note1】 Timing of VIN input to be specified. (See fig. 2-h)

【Note2】 fsyn=SYNI (composite sync. signal) input frequency (unit : kHz)

【Note3】 In case of no VIN input, vertical counter inside of IC is reset automatically based on $f_{SYN}/284$ (NTPC=H), $f_{SYN}/344$ (NTPC=L).

【Note4】 After VSY falling, VIN input is invalid during the period of 192H(NTPC=H), 227H(NTPC=L). (1H=1/ f_{SYN})
However, the case of VSY falling by automatic reset is exceptional.

Input LOWI, RESH and RESV
Input V_{DD} through and integration circuit(Control circuitry example : refernces) with following value(τ_v),
or please input the Low level after V_{DD} turning on by this period system reset.

Symbol	min	typ	max	Unit
τ_v	20		100	ms

7-2 In case of input outside sync. signal (CLKC=L)

1) Outside clock input : EXCL

Parameter	Symbol	min	typ	max	Unit	remarks
Input frequency	FCLI	18.2	18.9	19.6	MHz	SAMC=H
		6.0	6.8	7.6	MHz	SAMC=L
Hi Pulse width	τ_{WH}	20			ns	
Lo Pulse width	τ_{WL}	20			ns	
Rising time	τ_{rCLI}			5	ns	
Falling time	τ_{WH}			5	ns	

2) Horizontal sync. signal (Negative) : HSY

Parameter	Symbol	min	typ	max	Unit	remarks
Input frequency	f_{HI}	$f_{CLI}/1230$	$f_{CLI}/1200$	$f_{CLI}/1170$	kHz	SAMC=H
		$f_{CLI}/465$	$f_{CLI}/435$	$f_{CLI}/405$	kHz	SAMC=L
Pulse width	τ_{HI}	1.0	4.7	4.8	μs	
Rising time	τ_{rHI1}			0.05	μs	
Falling time	τ_{fHI1}			0.05	μs	

3) Vertical sync. signal (Negative) : VSY

Parameter	Symbol	min	typ	max	Unit	remarks
Input frequency	f_{VI}	50	$f_{HI}/262$	$f_{HI}/258$	Hz	
Pulse width	τ_{VI}	1	3	5	H	

4) Input signal timing

Parameter		Symbol	min	typ	max	Unit	remarks
EXCL-HSY	Data setup time	t_{SU1}	25			ns	【Note5】
	Data hold time	t_{HO1}	25			ns	
HSY-VSY	Data setup time	t_{SU2}	1.0			μs	【Note6】
	Data hold time	t_{HO2}	1.0			μs	

【Note5】 In case of outside sync. signal input mode, it show EXCL and HSY timing.
In this case HSY input signal is brought at the rising timing of EXCL input signal.

【Note6】 In case of outside sync. signal input mode, it show HSY and VSY timing.
In this case VSY input signal is brought at the rising timing of HSY input signal.

8. Illustration of control circuit

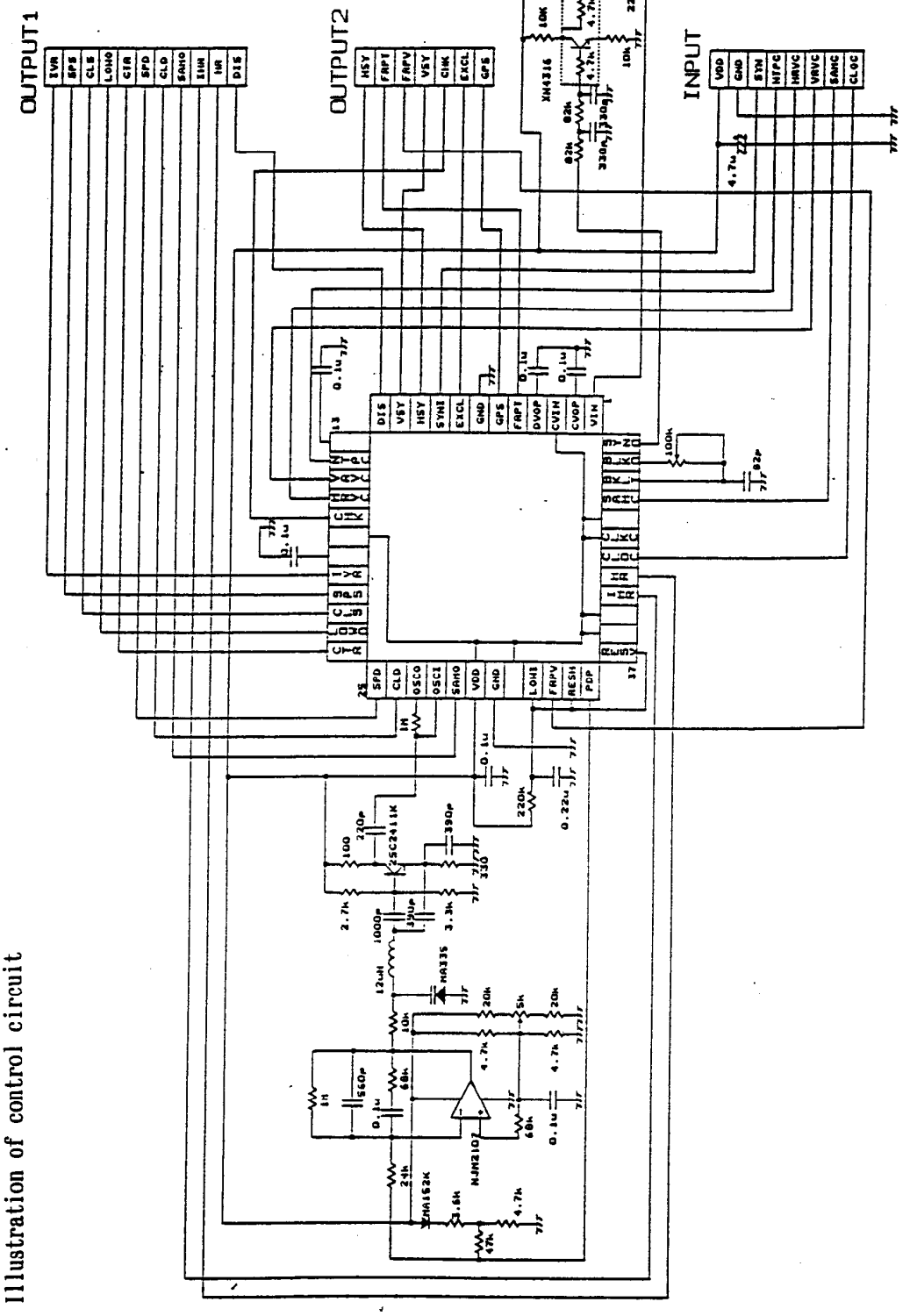


Fig.1-a Illustration of control circuit
In case of using PLL circuit , using separated circuit of vertical sync. signal and CLKC = "H"

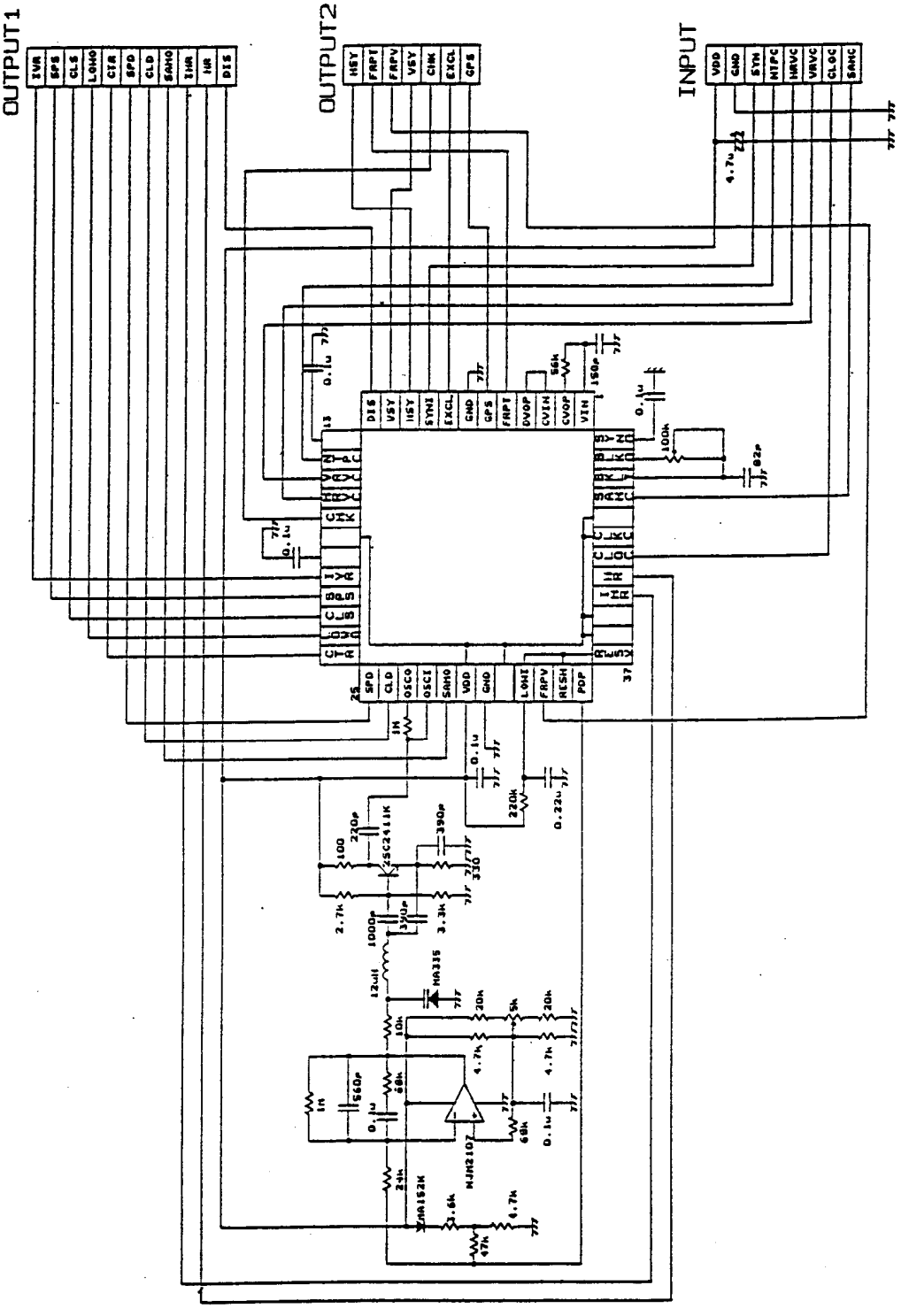


Fig.1-b Illustration of control circuit
In case of using PLL circuit , using output vertical sync. signal of digital separator and CLKC = "H"

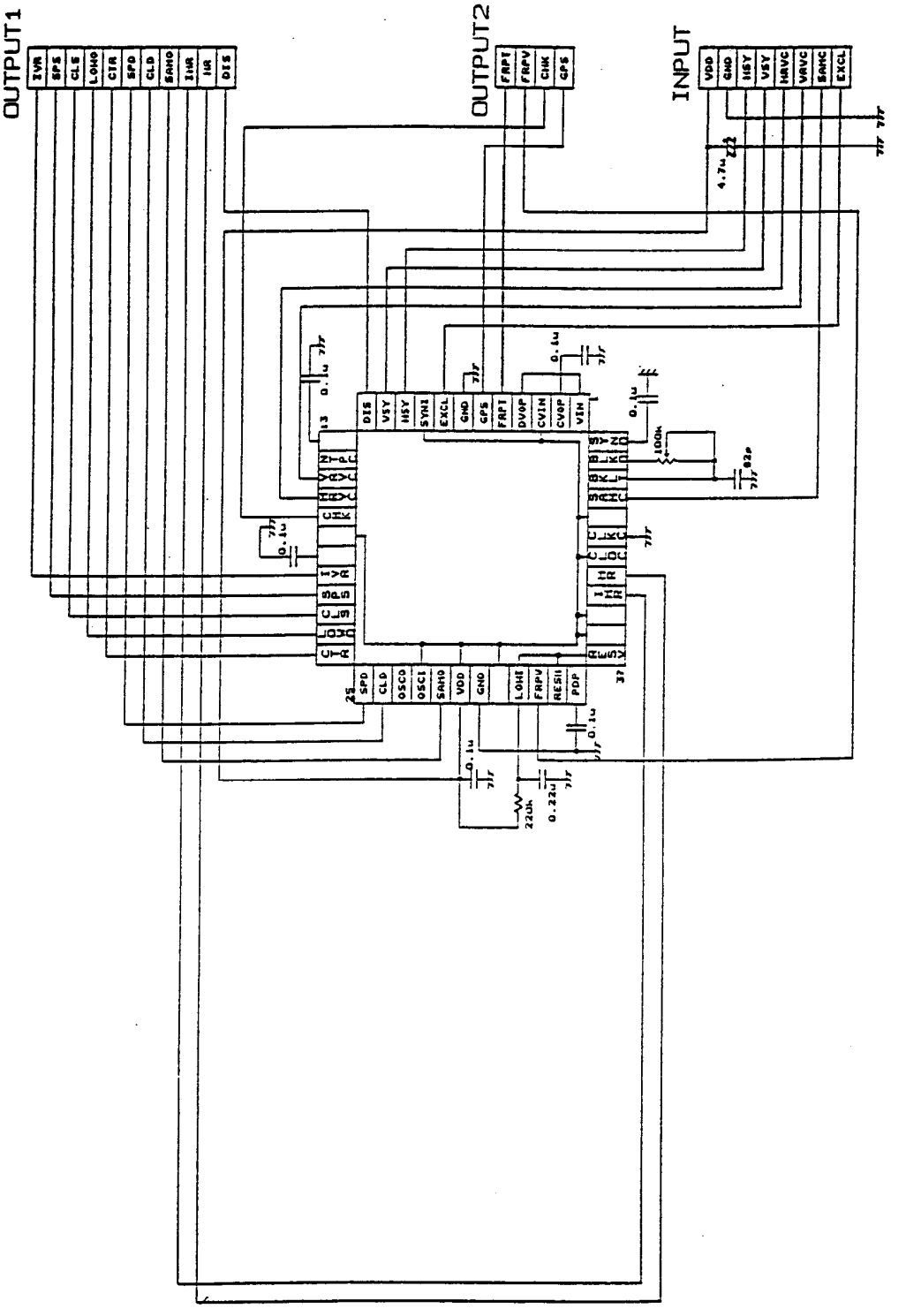


Fig. 1-c Illustration of control circuit
In case of input outside sync. signal and CLKC = "L"

9. Input / Output signal timing chart for above cases

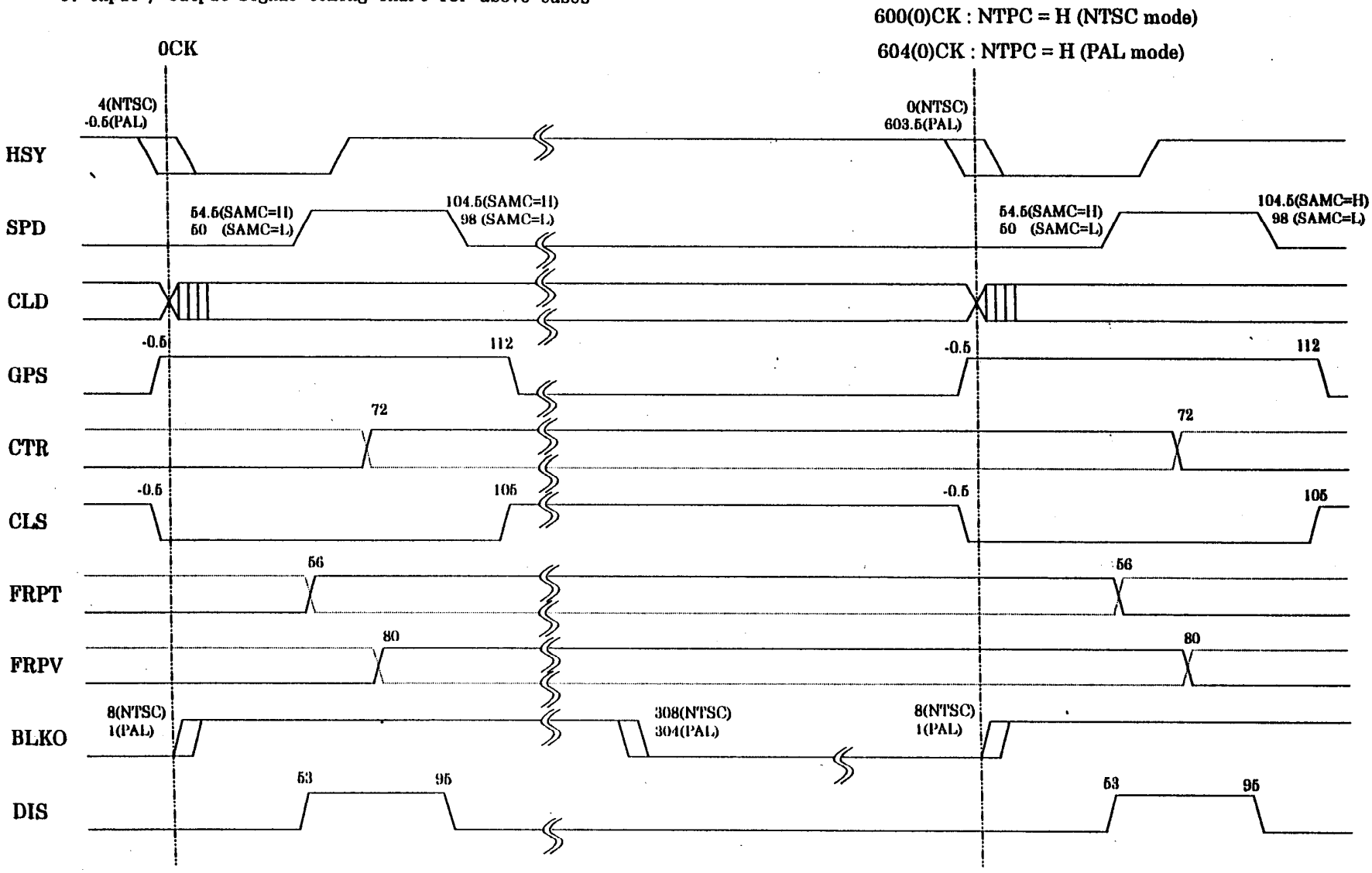


Fig.2-a Horizontal counter timing chart-1 (In case of using PLL circuit)

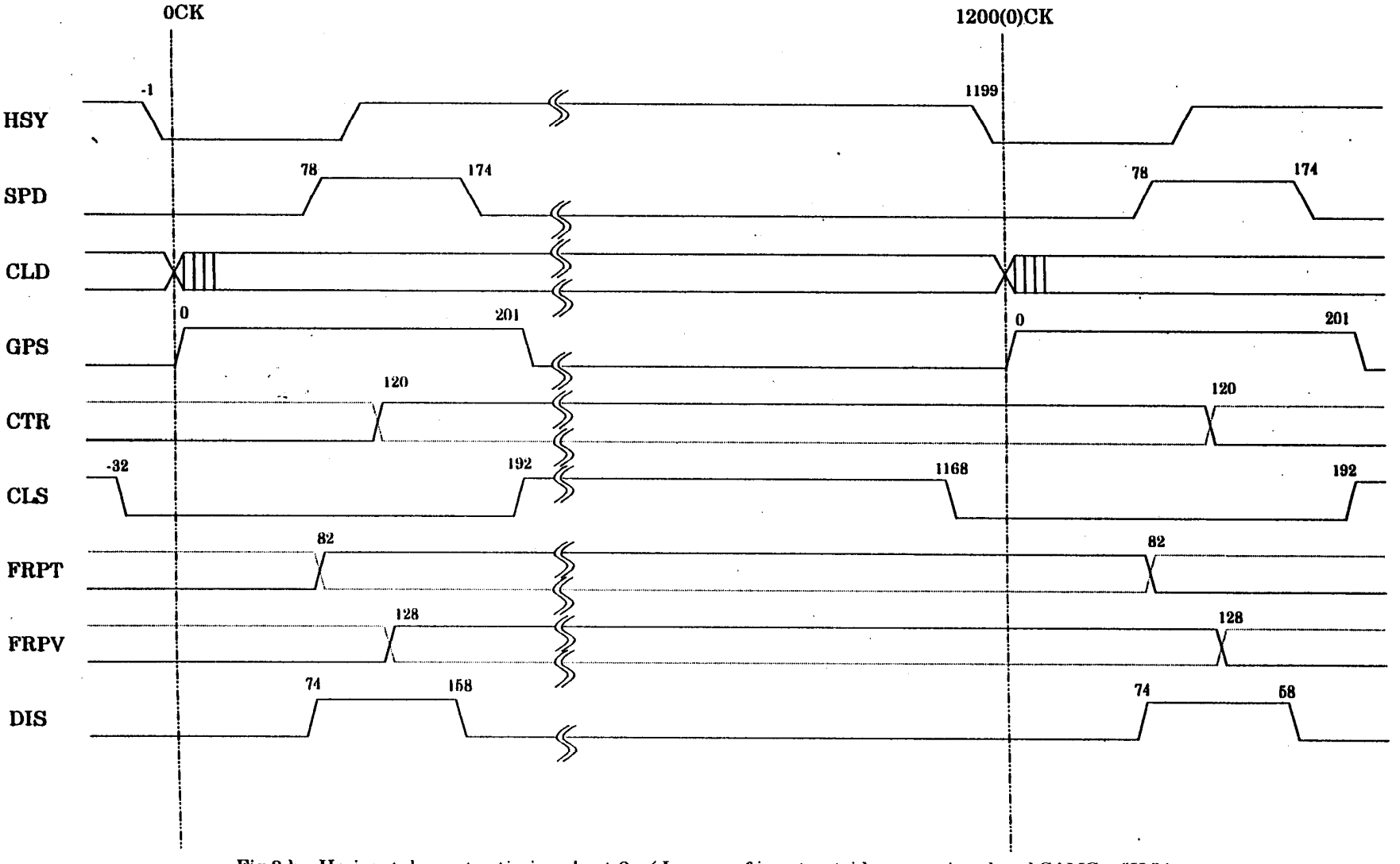


Fig.2-b Horizontal counter timing chart-2 (In case of input outside sync. signal and SAMC = "H ")

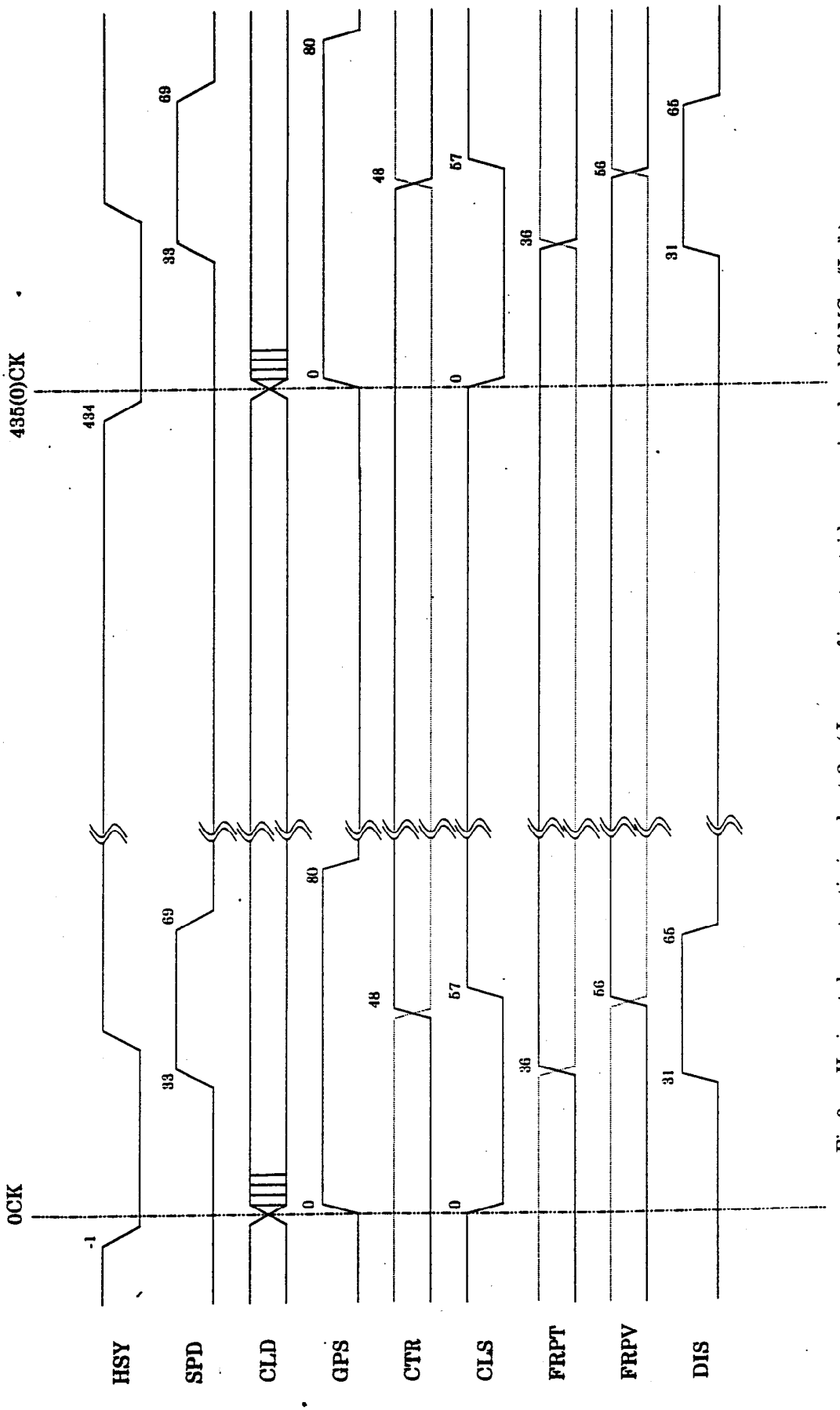


Fig.2-c Horizontal counter timing chart-3 (In case of input outside sync. signal and SAMC = "L ")

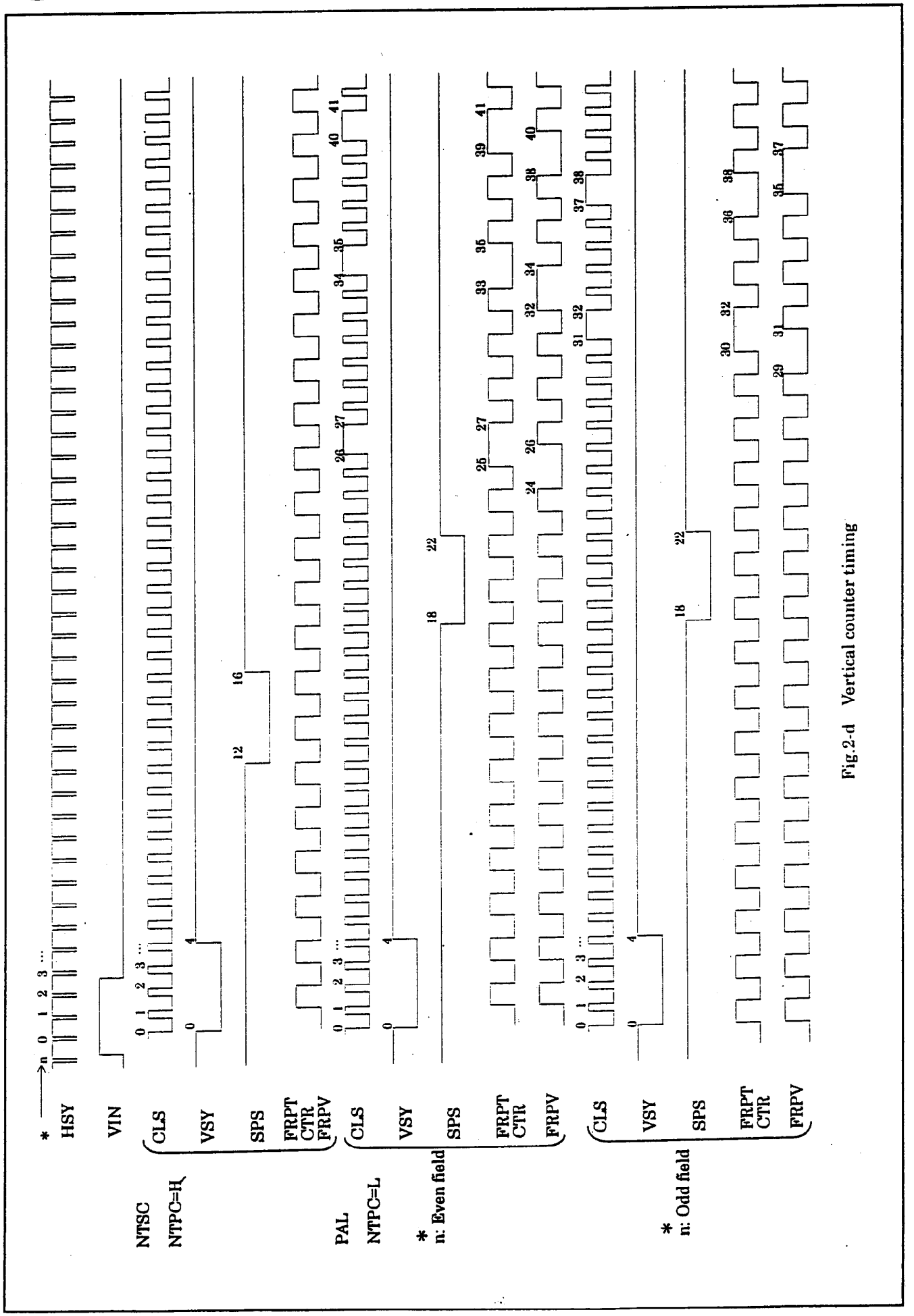


Fig.2-d Vertical counter timing

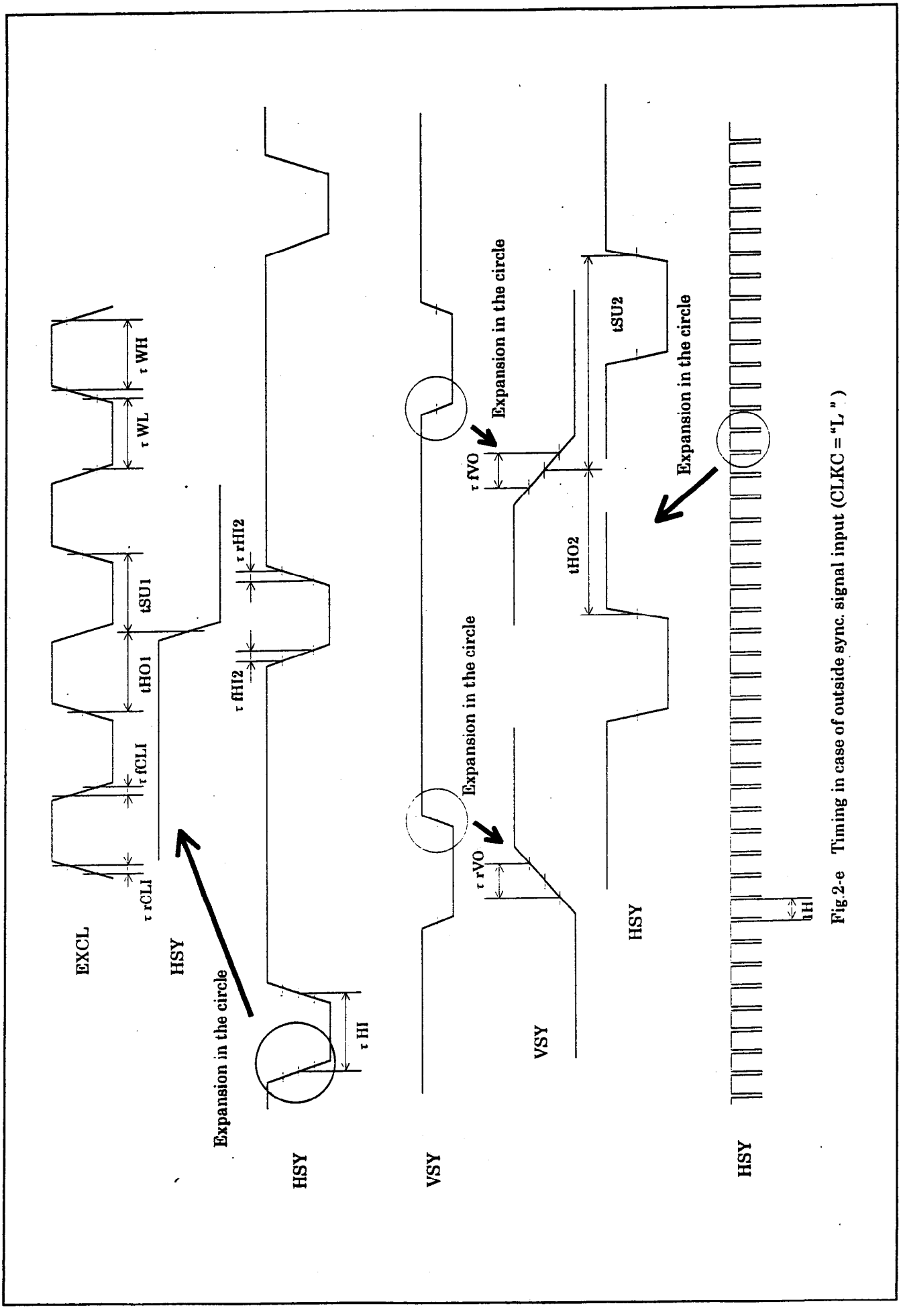


Fig.2-e Timing in case of outside sync. signal input (CLKC = "L")

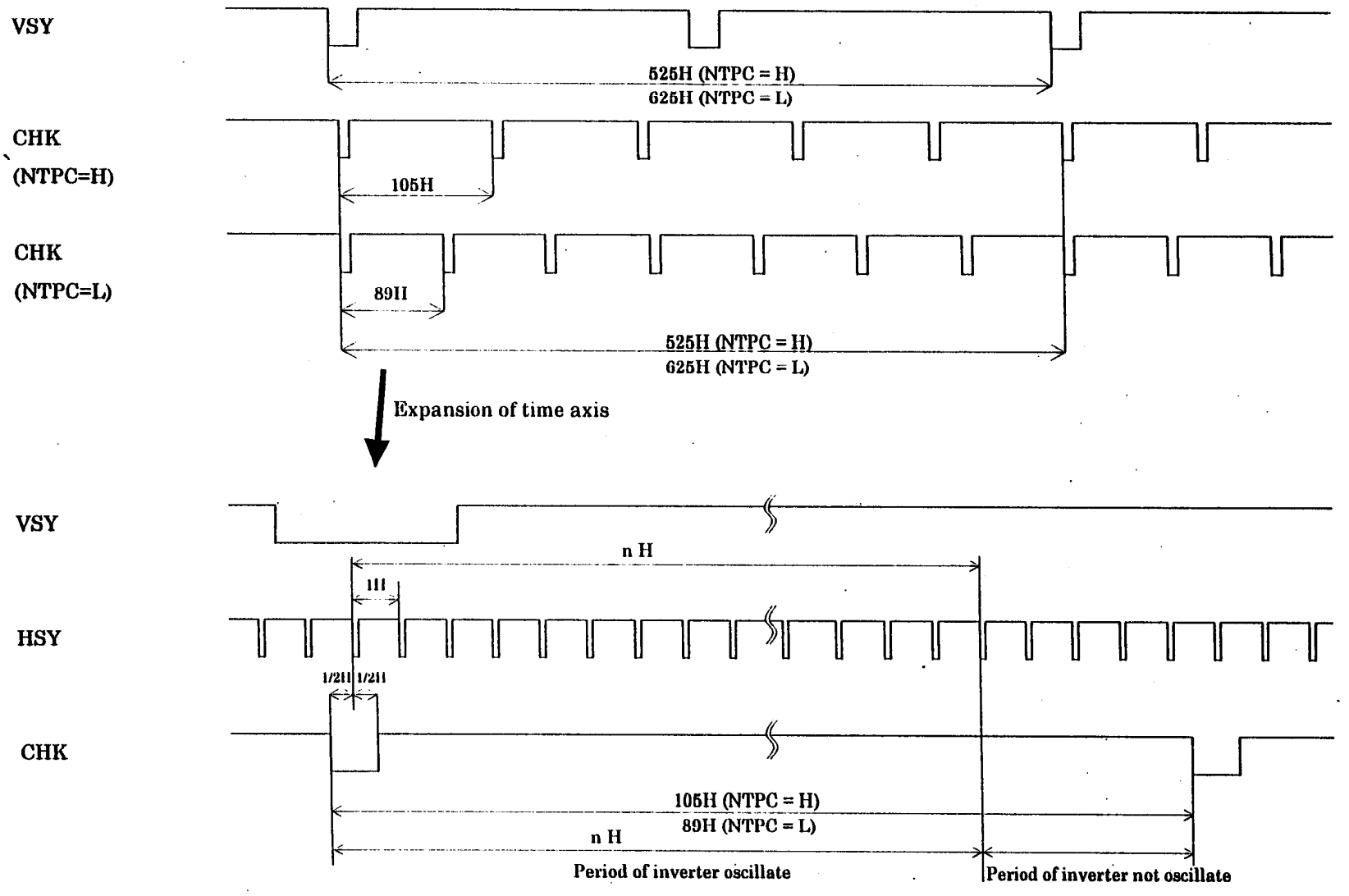


Fig.2-f Output signal timing of CHK (Control signal for the backlight PWM brightness control)

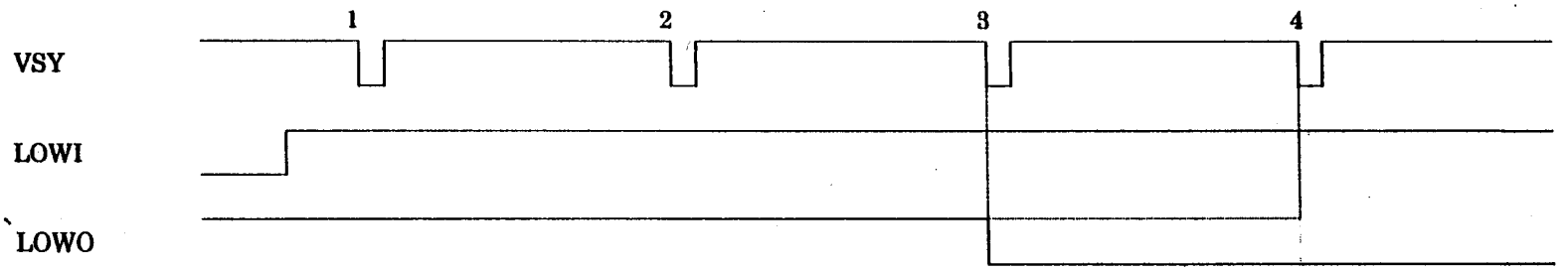


Fig.2-g Output signal timing of LOWO

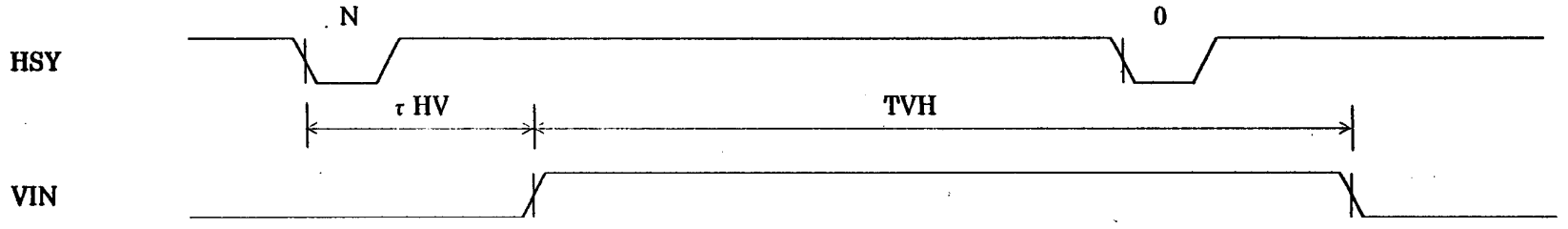


Fig.2-h Input signal timing of VIN (Using separated circuit of vertical sync. signal)

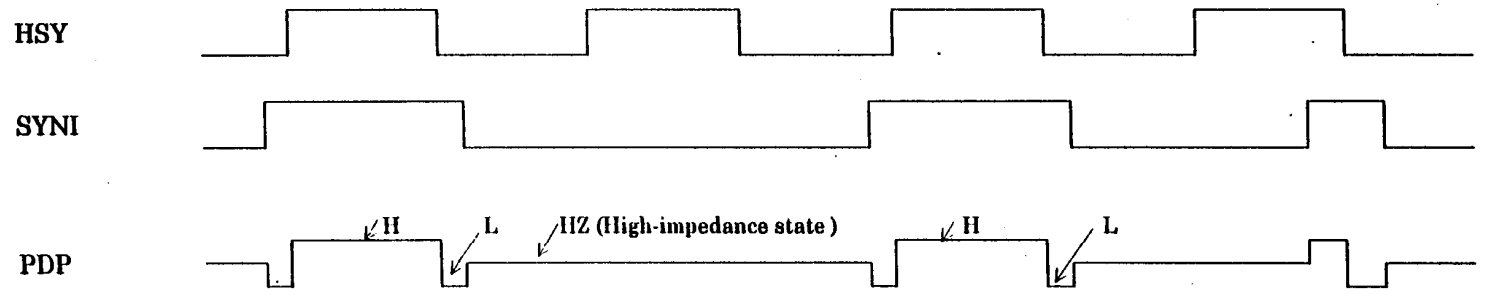


Fig.2-i Output signal timing of PDP

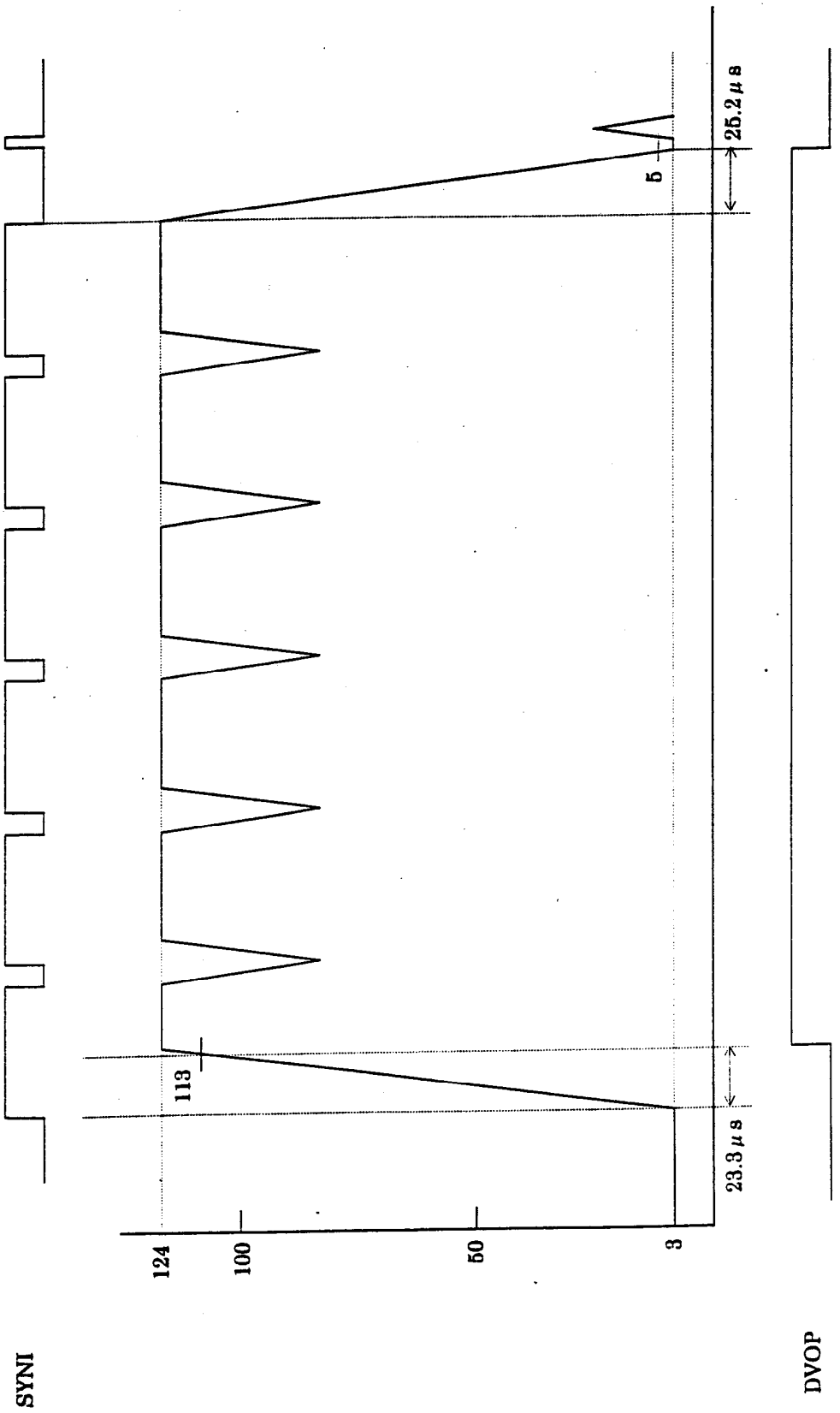
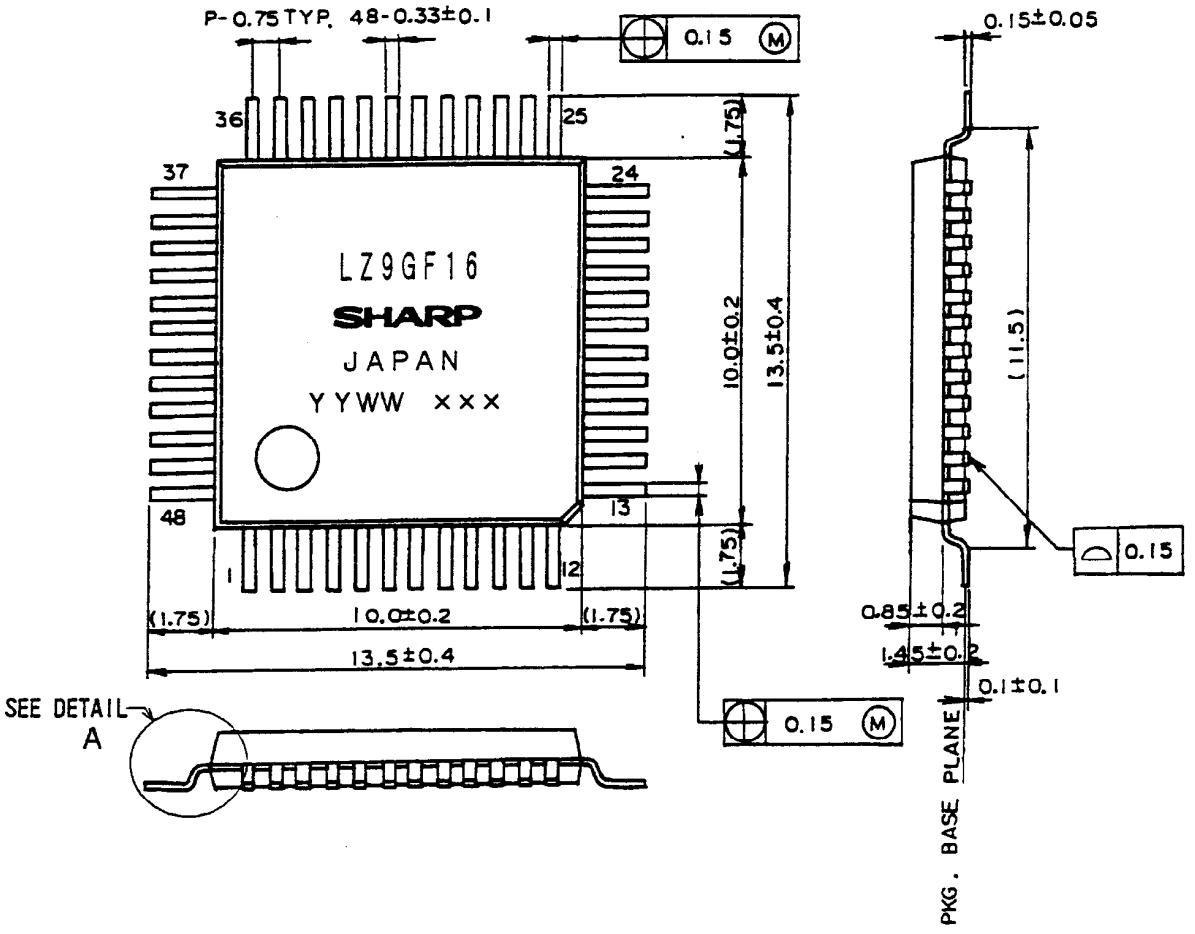
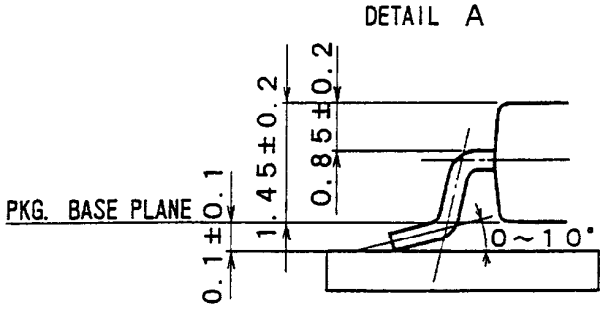


Fig.2-j Output signal timing of DVOP (Output vertical sync. signal of digital separator)

10. Outline dimension





名称 NAME	QFP48-P-1010	リード仕上 LEAD FINISH	TIN-LEAD PLATING
DRAWING NO.	AA873	単位 UNIT	mm

備考 プラスチックパッケージ外形寸法は、バリを含まないものとする。
NOTE Plastic body dimensions do not include burr of resin.