APRIL 1997
Revision 2.1

LXT902

Ethernet Twisted-Pair Media Attachment Unit

General Description

The LXT902 twisted-pair Media Attachment Unit (TP-MAU) is designed to allow Ethernet connections to use the existing twisted-pair wiring plant through an Ethernet Attachment Unit Interface (AUI). The LXT902 provides the electrical interface between the AUI and the twisted-pair wire.

LXT902 functions include level-shifted data pass-through from one transmission media to another, collision detection, Signal Quality Error (SQE) testing and automatic correction of polarity reversal on the twisted-pair input. It also includes LED drivers for transmit, receive, jabber, collision, reversed polarity detect and link functions. The LXT902 is an advanced CMOS device and requires only a single 5-volt power supply.

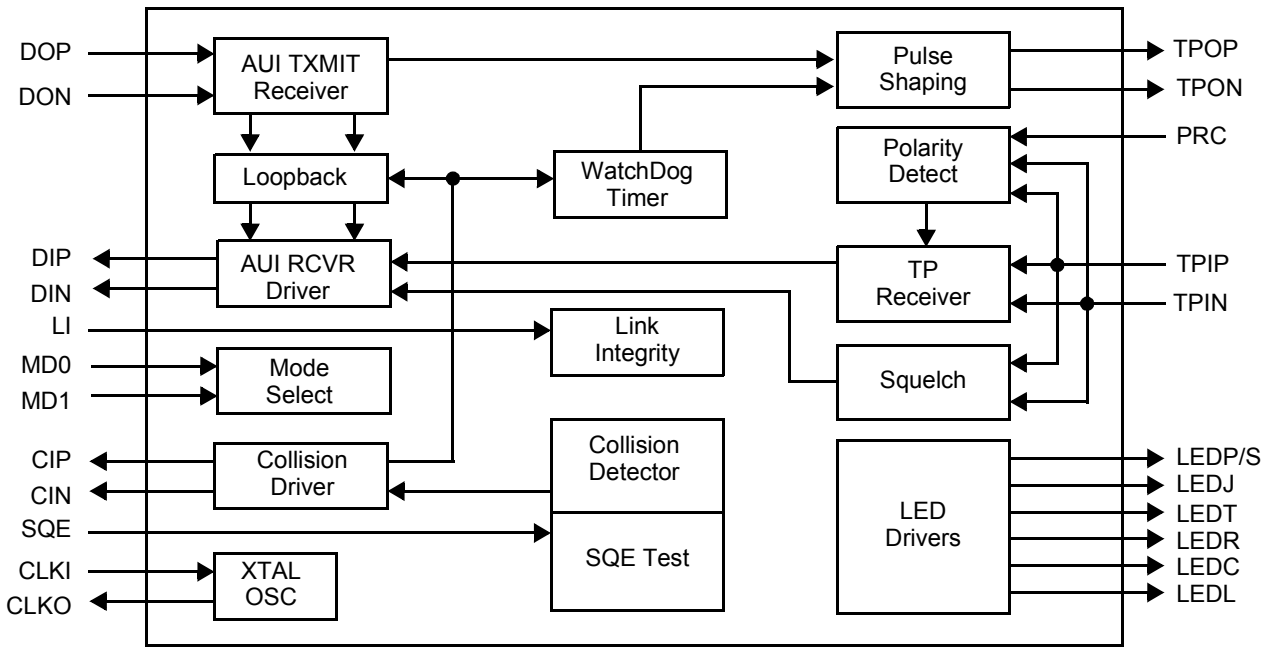
Applications

- Computer/workstation interface boards
- LAN repeater
- External 10BASE-T transceiver (MAU)

Features

- Meets or exceeds IEEE 802.3 standards for AUI and 10BASE-T interface
- Direct interface to AUI and RJ45 connectors
- Automatic AUI/RJ45 selection
- Internal pre-distortion generation
- Internal common mode voltage generation
- Jabber function
- Selectable link test, SQE test disable
- Twisted-pair receive polarity reverse detection and selectable polarity correction
- LED driver for transmit, receive, jabber, collision, link and reversed polarity indicators or for flashing status indicator
- Single 5 V supply, CMOS technology
- Available in 28-pin DIP or PLCC

LXT902 Block Diagram



PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT902 Pin Assignments

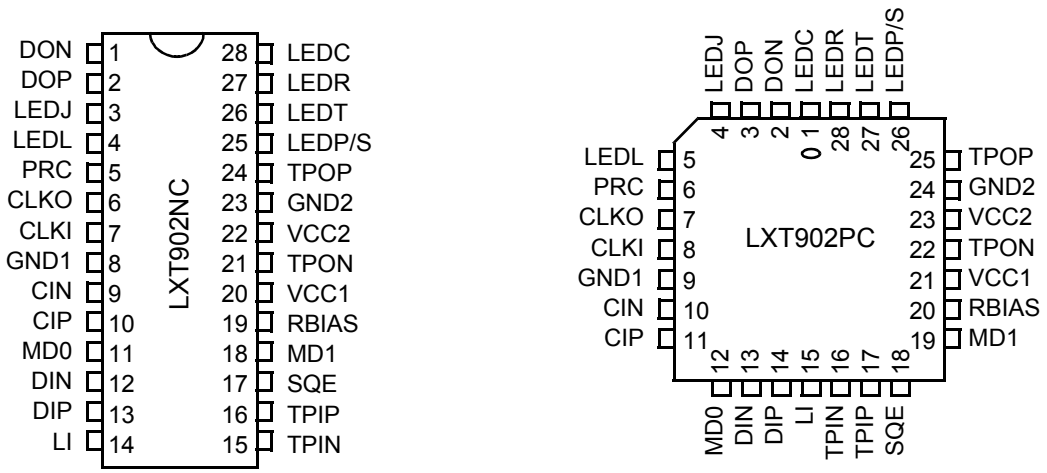


Table 1: LXT902 Signal Descriptions

DIP	PLCC	Symbol	I/O	Description
1 2	2 3	DON DOP	I I	**Data Out Negative and Data Out Positive.** Differential input pair from the AUI transceiver DO circuit.
3	4	LEDJ	I/O	**Jabber LED Driver.** Active Low, open drain driver for the Jabber indicator LED. Output goes active when watchdog timer begins jab, and stays active until end of the unjab wait period (491 - 525 ms). When tied to ground, causes LEDP/S to act as a multi-function blinking status indicator.
4	5	LEDL	O	**Link LED Driver.** Active Low, open drain driver for the Link indicator LED. Output is active except during Link Fail or when Link Integrity Test is disabled.
5	6	PRC	I/O	**Polarity Reverse Correction.** The LXT902 automatically corrects reversed polarity at TPI when PRC is tied High. In Test mode, this pin is a 10 MHz output.
6 7	7 8	CLKO CLKI	O I	**Crystal Oscillator.** The LXT902 requires either a 20 MHz crystal (or ceramic resonator) connected across these pins, or a 20 MHz external clock applied at CLKI with CLKO left unconnected.
8	9	GND1	–	**Ground 1**. Ground
9 10	10 11	CIN CIP	O O	**Collision Negative and Collision Positive.** Differential driver output pair tied to the collision presence pair of the Ethernet transceiver AUI cable. The collision presence signal is a 10 MHz square wave. This output is activated when a collision is detected on the network, during self-test by the SQE sequence, or after the watchdog timer has expired to indicate the transmit wire pair has been disabled.

Table 1: LXT902 Signal Descriptions – continued

DIP	PLCC	Symbol	I/O	Description
11	12	MD0	I	**Mode Select 0.** Selects operating modes in conjunction with MD1. See Table 2 for mode select options.
12 13	13 14	DIN DIP	O O	**Data In Negative and Data In Positive.** Differential driver pair connected to the AUI transceiver DI circuit.
14	15	LI	I	**Link Integrity Test Enable.** Link integrity testing is enabled when this pin is tied High. With link test enabled, the LXT902 sends the link integrity signal in the absence of transmit traffic. It also recognizes received link test pulses, indicating the receive wire pair is present in the absence of transmit traffic.
15 16	16 17	TPIN TPIP	I I	**Twisted-Pair Receive Inputs.** Differential receive inputs from the twisted-pair input filter.
17	18	SQE	I/O	**Signal Quality Error Test Enable.** SQE is enabled when this pin is tied High. When enabled, the LXT902 sends the signal quality error test sequence to the CI of the AUI cable after every successful transmission to the media. In Test mode, SQE becomes a 20 MHz output.
18	19	MD1	I	**Mode Select 1.** Selects operating modes in conjunction with MD0. (See Table 2.) MD1 clock input between 2.0 and 2.5 MHz enables Test mode.
19	20	RBIAS	–	**Resistor Bias Control.** Bias control pin for the operating circuit. Bias set from external resistor to ground. External resistor value = 12.4 kΩ (± 1%).
20	21	VCC1	I	**Power Supply 1.** +5 V power supply.
21 24	22 25	TPON TPOP	O O	**Twisted-Pair Transmit Outputs.** Transmit drivers to the twisted-pair output filter. The output is Manchester encoded and pre-distorted to meet the 10BASE-T template.
22	23	VCC2	I	**Power Supply 2.** +5 V power supply.
23	24	GND2	–	**Ground 2.** Ground.
25	26	LEDP/S	O	**Polarity/Status LED Driver.** Active Low, open drain LED driver. In normal mode, LEDP/S is active when reversed polarity is detected. If LEDJ is tied to ground, LEDP/S indicates multiple status conditions as shown in Figure 11: On solid = Normal, 1 Blink = Link Down, 2 Blinks = Jabber, 5 Blinks = Polarity Reversed.
26	27	LEDT	O	**Transmit LED Driver.** Active Low, open drain driver for the Transmit indicator LED. Output is active during transmit.
27	28	LEDR	O	**Receive LED Driver.** Active Low, open drain driver for the Receive indicator LED. Output is active during receive.
28	1	LEDC	O	**Collision LED Driver.** Active Low, open drain driver for the Collision indicator LED. Output is active when a collision occurs.

FUNCTIONAL DESCRIPTION

Introduction

The LXT902 Media Attachment Unit (MAU) interfaces the Attachment Unit Interface (AUI) to the unshielded twisted-pair cables, transferring data in both directions between the two. The AUI side of the interface comprises three circuits: Data Output (DO), Data Input (DI) and Control Interface (CI). The twisted-pair network side of the interface comprises two circuits: Twisted-Pair Input (TPI) and Twisted-Pair Output (TPO). In addition to these five basic circuits, the LXT902 also contains: crystal oscillator circuitry, separate power and ground pins for analog and digital circuits, mode selection logic (see Table 2) and six LED drivers for status indications.

Table 2: Mode Select Options

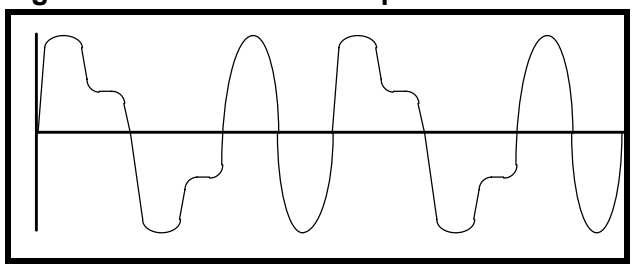
MD1	MD0	Mode
Low	Low	10BASE-T compliant MAU
Low	High	Reduced squelch level
High	Low	Half current AUI driver
High	High	DO, DI & CI ports disabled
High	Clock	Test Mode, Jabber on
Low	Clock	Test mode, Jabber disabled

Functions are defined from the AUI side of the interface. The LXT902 Transmit function refers to data transmitted by the Data Terminal Equipment (DTE) through the AUI and MAU to the twisted-pair network. The LXT902 Receive function refers to data received by the DTE through the MAU and AUI from the twisted-pair network. In addition to basic transmit and receive functions, the LXT902 performs all required functions defined by the IEEE 802.3 10BASE-T MAU specification such as collision detection, link integrity testing, Signal Quality Error (SQE), jabber control and loopback.

Transmit Function

The LXT902 transfers Manchester encoded data from the AUI port of the DTE (the DO circuit) to the twisted-pair network (the TPO circuit). The output signal on TPON and TPOP is pre-distorted to meet the 10 BASE-T jitter template, and filtered to meet FCC requirements. The output waveform (after the transmit filter) is shown in Figure 2. If the differential inputs at the DO circuit fall below 75% of the threshold level for 8 bit times (typical), the LXT902 transmit function will enter the idle state. During idle periods, the LXT902 transmits link integrity test pulses on the TPO circuit.

Figure 2: LXT902 TPO Output Waveform



Receive Function

The LXT902 receive function transfers serial data from the twisted-pair network (the TPI circuit) to the DTE (over the DI circuit of the AUI). An internal squelch function discriminates noise from link test pulses and valid data streams. Only valid data streams activate the receive function. If the differential inputs at the TPI circuit fall below 75% of the threshold level (unsquelched) for 8 bit times (typical), the LXT902 receive function will enter the idle state. The TPI threshold can be reduced by approximately 3 dB to allow for longer loops in low-noise environments. The reduced threshold is selected when MD1 = Low and MD0 = High.

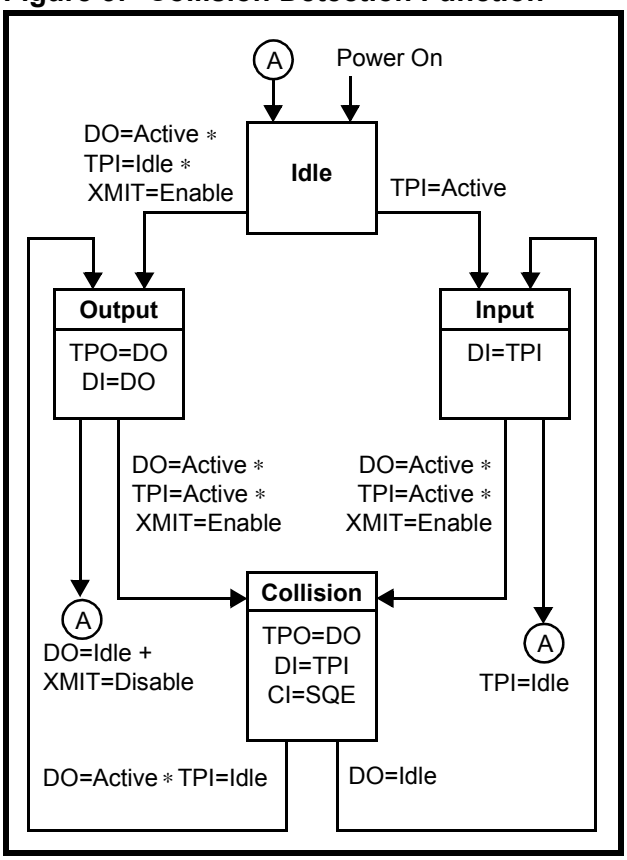
Polarity Reverse Function

The LXT902 polarity reverse function uses both link pulses and end-of-frame data to determine polarity of the received signal. A reversed polarity condition is detected when eight opposite receive link pulses are detected without receipt of a link pulse with the expected polarity. Reversed polarity is also detected if four frames are received with a reversed start-of-idle. Whenever polarity is reversed, these two counters are reset to zero. If the LXT902 enters the link fail state, and no data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. If Link Integrity is disabled, polarity detection is based only on received data pulses.

Collision Detection Function

The collision detection function operates on the twisted-pair side of the interface. A collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The LXT902 reports collisions to the AUI by sending a 10 MHz signal over the CI circuit. The collision report signal is output no more than 9 bit times (BT) after the chip detects a collision. If the TPI circuit becomes active while there is activity on the TPO circuit, the TPI data is passed to the DTE over the DI circuit, disabling the loopback. Figure 3 is a state diagram of the LXT902 collision detection function (refer to IEEE 802.3 10BASE-T specification).

Figure 3: Collision Detection Function



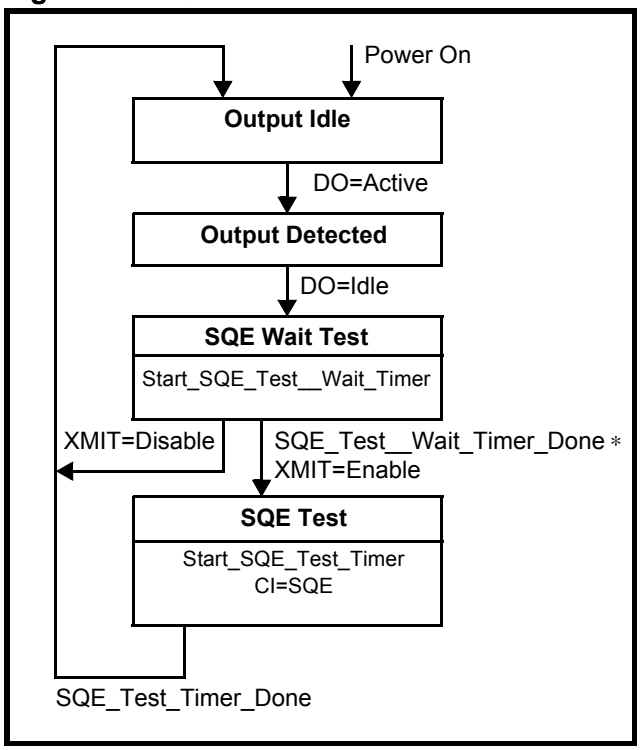
Loopback Function

The LXT902 loopback function operates in conjunction with the transmit function. Data transmitted by the DTE is internally looped back within the LXT902 from the DO pins to the DI pins and returned to the DTE. The loopback function is disabled when a data collision occurs, clearing the DI circuit for the TPI data. Loopback is also disabled during link fail and jabber states.

SQE Test Function

Figure 4 is a state diagram of the SQE Test function. The SQE test function is enabled when the SQE pin is tied High. When enabled, the SQE test sequence is transmitted to the controller after every successful transmission on the 10BASE-T network. When a successful transmission is completed, the LXT902 transmits the SQE signal to the AUI over the CI circuit for 10 BT ± 5 BT. The SQE function can be disabled for hub applications by tying the SQE pin to ground.

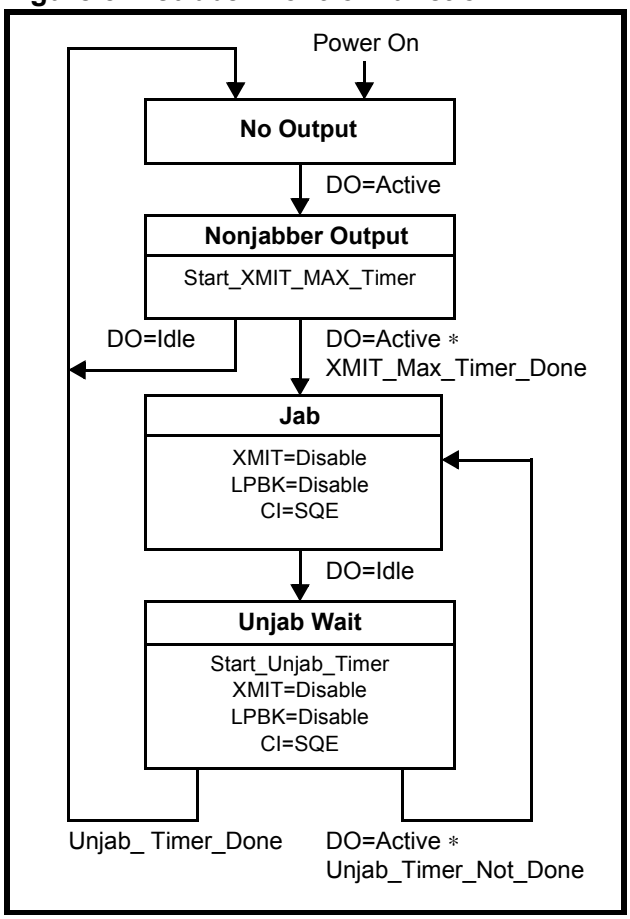
Figure 4: SQE Function



Jabber Control Function

Figure 5 is a state diagram of the LXT902 Jabber control function. The LXT902 on-chip watchdog timer prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the Watchdog timer disables the transmit and loopback functions, and sends the SQE signal to the DTE over the CI circuit. Once the LXT902 is in the jabber state, the DO circuit must remain idle for a period of 491 to 525 ms before it will exit the jabber state.

Figure 5: Jabber Control Function



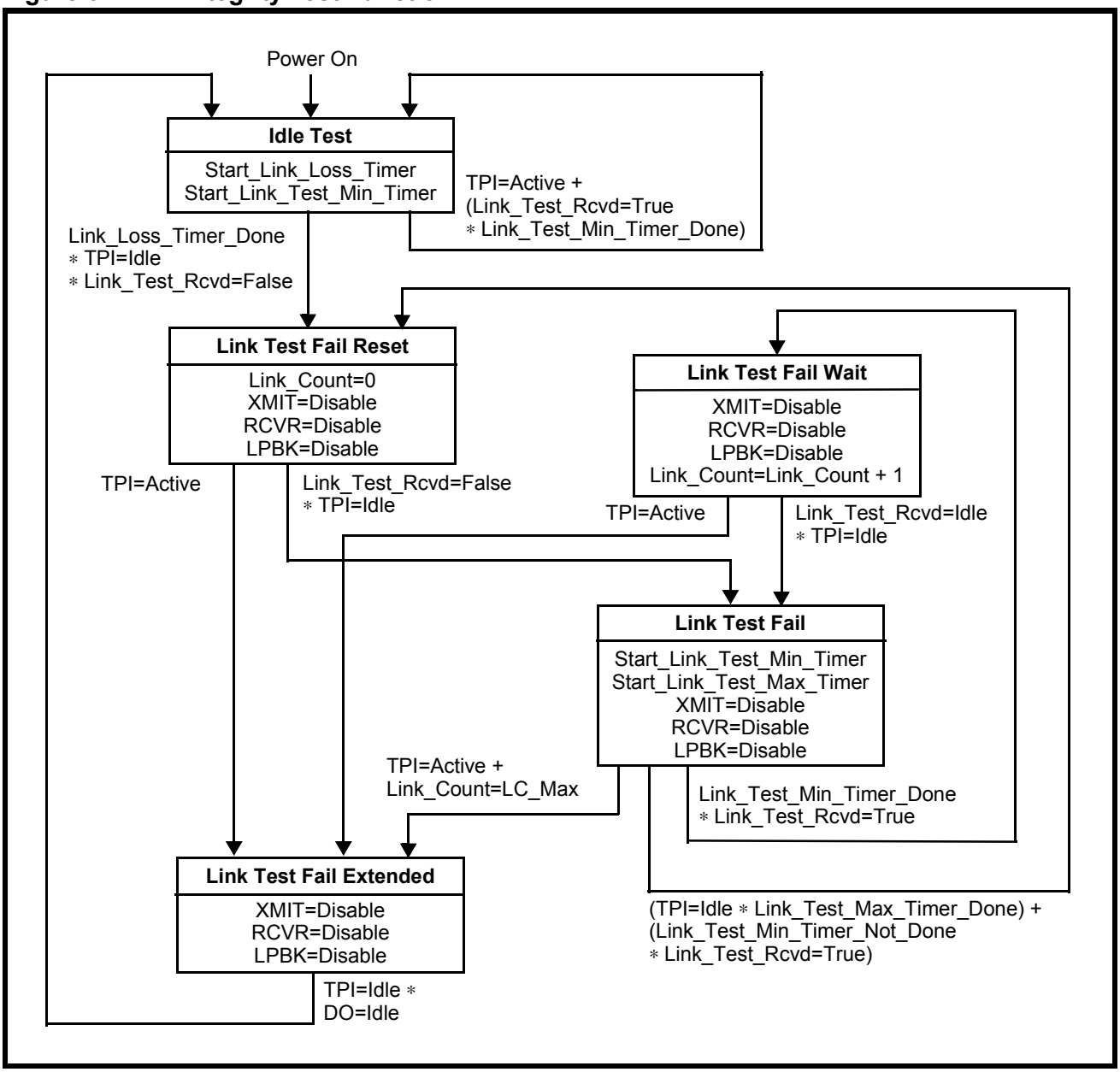
Link Integrity Test Function

Figure 6 is a state diagram of the LXT902 Link Integrity Test Function. The Link Integrity Test is used to determine the status of the receive side twisted-pair cable. The link integrity test is enabled when the LI pin is tied High. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50 - 150 ms, the chip enters a link fail state and disables the transmit and loopback functions. The LXT902 ignores any link integrity pulse with interval less than 2 - 7 ms. The LXT902 will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses.

Test Mode

The LXT902 Test mode is selected when a 2 - 2.5 MHz clock is input on the MD0 mode select pin. Test mode sets the internal counter chains to run at 1024 times their normal speed. The maximum transmit time, unjab time, Link Integrity timing and LED timing are reduced by a factor of 1024. During test operation, 10 MHz and 20 MHz signals are output on the PRC and SQE pins, respectively. When Test mode is selected, the SQE function cannot be disabled. In Test mode the PRC function can be disabled by the LI pin. Jabber can be disabled by setting MD1 Low.

Figure 6: Link Integrity Test Function



APPLICATION INFORMATION

External MAU

Figure 7 shows the LXT902 in a typical external MAU application, interfacing between an AUI and the RJ45 connectors of the twisted-pair network. A 20 MHz crystal (or ceramic resonator) connected across CLKI and CLKO provides the required clock signal. Transmit and receive filters are required in the TPO and TPI circuits. Details of the transmit and receive filters are shown in Figures 8 and 9, respectively. (Differential filters are also recommended.)

Internal MAU

Figure 10 shows an internal MAU application which takes advantage of the LXT902's unique AUI/10BASE-T switching feature to select either the D-connector (AUI) or the RJ45 connector (10BASE-T). No termination resistors are used on the LXT902 side of the AUI interface to prevent impedance mismatch with the drop cable. The half current drive mode is used to maintain the same voltage levels in the absence of termination resistors. This application uses capacitive coupling instead of transformer coupling. MD1 is tied High so MD0 functions as the mode control switch.

When MD0 is Low, the half current drive mode is selected. When MD0 is High, the LXT902 is effectively removed from the circuit. The 902 AUI ports (DO, DI and CI) are disabled isolating the LXT902 from the AUI. The LXT902 DI and CI ports go to a high impedance state and the DO port is ignored. To implement an auto-select function, LEDL can be tied to MD0. This activates the 902/AUI interface when the TP link is active (data or link integrity pulses) and disables it when the link is inactive.

Figure 7: Typical External MAU Application

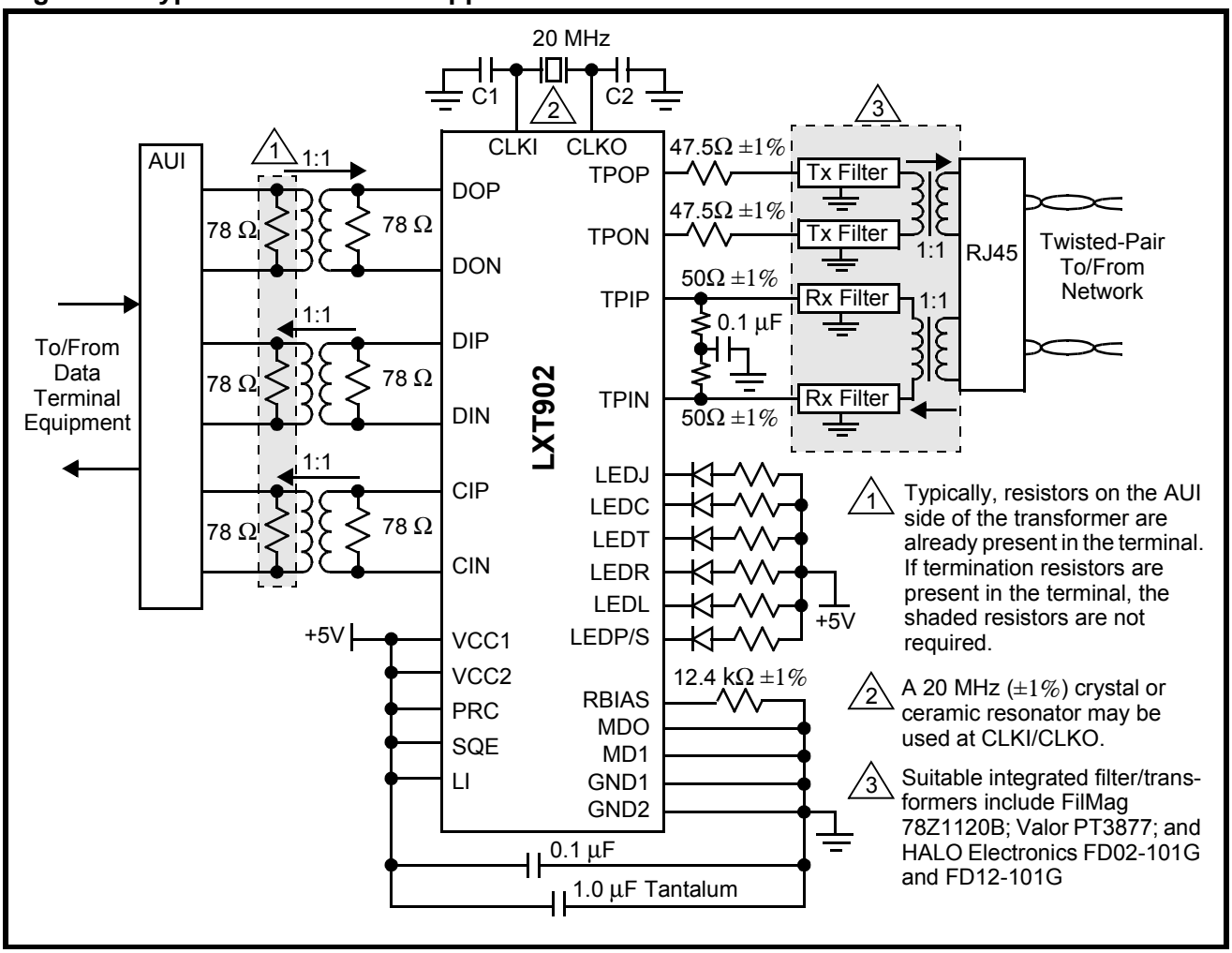


Figure 8: Typical Transmit Filter

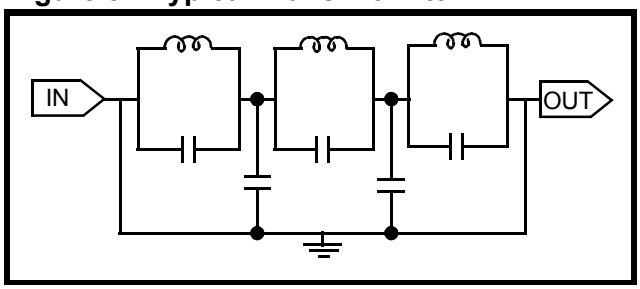


Figure 9: Typical Receive Filter

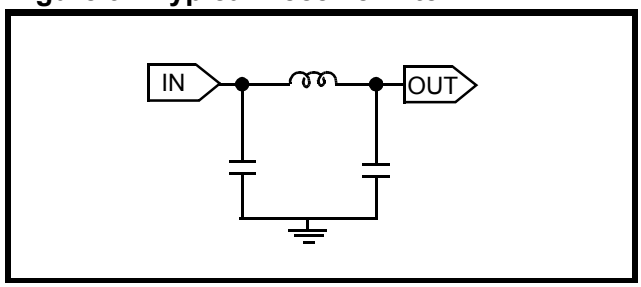
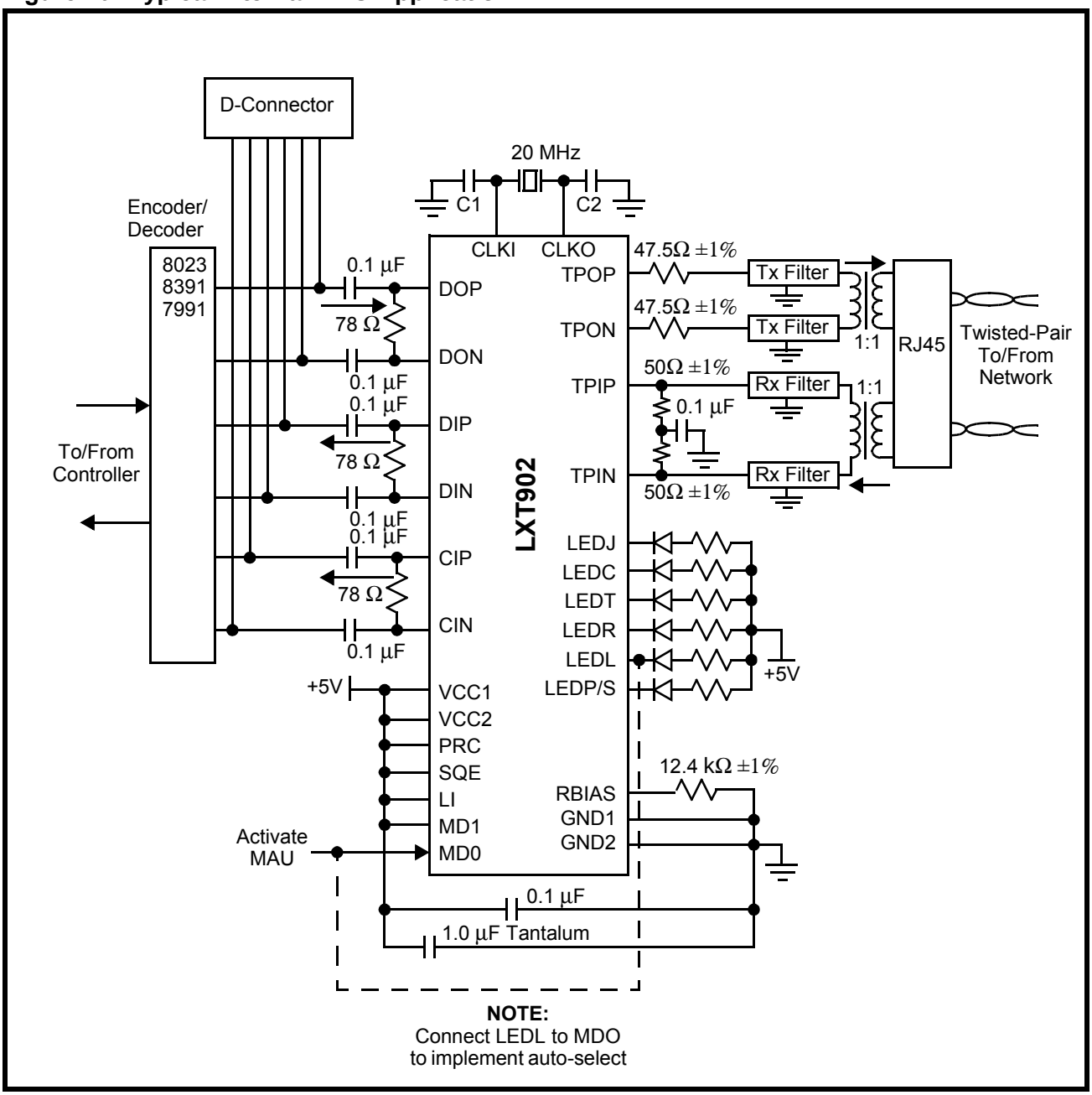


Figure 10: Typical Internal MAU Application



TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 3 through 9 and Figure 11 represent the performance specifications of the LXT902 and are guaranteed by test, except where noted by design.

Table 3: Absolute Maximum Values

Parameter	Symbol	Min	Max	Units
Supply voltage	V_{CC}	-0.3	6	V
Ambient operating temperature	T_A	0	70	ºC
Storage temperature	T_{STG}	-65	+150	ºC

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Recommended supply voltage[1, 2]	V_{CC}	4.75	5.0	5.25	V	–
Recommended operating temperature	T_{OP}	0	–	70	ºC	–

2. Voltages with respect to ground unless otherwise specified.
3. Maximum voltage differential between VCC1 and VCC2 must not exceed 0.3 V.

Table 5: I/O Electrical Characteristics (Over Recommended Range)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage[2]	V_{IL}	–	–	0.8	V	–
Input High voltage[2]	V_{IH}	2.0	–	–	V	–
Output Low voltage (Open drain LED driver)	V_{OLL}	–	–	0.7	V	I_{OLL} = 10 mA
Supply Current ($V_{CC}1=V_{CC}2=5.25$ V)	I_{CC}	–	60	70	mA	Line Idle
		–	125	140	mA	Line Active, transmitting all ones
Input Leakage Current[3]	I_{LL}	–	±1	±10	µA	Input between V_{CC} and GND
Three state leakage current (high Z)	I_{TS}	–	±1	±10	µA	Output between V_{CC} and GND

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. MD0, MD1, SQE, PRC, and LI pins. MD0 clock (test mode) must be CMOS level input.
3. Not including TPIN, TPIP, DOP, or DON.

Table 6: AUI Electrical Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Input Low current	I_{IL}	–	–	-700	µA	–
Input High current	I_{IH}	–	–	500	µA	–
Differential output voltage	V_{OD}	±550	–	±1200	mV	–
Differential squelch threshold	V_{DS}	–	220	–	mV	–
Receive input impedance	RZ	–	20	–	kΩ	Between DOP and DON

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 7: Transmit Characteristics (Over Recommended Range)

Parameter	Sym	Minimum	Typical[1]	Maximum	Units	Test Conditions
Transmit output impedance	Z_{OUT}	–	5	–	Ω	–
Transmit timing jitter addition[2]	–	–	–	±8	ns	After Tx filter, 0 line length
Transmit timing jitter addition[2]	–	–	–	±3.5	ns	After Tx filter and line model specified by IEEE 802.3 for 10BASE-T

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.

Table 8: Receive Characteristics (Over Recommended Range)

Parameter	Sym	Minimum	Typical[1]	Maximum	Units	Test Conditions
Receive input impedance	Z_{IN}	–	20	–	kΩ	Between TPIP/TPIN
Differential squelch threshold	V_{DS}	–	420	–	mV	–
Reduced squelch threshold	V_{DSR}	–	300	–	mV	–
Receive timing jitter addition[2]	–	–	–	1.5	ns	–

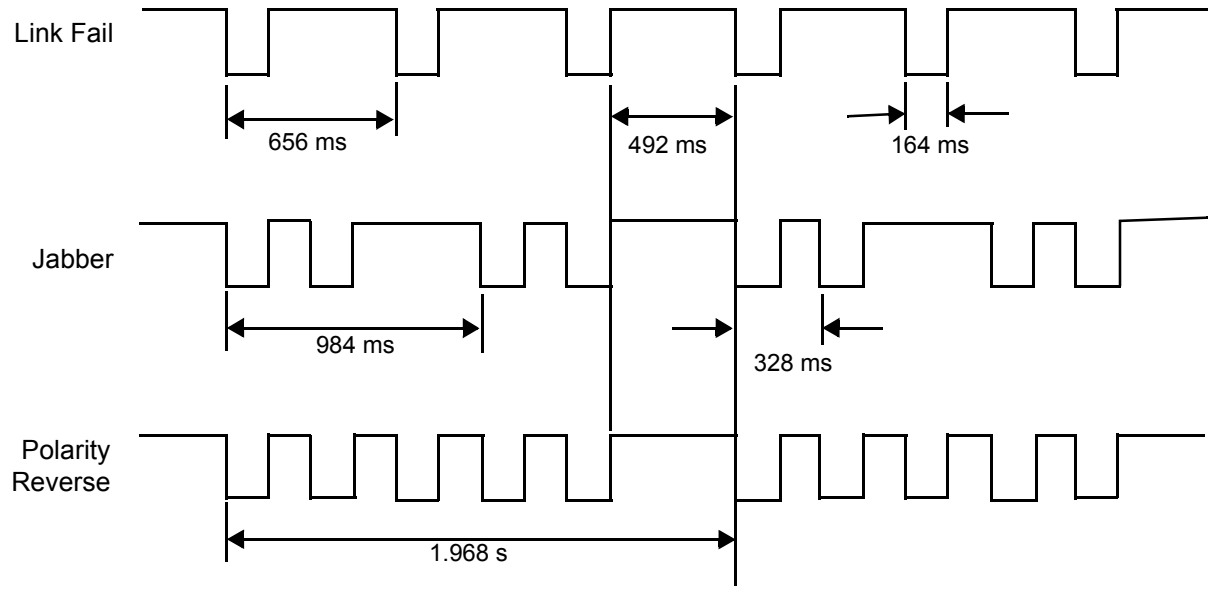
1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.

Table 9: Switching Characteristics (Over Recommended Range)

	Parameter	Min	Typ[1]	Max	Units
Jabber Timing	Maximum transmit time [2]	98.5	–	131	ms
	Unjab time [2]	491	–	525	ms
	Time from Jabber to CS0 on CIP/CIN [3]	0	–	900	ns
Link Integrity Timing	Time link loss [2]	65	–	66	ms
	Time between Link Integrity Pulses [2]	9	–	11	ms
	Interval for valid receive Link Integrity Pulses [2]	4.1	–	65	ms
Collision Timing	Simultaneous TPI/TPO to CSO state on CIN/CIP	0	–	900	ns
	DO loopback to TPI on DI [3]	300	–	900	ns
	CS0 state delay after TPI/DO idle	–	–	900	ns
	CS0 High pulse width	40	–	60	ns
	CS0 Low pulse width	40	–	60	ns
	CS0 frequency	–	10	–	MHz
SQE Timing	SQE signal duration	500	–	1500	ns
	Delay after last positive transition of DO	0.6	–	1.6	µs
LED Timing	LEDC, LEDT, LEDR on time [2]	100	–	–	ms
	LEDP/S on time [2] (See Figure 11)	–	164	–	ms
	LEDP/S period [2] (See Figure 11)	–	328	–	ms
General	Receive start-up delay	0	–	500	ns
	Transmit start-up delay	0	–	200	ns
	Loopback start-up delay	0	–	500	ns

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Switching times reduced by a factor of 1024 during Test mode.
3. Parameter is guaranteed by design; not subject to production testing.

Figure 11: LEDP/S Status Indication Timing



NOTE:

1. LEDP/S status indications are shown in order of priority, i.e., Link Fail indication supersedes Jabber indication which supersedes Polarity Reverse (when PRC = 1). Reversed polarity conditions supersede Link Fail conditions when PRC = 0 (Polarity Correction Disabled). At the LEDL indicator, reversed polarity conditions are reported as Link Fail when PRC = 0. This allows the user to distinguish between actual link failure and apparent link failure due to polarity reversal.

NOTES