



530 MHz PLL Frequency Synthesizer LSI



Overview

The LV2105V is a PLL frequency synthesizer Bi-CMOS LSI that provides low-voltage operation and low current drain, and that is suitable for use in a variety of radio equipment.

Functions

- PLL function
- Data input by serial transfer (CCB format)
- Input amplifier for crystal oscillation circuit
- Data output port

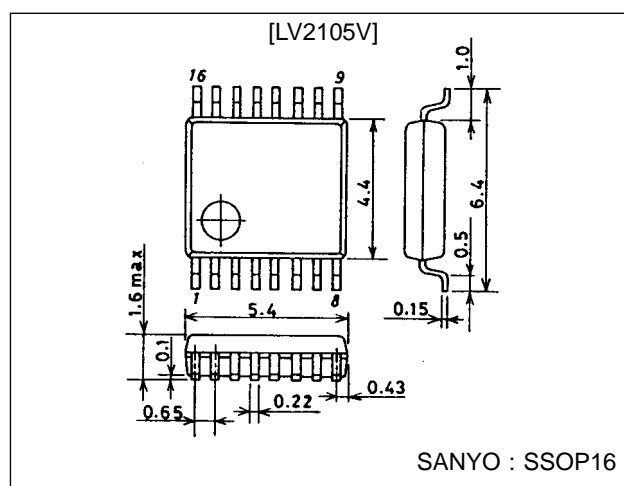
Features

- Low operating voltage: ($V_{CC} = 2.5$ to 5.5 V)
- Low current drain (5.5 mA)
- Compact package (SSOP16, 0.65 mm pitch)
- VCO band switching data output port on chip
- Data can be input while in power saving mode
- Data input pin high level can be input at V_{CC} or higher
- Independent setting of CP ON/OFF (high impedance) possible

Package Dimensions

unit: mm

3178-SSOP16



- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

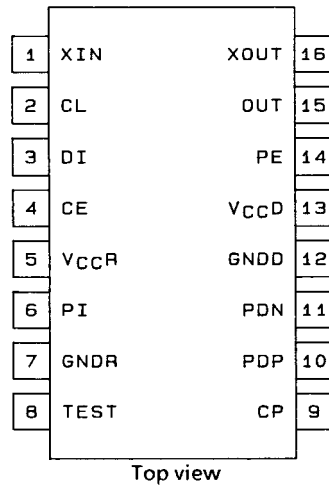
Specifications

Absolute Maximum Ratings at $T_a = 25$ °C

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|------------------|--|----------------------|------|
| Maximum supply voltage | V_{CC} max | V_{CCR} , V_{CCD} | -0.3 to +6.0 | V |
| Maximum input voltage | V_{IN} max(1) | CE, CL, DI | -0.3 to +6.0 | V |
| | V_{IN} max(2) | XIN, TEST | -0.3 to $V_{CC}+0.3$ | V |
| Maximum output voltage | V_{OUT} max(1) | PDP | -0.3 to +9.0 | V |
| | V_{OUT} max(2) | PDN, OUT, PE | -0.3 to $V_{CC}+0.3$ | V |
| Maximum output current | I_{OUT} max | PDP | 0 to +1.0 | mA |
| Allowable power dissipation | P_d max | $114 \times 76 \times 1.6$ mm ³ When using glass epoxy board | 230 | mW |
| Operating temperature | T_{opr} | | -40 to +85 | °C |
| Storage temperature | T_{stg} | | -50 to +125 | °C |

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Pin Assignment



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Allowable Operating Ranges at $T_a = -40$ to $+85$ °C

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-------------------------------|-------------|------------------------------------|----------------------|-----|------|------|
| Supply voltage | V_{CC} | V_{CCR}, V_{CCD} | 2.5 | | 5.5 | V |
| High-level input voltage | V_{IH} | CE, CL, DI | $V_{CCR} \times 0.7$ | | 5.5 | V |
| Low-level input voltage | V_{IL} | CE, CL, DI | 0 | | +0.6 | V |
| Output voltage | V_{OUT} | PDP | 0 | | +7.0 | V |
| Input frequency | $f_{IN(1)}$ | XIN: Sine wave capacitive coupling | 5 | | 22 | MHz |
| | $f_{IN(2)}$ | PI: Sine wave capacitive coupling | 100 | | 530 | MHz |
| Input amplitude | $V_{IN(1)}$ | XIN: Sine wave capacitive coupling | -12 | | +10 | dBm |
| | $V_{IN(2)}$ | PI: Sine wave capacitive coupling | -18 | | 0 | dBm |
| Crystal oscillation condition | Xtal | XIN, (XOUT) | 5 | | 13 | MHz |

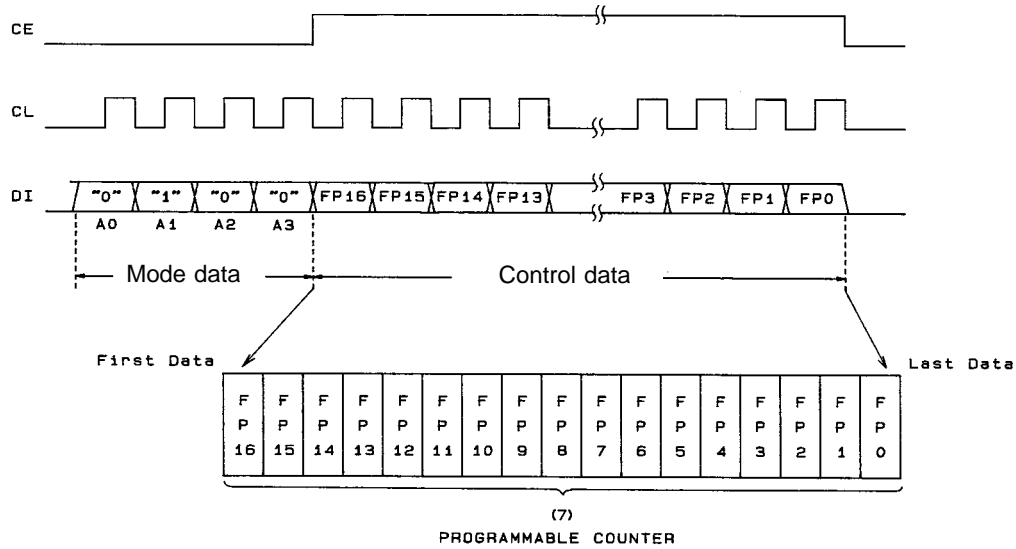
Electrical Characteristics at $T_a = 25$ °C, $V_{CCR} = 3.0$ V, $V_{CCD} = 3.0$ V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|------------------------------|--------------|---------------------------|----------------|-----------|----------|------------|
| Low-level output voltage | $V_{OL(1)}$ | PDP: $I_O = 0.5$ mA | | | 0.5 | V |
| | $V_{OL(2)}$ | PDN: $I_O = 0.5$ mA | | | 0.5 | V |
| | $V_{OL(3)}$ | PE: $I_O = 0.5$ mA | | | 0.5 | V |
| | $V_{OL(4)}$ | OUT: $I_O = 2.0$ mA | | | 0.5 | V |
| High-level output voltage | $V_{OH(1)}$ | PE: $I_O = -0.5$ mA | $V_{CC} - 0.5$ | | | V |
| | $V_{OH(2)}$ | PDN: $I_O = -0.5$ mA | $V_{CC} - 0.5$ | | | V |
| Output off leak current | $I_{OFF(1)}$ | PDP: $V_O = 3.0$ V | | | 1.0 | μ A |
| | $I_{OFF(2)}$ | CP: $V_O = 1.5$ V | | | 100 | nA |
| C.P output current | I_{CP} | CP: $V_O = 1.5$ V | ± 4.0 | ± 7.5 | ± 11 | mA |
| High-level input current | $I_{H(1)}$ | CE, CL, DI: $V_I = 3.0$ V | | | 5.0 | μ A |
| | $I_{H(2)}$ | XIN: $V_I = 3.0$ V | 2.3 | 3.0 | 4.3 | μ A |
| | $I_{H(3)}$ | TEST: $V_I = 3.0$ V | | | 5.0 | μ A |
| Low-level input current | $I_{L(1)}$ | CE, CL, DI: $V_I = 0$ V | | | 5.0 | μ A |
| | $I_{L(2)}$ | XIN: $V_I = 0$ V | 2.3 | 3.0 | 4.3 | μ A |
| | $I_{L(3)}$ | TEST: $V_I = 0$ V | | | 5.0 | μ A |
| Internal feedback resistance | Rf | XIN | | 1.0 | | M Ω |
| Supply current | $I_{CC(1)}$ | $V_{CCR}, V_{CCD}: *1$ | | 5.5 | 9.0 | mA |
| PS supply current | $I_{CC(2)}$ | $V_{CCR}, V_{CCD}: *1$ | | 0.4 | 0.6 | mA |

*1: XIN = 12.8 MHz, 10 dBm, PI = 400 MHz, 0 dBm, other input pins = 0 V, output, I/O pins = OPEN CP OFF

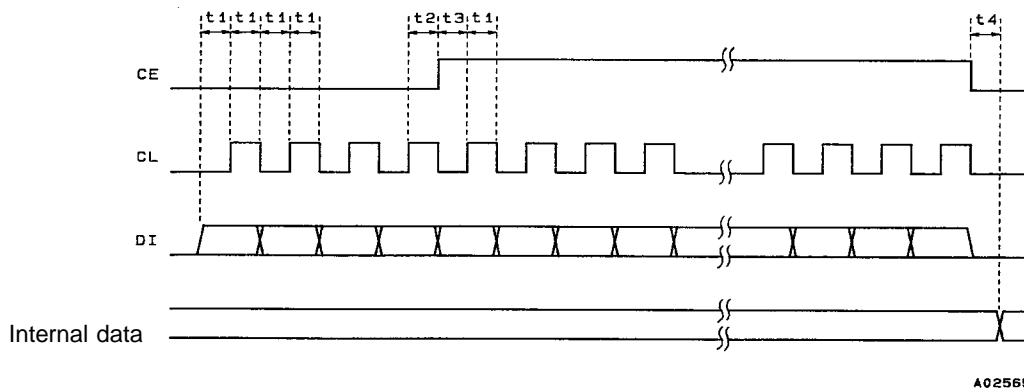
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2) Mode 2: Latch-2 data (Programmable divider data)



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Serial Data (Transfer) Timing



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$$t_1 \geq 1.0 \mu s$$

$$t_2 \geq 1.0 \mu s$$

$$t_3 \geq 1.0 \mu s$$

$$t_4 < 1.0 \mu s$$

Serial Data Explanation

| Pin No. | Control block/data | Internal block | | | | | | |
|----------|--|---|----------|------|---|---------|---|---------|
| (1) | Reference frequency data FR0 to FR1 | <ul style="list-style-type: none"> Data that sets the division ratio of the reference divider. Binary value with FR0 as the LSB. However, the settable division ratio factor is up to 4095. (Actual division ratio) = (Set division ratio) (x2: when DIV is "1") | | | | | | |
| (2) | 1/2 divider data DIV | <ul style="list-style-type: none"> Data that sets whether to use 1/2 DIV or to enter the through state. <table border="1"> <thead> <tr> <th>DIV data</th> <th>Item</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Through</td> </tr> <tr> <td>1</td> <td>1/2 DIV</td> </tr> </tbody> </table> | DIV data | Item | 0 | Through | 1 | 1/2 DIV |
| DIV data | Item | | | | | | | |
| 0 | Through | | | | | | | |
| 1 | 1/2 DIV | | | | | | | |

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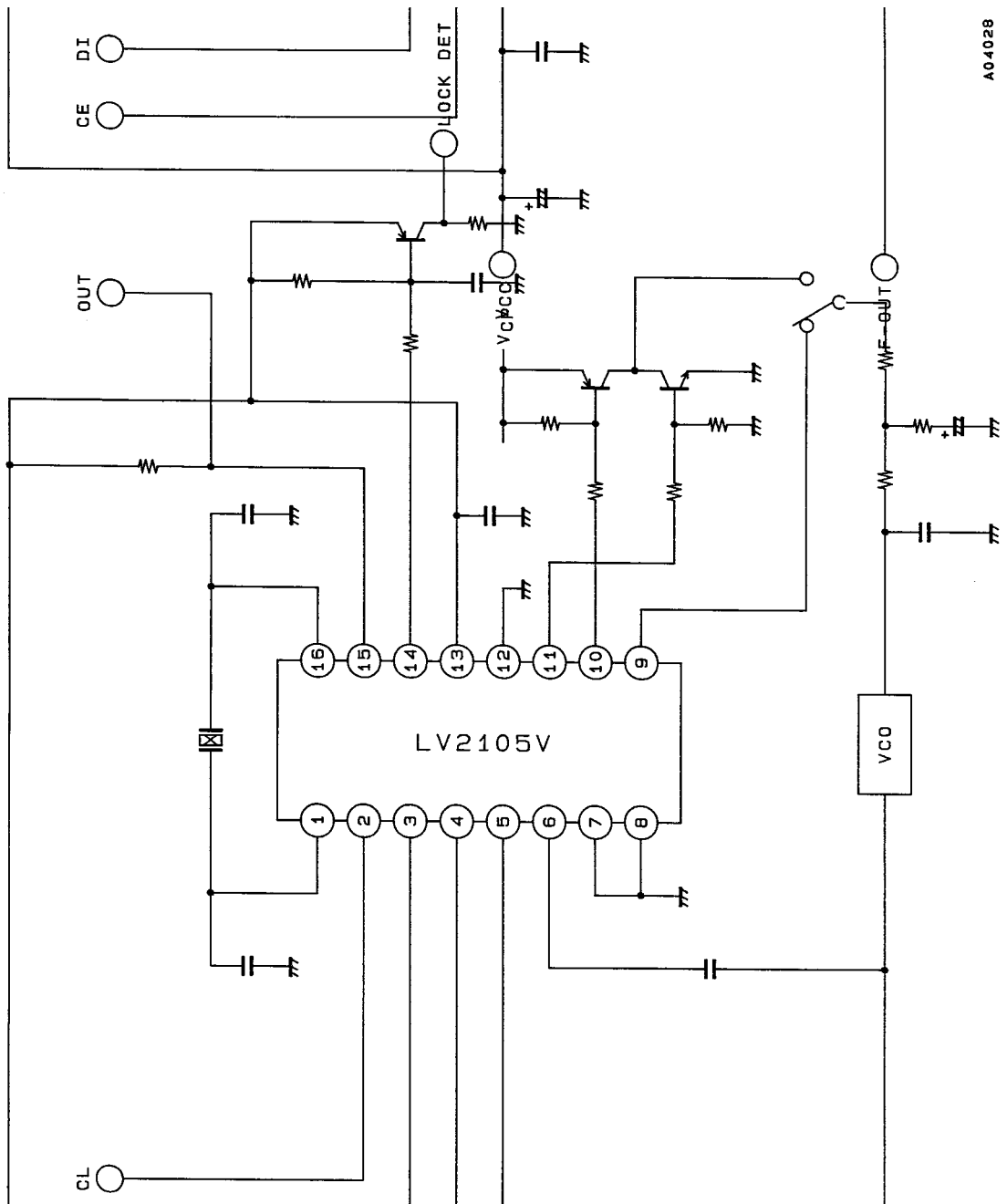
| Pin No. | Control block/data | Internal block | | | | | | |
|----------|--|--|----------|---------|---|-----------------|---|------------------|
| (3) | Power save data PS | <ul style="list-style-type: none"> ▪ Data that sets the power save mode on or off <table border="1" style="margin-left: 20px;"> <thead> <tr> <th style="text-align: center;">PS data</th> <th style="text-align: center;">Item</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">Power save mode</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">Normal operation</td> </tr> </tbody> </table> | PS data | Item | 0 | Power save mode | 1 | Normal operation |
| PS data | Item | | | | | | | |
| 0 | Power save mode | | | | | | | |
| 1 | Normal operation | | | | | | | |
| (4) | Output port data OUT | <ul style="list-style-type: none"> ▪ Data that sets the output of the output port <table border="1" style="margin-left: 20px;"> <thead> <tr> <th style="text-align: center;">OUT data</th> <th style="text-align: center;">OUT Pin</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">Low</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">High</td> </tr> </tbody> </table> | OUT data | OUT Pin | 0 | Low | 1 | High |
| OUT data | OUT Pin | | | | | | | |
| 0 | Low | | | | | | | |
| 1 | High | | | | | | | |
| (5) | Charge pump ON/OFF data CP | <ul style="list-style-type: none"> ▪ Data that sets whether to operate the charge pump or to implement high impedance. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th style="text-align: center;">CP data</th> <th style="text-align: center;">Item</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">High impedance</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">Normal operation</td> </tr> </tbody> </table> | CP data | Item | 0 | High impedance | 1 | Normal operation |
| CP data | Item | | | | | | | |
| 0 | High impedance | | | | | | | |
| 1 | Normal operation | | | | | | | |
| (6) | LSI test data TS1 | <ul style="list-style-type: none"> ▪ LSI test mode switch. Set TS1 = 0. Normally, the TEST pin is connected to GND. | | | | | | |
| (7) | Programmable divider data FP0 to FP16 | <ul style="list-style-type: none"> ▪ Data that sets the division ratio of the programmable divider. Binary value with FP0 as the LSB. However, the settable division ratio factor is up to 131071. | | | | | | |

Pin Functions

| | Pin Name | Pin Function | I/O Style |
|----|------------------|--|-------------------------------|
| 1 | XIN | Reference signal input pin (Xtal oscillation pin) | CMOS input |
| 2 | CL | Data input pin | CMOS, No pull-down |
| 3 | DI | Data input pin | CMOS, No pull-down |
| 4 | CE | Data input pin | CMOS, No pull-down |
| 5 | V _{CCR} | ECL block power supply pin | |
| 6 | PI | Comparison signal input pin | BIP input |
| 7 | GND R | ECL block GND pin | |
| 8 | TEST | LSI test pin. Must be connected to GND. | CMOS, No pull-down |
| 9 | CP | Built-in charge pump output pin | BIP |
| 10 | PDP | Phase comparator output for an external charge pump. If not to be used, connect to GND. | CMOS, Nch open-drain output |
| 11 | PDN | Phase comparator output for an external charge pump. | CMOS output |
| 12 | GND D | GND pin for circuits except the ECL block | |
| 13 | V _{CCD} | Power supply pin for circuits except the ECL block | |
| 14 | PE | Phase error output pin for phase comparator | CMOS output |
| 15 | OUT | Output port pin for switching external SW. | BIP NPN open-collector output |
| 16 | XOUT | Output pin for Xtal oscillation | CMOS output |

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Sample Application Circuit



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