



LP62E16256E-T Series

Preliminary

256K X 16 BIT LOW VOLTAGE CMOS SRAM

Document Title

256K X 16 BIT LOW VOLTAGE CMOS SRAM

Revision History

| <u>Rev. No.</u> | <u>History</u> | <u>Issue Date</u> | <u>Remark</u> |
|------------------------|-----------------------|--------------------------|----------------------|
| 0.0 | Initial issue | July 4, 2002 | Preliminary |



LP62E16256E-T Series

256K X 16 BIT LOW VOLTAGE CMOS SRAM

Features

- Operating voltage: 1.65V to 2.2V
- Access times: 70ns (max.)
- Current:
 - Very low power version: Operating: 30mA (max.)
 - Standby: 10μA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Data retention voltage: 1.2V (min.)
- Available in 44-pin TSOP and 48-ball CSP packages

General Description

The LP62E16256E-T is a low operating current 4,194,304-bit static random access memory organized as 262,144 words by 16 bits and operates on low power voltage from 1.65V to 2.2V. It is built using AMIC's high performance CMOS process.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

The chip enable input is provided for POWER-DOWN, device enable. Two byte enable inputs and an output enable input are included for easy interfacing.

Data retention is guaranteed at a power supply voltage as low as 1.2V.

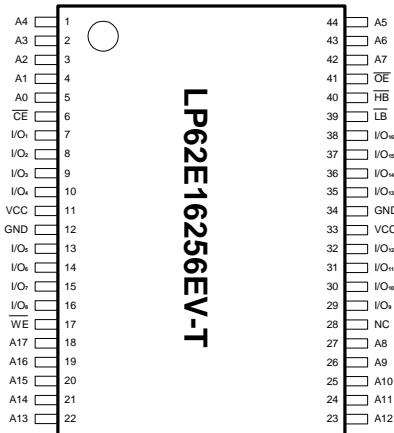
Product Family

| Product Family | Operating Temperature | VCC Range | Speed | Power Dissipation | | | Package Type |
|----------------|-----------------------|------------|-------|---|-----------------------------------|-------------------------------------|---------------------|
| | | | | Data Retention (I _{CCDR} , Typ.) | Standby (I _{SB1} , Typ.) | Operating (I _{CC2} , Typ.) | |
| LP62E16256E | -25°C ~ +85°C | 1.65V~2.2V | 70ns | 0.2μA | 1.4μA | 2mA | 44L TSOP 48B CSP |

1. Typical values are measured at VCC = 2.0V, T_A = 25°C and not 100% tested.
2. Data retention current VCC = 1.2V.

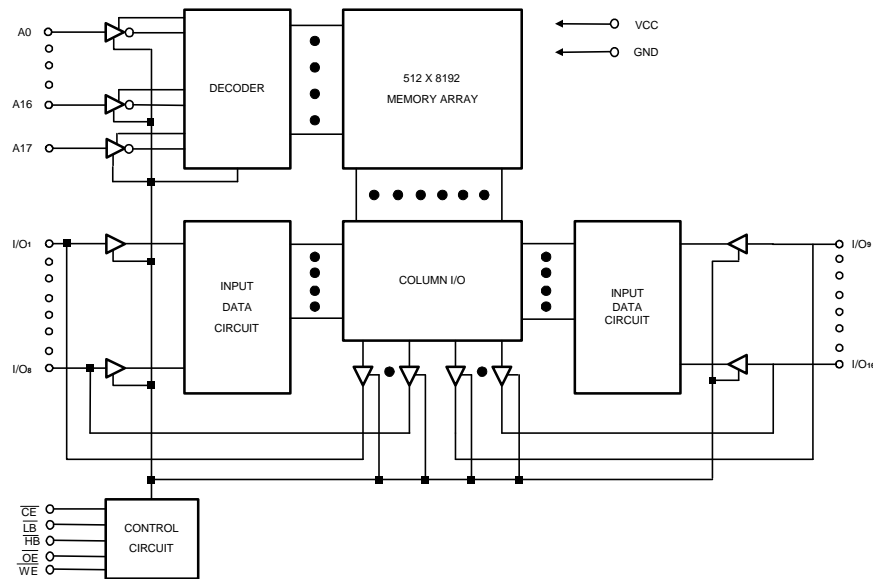
Pin Configurations

■ TSOP



■ CSP (Chip Size Package) 48-pin Top View

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|-------------------|-------------------|-----|-----|------------------|------------------|
| A | LB̄ | OĒ | A0 | A1 | A2 | NC |
| B | I/O ₉ | HB̄ | A3 | A4 | CĒ | I/O ₁ |
| C | I/O ₁₀ | I/O ₁₁ | A5 | A6 | I/O ₂ | I/O ₃ |
| D | GND | I/O ₁₂ | A17 | A7 | I/O ₄ | VCC |
| E | VCC | I/O ₁₃ | NC | A16 | I/O ₅ | GND |
| F | I/O ₁₅ | I/O ₁₄ | A14 | A15 | I/O ₆ | I/O ₇ |
| G | I/O ₁₆ | NC | A12 | A13 | WĒ | I/O ₈ |
| H | NC | A8 | A9 | A10 | A11 | NC |

Block Diagram

Pin Descriptions -- TSOP

| Pin No. | Symbol | Description |
|--------------------------------------|--------------------------------------|---|
| 1 - 5, 18 - 27, 42 - 44 | A0 - A17 | Address Inputs |
| 6 | \overline{CE} | Chip Enable Input |
| 7 - 10, 13 - 16, 29 - 32, 35 - 38 | I/O ₁ - I/O ₁₆ | Data Inputs/Outputs |
| 17 | \overline{WE} | Write Enable Input |
| 39 | \overline{LB} | Lower Byte Enable Input (I/O ₁ to I/O ₈) |
| 40 | \overline{HB} | Higher Byte Enable Input (I/O ₉ to I/O ₁₆) |
| 41 | \overline{OE} | Output Enable Input |
| 11, 33 | VCC | Power |
| 12, 34 | GND | Ground |
| 28 | NC | No Connection |

Pin Description - CSP

| Symbol | Description | Symbol | Description |
|--------------------------------------|--|------------------------|--|
| A0 - A17 | Address Inputs | $\overline{\text{HB}}$ | Higher Byte Enable Input (I/O ₉ - I/O ₁₆) |
| $\overline{\text{CE}}$ | Chip Enable | $\overline{\text{OE}}$ | Output Enable |
| I/O ₁ - I/O ₁₆ | Data Input/Output | VCC | Power Supply |
| $\overline{\text{WE}}$ | Write Enable Input | GND | Ground |
| $\overline{\text{LB}}$ | Byte Enable Input (I/O ₁ - I/O ₈) | NC | No Connection |

Recommended DC Operating Conditions

 (T_A = -25°C to + 85°C)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------------|--------------------|------|-----------|-----------|------|
| VCC | Supply Voltage | 1.65 | 1.8 / 2.0 | 2.2 | V |
| GND | Ground | 0 | 0 | 0 | V |
| V _{IH} | Input High Voltage | 1.4 | - | VCC + 0.2 | V |
| V _{IL} | Input Low Voltage | -0.2 | - | +0.4 | V |
| C _L | Output Load | - | - | 30 | pF |
| TTL | Output Load | - | - | 1 | - |



Absolute Maximum Ratings*

VCC to GND-0.5V to +3.0V
 IN, IN/OUT Volt to GND -0.5V to VCC + 0.5V
 Operating Temperature, Topr-25°C to +85°C
 Storage Temperature, Tstg.....-55°C to +125°C
 Power Dissipation, Pr.....0.7W

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (TA = -25°C to + 85°C, VCC = 1.65V to 2.2V, GND = 0V)

| Symbol | Parameter | LP62E16256E-70LLT | | Unit | Conditions |
|-----------|-----------------------------|-------------------|------|---------|--|
| | | Min. | Max. | | |
| I_{LI} | Input Leakage Current | - | 1 | μ A | $V_{IN} = GND \text{ to } VCC$ |
| I_{LO} | Output Leakage Current | - | 1 | μ A | $\overline{CE} = V_{IH}$ $\overline{HB} = V_{IH} \text{ or } \overline{OE} = V_{IH} \text{ or}$ $\overline{WE} = V_{IH}$ $V_{IO} = GND \text{ to } VCC$ |
| I_{CC} | Active Power Supply Current | - | 5 | mA | $\overline{CE} = V_{IL}, I_{IO} = 0mA$ |
| I_{CC1} | Dynamic Operating Current | - | 30 | mA | * Min. Cycle, Duty = 100% $\overline{CE} = V_i, I_{IO} = 0mA$ |
| I_{CC2} | | - | 10 | mA | $\overline{CE} = V_{IL}, V_{IH} = VCC,$ $V_{IL} = 0V, f = 1MHz,$ $I_{IO} = 0 \text{ mA}$ |
| I_{SB} | Standby Current | - | 0.5 | mA | $\overline{CE} = V_{IH}$ |
| I_{SB1} | | - | 10 | μ A | $\overline{CE} \geq VCC - 0.2V,$ $V_{IN} \geq 0V$ |
| V_{OL} | Output Low Voltage | - | 0.2 | V | $I_{OL} = 0.1 \text{ mA}$ |
| V_{OH} | Output High Voltage | 1.4 | - | V | $I_{OH} = -0.1 \text{ mA}$ |

Truth Table

| $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | $\overline{\text{LB}}$ | $\overline{\text{HB}}$ | I/O ₁ to I/O ₈ Mode | I/O ₉ to I/O ₁₆ Mode | VCC Current |
|------------------------|------------------------|------------------------|------------------------|------------------------|---|--|---|
| H | X | X | X | X | Not selected | Not selected | I _{SB1} , I _{SB} |
| X | X | X | H | H | High - Z | High - Z | I _{SB1} , I _{SB} |
| L | L | H | L | L | Read | Read | I _{CC1} , I _{CC2} , I _{CC} |
| | | | L | H | Read | High - Z | I _{CC1} , I _{CC2} , I _{CC} |
| | | | H | L | High - Z | Read | I _{CC1} , I _{CC2} , I _{CC} |
| L | X | L | L | L | Write | Write | I _{CC1} , I _{CC2} , I _{CC} |
| | | | L | H | Write | High - Z | I _{CC1} , I _{CC2} , I _{CC} |
| | | | H | L | High - Z | Write | I _{CC1} , I _{CC2} , I _{CC} |
| L | H | H | L | X | High - Z | High - Z | I _{CC1} , I _{CC2} , I _{CC} |
| L | H | H | X | L | High - Z | High - Z | I _{CC1} , I _{CC2} , I _{CC} |

Note: X = H or L

Capacitance (T_A = 25°C, f = 1.0MHz)

| Symbol | Parameter | Min. | Max. | Unit | Conditions |
|--------------------|--------------------------|------|------|------|-----------------------|
| C _{IN} * | Input Capacitance | | 6 | pF | V _{IN} = 0V |
| C _{I/O} * | Input/Output Capacitance | | 8 | pF | V _{I/O} = 0V |

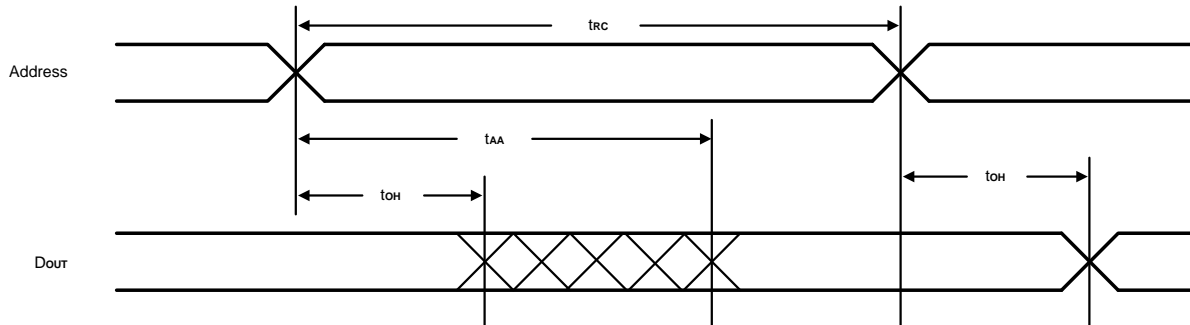
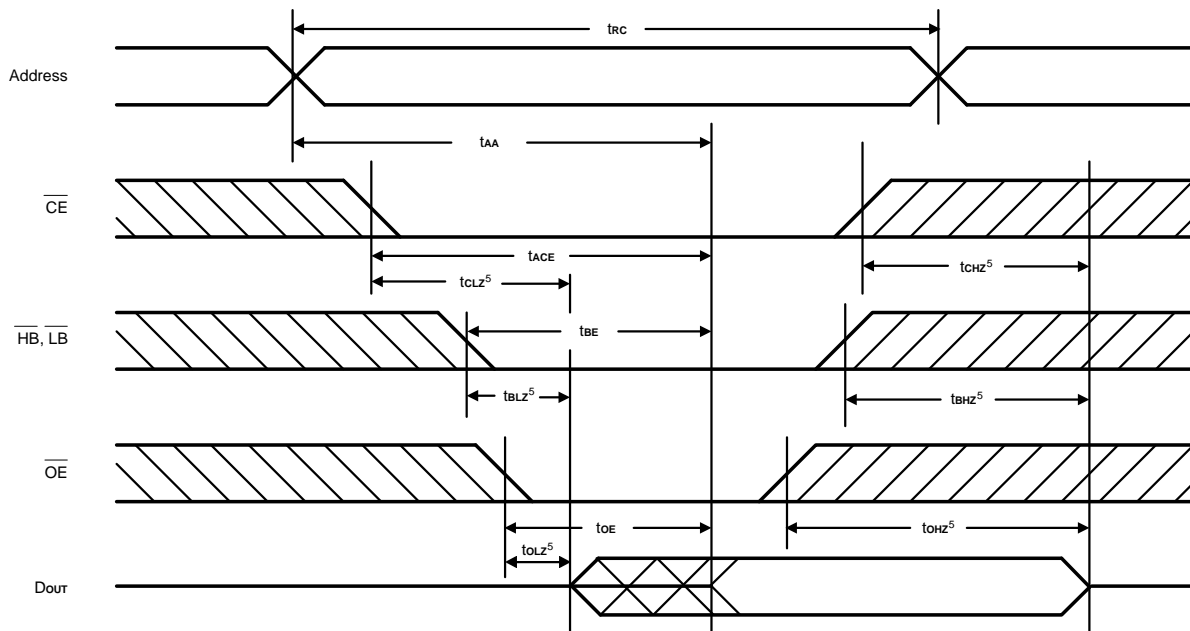
* These parameters are sampled and not 100% tested.



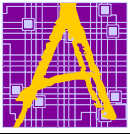
AC Characteristics (T_A = -25°C to +85°C, V_{CC} = 1.65V to 2.2V)

| Symbol | Parameter | LP62E16256E-70LLT | | Unit |
|------------------|------------------------------------|-------------------|------|------|
| | | Min. | Max. | |
| Read Cycle | | | | |
| t _{rc} | Read Cycle Time | 70 | - | ns |
| t _{AA} | Address Access Time | - | 70 | ns |
| t _{ACE} | Chip Enable Access Time | - | 70 | ns |
| t _{BE} | Byte Enable Access Time | - | 70 | ns |
| t _{OE} | Output Enable to Output Valid | - | 35 | ns |
| t _{CLZ} | Chip Enable to Output in Low Z | 10 | - | ns |
| t _{BLZ} | Byte Enable to Output in Low Z | 10 | - | ns |
| t _{OLZ} | Output Enable to Output in Low Z | 5 | - | ns |
| t _{CHZ} | Chip Disable to Output in High Z | - | 25 | ns |
| t _{BHZ} | Byte Disable to Output in High Z | - | 25 | ns |
| t _{OHZ} | Output Disable to Output in High Z | - | 25 | ns |
| t _{OH} | Output Hold from Address Change | 5 | - | ns |
| Write Cycle | | | | |
| t _{wc} | Write Cycle Time | 70 | - | ns |
| t _{cw} | Chip Enable to End of Write | 60 | - | ns |
| t _{bw} | Byte Enable to End of Write | 60 | - | ns |
| t _{AS} | Address Setup Time | 0 | - | ns |
| t _{AW} | Address Valid to End of Write | 60 | - | ns |
| t _{wP} | Write Pulse Width | 55 | - | ns |
| t _{wR} | Write Recovery Time | 0 | - | ns |
| t _{wHZ} | Write to Output in High Z | - | 25 | ns |
| t _{dW} | Data to Write Time Overlap | 30 | - | ns |
| t _{dH} | Data Hold from Write Time | 0 | - | ns |
| t _{OW} | Output Active from End of Write | 5 | - | ns |

Note: t_{CHZ}, t_{BHZ} and t_{OHZ} and t_{wHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

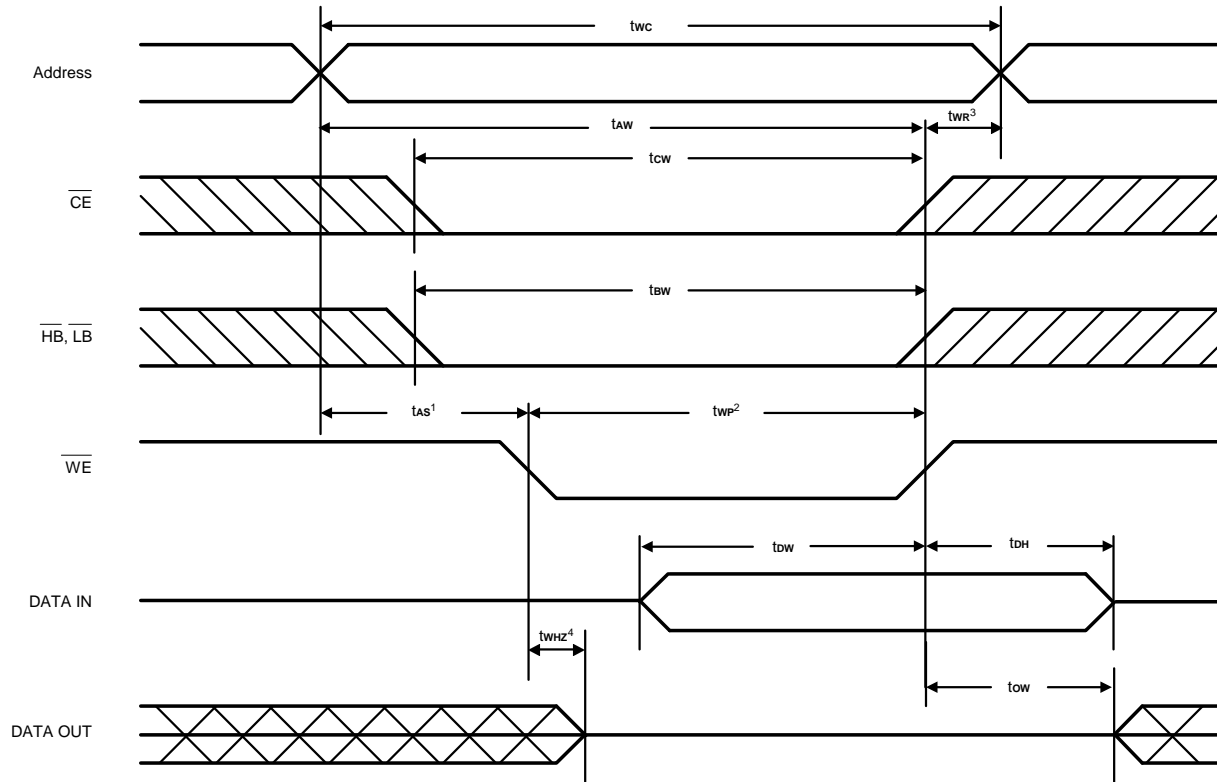
Timing Waveforms
Read Cycle 1^(1, 2, 4)

Read Cycle 2^(1, 2, 3)


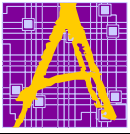
- Notes:
1. \overline{WE} is high for Read Cycle.
 2. Device is continuously enabled $\overline{CE} = V_{IL}$, $\overline{HB} = V_{IL}$ and, or $\overline{LB} = V_{IL}$.
 3. Address valid prior to or coincident with \overline{CE} and (\overline{HB} and, or \overline{LB}) transition low.
 4. $\overline{OE} = V_{IL}$.
 5. Transition is measured $\pm 200\text{mV}$ from steady state. This parameter is sampled and not 100% tested.



Timing Waveforms (continued)

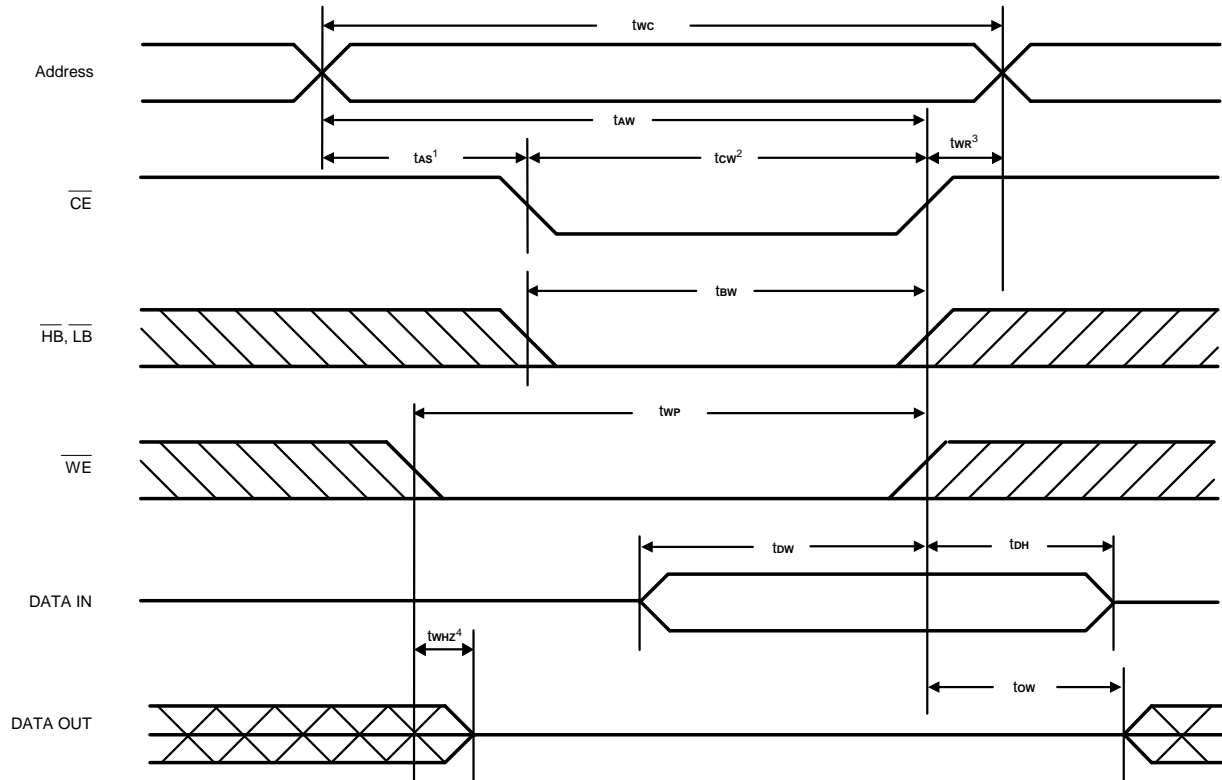
Write Cycle 1
(Write Enable Controlled)

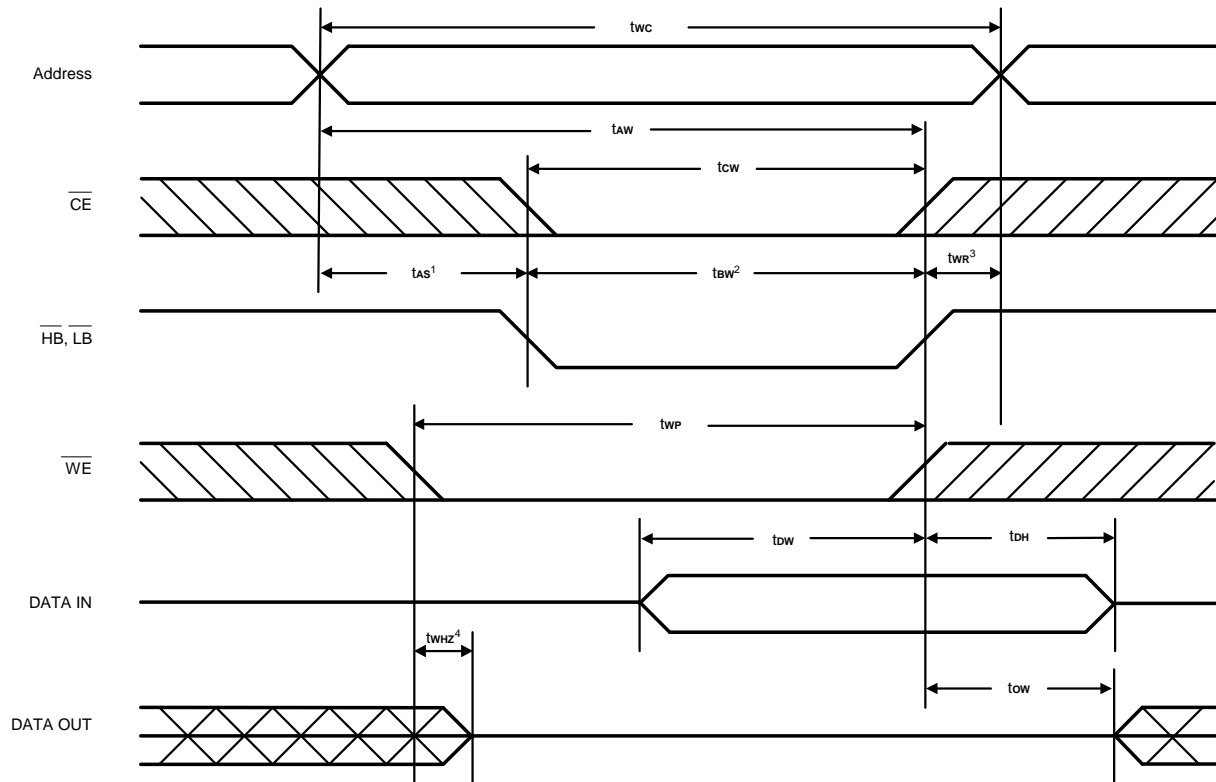




Timing Waveforms (continued)

Write Cycle 2
(Chip Enable Controlled)

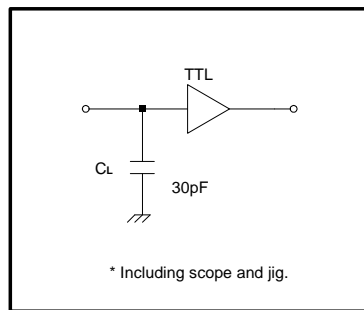
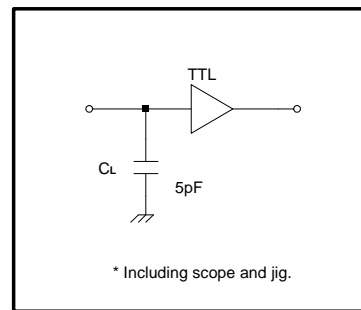


Timing Waveforms (continued)
**Write Cycle 3
(Byte Enable Controlled)**


- Notes:
1. t_{as} is measured from the address valid to the beginning of Write.
 2. A Write occurs during the overlap (t_{wp} , t_{bw}) of a low \overline{CE} , \overline{WE} and (\overline{HB} and , or \overline{LB}).
 3. t_{wr} is measured from the earliest of \overline{CE} or \overline{WE} or (\overline{HB} and , or \overline{LB}) going high to the end of the Write cycle.
 4. \overline{OE} level is high or low.
 5. Transition is measured $\pm 200\text{mV}$ from steady state. This parameter is sampled and not 100% tested.

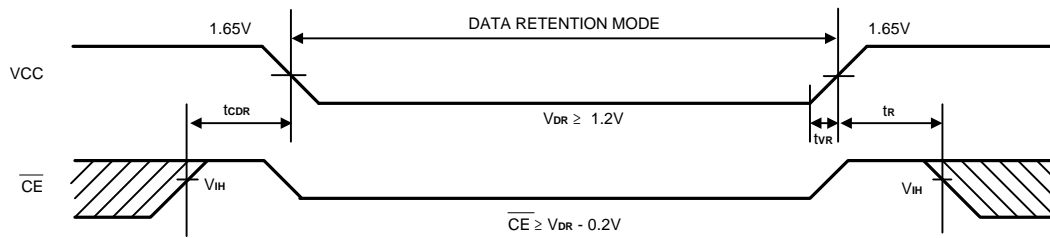
AC Test Conditions

| | |
|--|---------------------|
| Input Pulse Levels | 0.2V to Vcc -0.2V |
| Input Rise And Fall Time | 5 ns |
| Input and Output Timing Reference Levels | 0.9V |
| Output Load | See Figures 1 and 2 |


Figure 1. Output Load

Figure 2. Output Load for tCLZ, tOLZ, tCHZ, tOHZ, tWHZ, and tOW
Data Retention Characteristics (TA = -25°C to 85°C)

| Symbol | Parameter | Min. | Max. | Unit | Conditions |
|-------------------|--|-----------------|------|------|--|
| V _{DR} | VCC for Data Retention | 1.2 | 2.2 | V | $\overline{CE} \geq VCC - 0.2V$ |
| I _{CCDR} | Data Retention Current | - | 5* | μA | VCC = 1.2V, $\overline{CE} \geq VCC - 0.2V$ V _{IN} ≥ 0V |
| t _{CDR} | Chip Disable to Data Retention Time | 0 | - | ns | See Retention Waveform |
| t _R | Operation Recovery Time | t _{RC} | - | ns | |
| t _{VR} | VCC Rising Time from Data Retention Voltage to Operating Voltage | 5 | - | ms | |

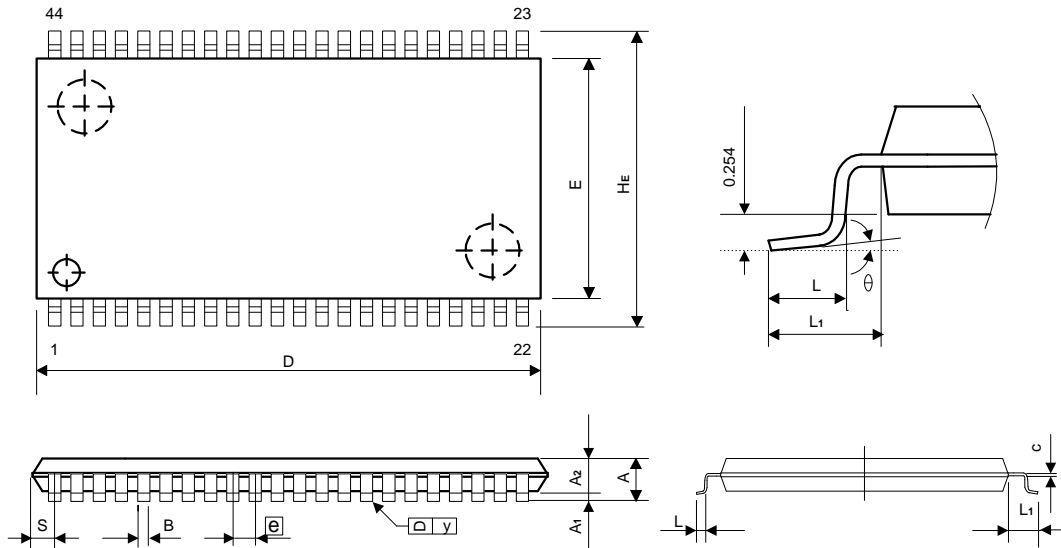
* LP62E16256E-70LLT I_{CCDR}: max. 1μA at TA = 0°C to + 40°C

Low VCC Data Retention Waveform

Ordering Information

| Part No. | Access Time (ns) | Operating Current Max. (mA) | Standby Current Max. (mA) | Package |
|--------------------|------------------|-----------------------------|---------------------------|----------|
| LP62E16256EV-70LLT | 70 | 30 | 10 | 44L TSOP |
| LP62E16256EU-70LLT | | 30 | 10 | 48L CSP |

Package Information
TSOP 44L TYPE II Outline Dimensions

unit: inches/mm



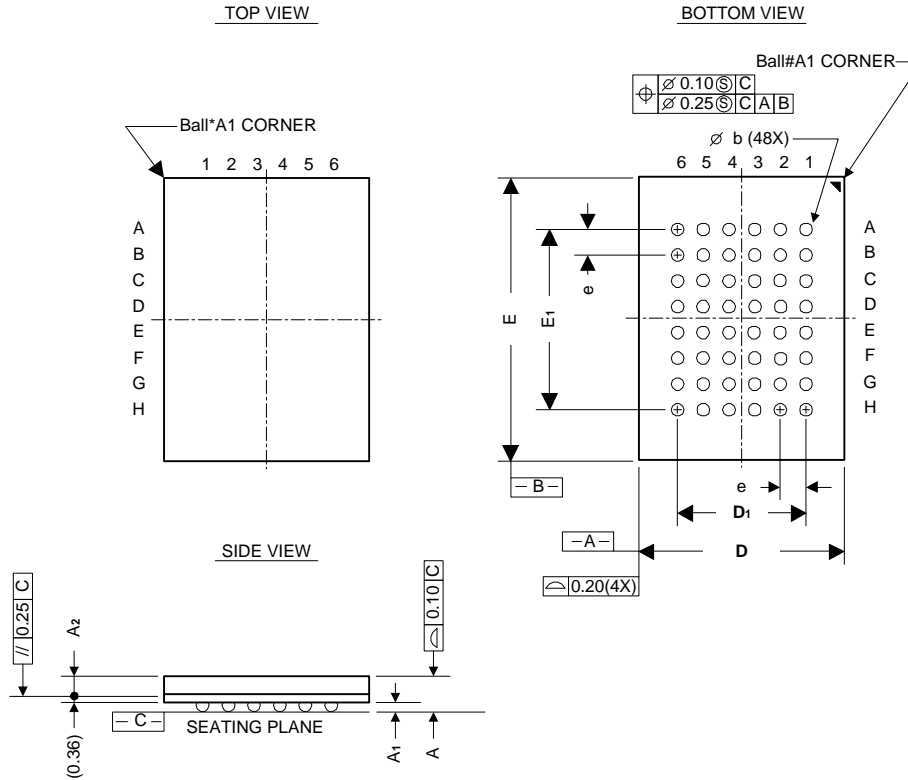
| Symbol | Dimension in inch | | | Dimension in mm | | |
|--------|-------------------|-------|-------|-----------------|-------|-------|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A | - | - | 0.047 | - | - | 1.20 |
| A1 | 0.002 | - | - | 0.05 | - | - |
| A2 | 0.037 | 0.039 | 0.041 | 0.95 | 1.00 | 1.05 |
| B | 0.010 | 0.014 | 0.018 | 0.25 | 0.35 | 0.45 |
| c | - | 0.006 | - | - | 0.15 | - |
| D | 0.721 | 0.725 | 0.729 | 18.31 | 18.41 | 18.51 |
| E | 0.396 | 0.400 | 0.404 | 10.06 | 10.16 | 10.26 |
| [e] | - | 0.031 | - | - | 0.80 | - |
| HE | 0.455 | 0.463 | 0.471 | 11.56 | 11.76 | 11.96 |
| L | 0.016 | 0.020 | 0.024 | 0.40 | 0.50 | 0.60 |
| L1 | - | 0.031 | - | - | 0.80 | - |
| S | - | - | 0.036 | - | - | 0.93 |
| y | - | - | 0.004 | - | - | 0.10 |
| theta | 0° | - | 5° | 0° | - | 5° |

Notes:

1. Dimension D&E do not include interlead flash.
2. Dimension B does not include dambar protrusion/intrusion.
3. Dimension S includes end flash.

Package Information
**48LD CSP (6 x 8 mm) Outline Dimensions
(48TFBGA)**

unit: mm



| Symbol | Dimensions in mm | | |
|----------------|------------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 1.04 | 1.14 | 1.24 |
| A ₁ | 0.20 | 0.25 | 0.30 |
| A ₂ | 0.48 | 0.53 | 0.58 |
| D | 5.90 | 6.00 | 6.10 |
| E | 7.90 | 8.00 | 8.10 |
| D ₁ | --- | 3.75 | --- |
| E ₁ | --- | 5.25 | --- |
| e | --- | 0.75 | --- |
| b | 0.30 | 0.35 | 0.40 |

Note:

1. THE BALL DIAMETER, BALL PITCH, STAND-OFF & PACKAGE THICKNESS ARE DIFFERENT FROM JEDEC SPEC MO192 (LOW PROFILE BGA FAMILY).
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM.
THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.