## Document Title

**128K X 8 BIT CMOS SRAM**

## Revision History

| Rev. No. | History | Issue Date | Remark |
|---|---|---|---|
| 1.1 | Add Pb-Free package type | August 19, 2004 | Final |
| 1.2 | Remove non-Pb-free package type | July 3, 2006 | |

# LP621024D-T Series

## 128K X 8 BIT CMOS SRAM

### Features

- Single +5V power supply
- Access times: 55/70 ns (max.)
- Current:
  Very low power version: Operating: 70mA (max.)
  Standby: 50μA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Output enable and two chip enable inputs for easy application
- Data retention voltage: 2V (min.)
- Available in 32-pin DIP, SOP TSOP and TSSOP (8 X 13.4mm) packages
- Pb-Free package only
- All Pb-free (Lead-free) products are RoHS compliant

### General Description

The LP621024D-T is a low operating current 1,048,576-bit static random access memory organized as 131,072 words by 8 bits and operates on a single 5V power supply.
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.
Two chip enable inputs are provided for POWER-DOWN and device enable and an output enable input is included for easy interfacing.
Data retention is guaranteed at a power supply voltage as low as 2V.

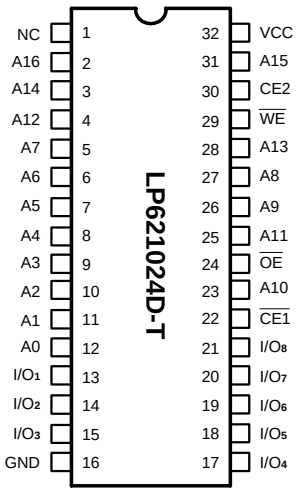
### Product Family

| Product Family | Operating Temperature | VCC Range | Speed | Power Dissipation | | | Package Type |
|---|---|---|---|---|---|---|---|
| | | | | Data Retention ($I_{CCDR}$, Typ.) | Standby ($I_{SB1}$, Typ.) | Operating ($I_{CC2}$, Typ.) | |
| LP621024D | -25°C to +85°C | 4.5V~5.5V | 55ns / 70ns | 0.5μA | 2μA | 10mA | 32L DIP/ SOP/TSOP/ TSSOP |

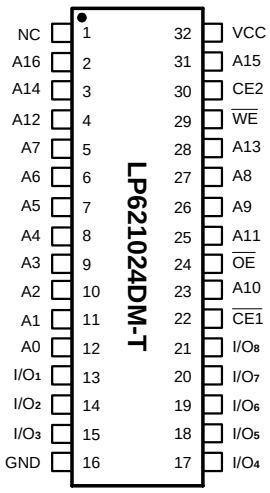
1. Typical values are measured at VCC = 5.0V, $T_A$ = 25°C and not 100% tested.
2. Data retention current VCC = 2.0V.

### Pin Configurations

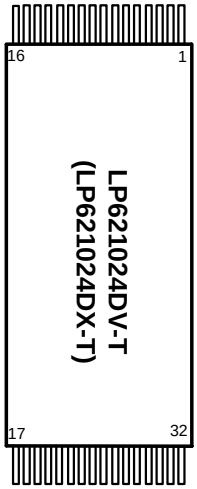
■ DIP




■ SOP

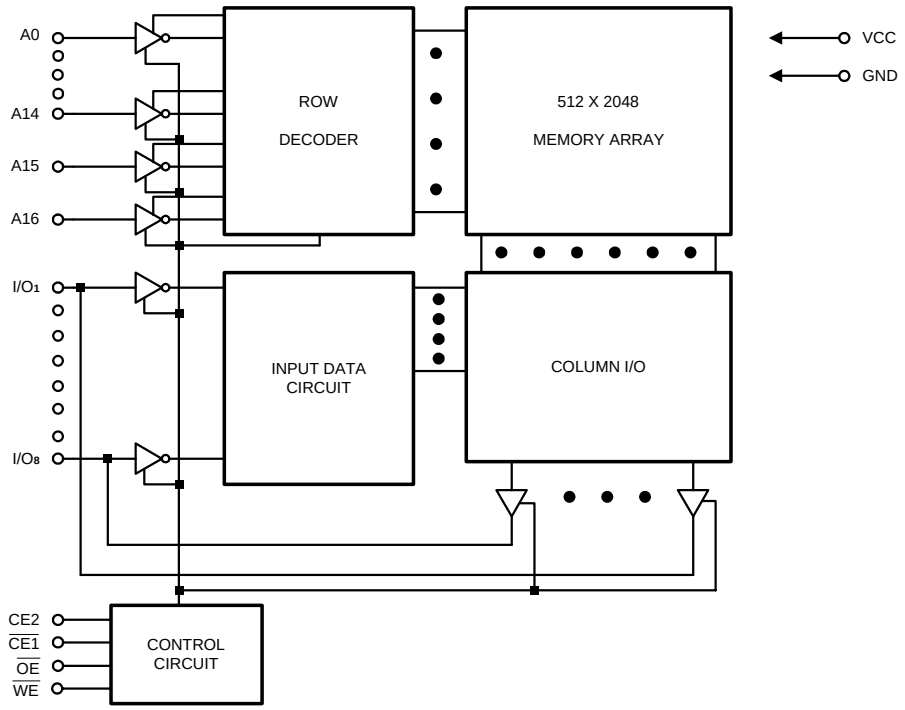



■ TSOP/(TSSOP)




| Pin No. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin Name | A11 | A9 | A8 | A13 | $\overline{WE}$ | CE2 | A15 | VCC | NC | A16 | A14 | A12 | A7 | A6 | A5 | A4 |
| Pin No. | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
| Pin Name | A3 | A2 | A1 | A0 | I/O1 | I/O2 | I/O3 | GND | I/O4 | I/O5 | I/O6 | I/O7 | I/O8 | $\overline{CE1}$ | A10 | $\overline{OE}$ |

## Block Diagram




## Pin Descriptions - DIP/SOP

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | NC | No Connection |
| 2 - 12, 23, 25 - 28, 31 | A0 - A16 | Address Inputs |
| 13 - 15, 17 - 21 | $I/O_1$ - $I/O_8$ | Data Input/Outputs |
| 16 | GND | Ground |
| 22 | $\overline{CE1}$ | Chip Enable |
| 24 | $\overline{OE}$ | Output Enable |
| 29 | $\overline{WE}$ | Write Enable |
| 30 | CE2 | Chip Enable |
| 32 | VCC | Power Supply (+5V) |

## Pin Description - TSOP/TSSOP

| Pin No. | Symbol | Description |
|---|---|---|
| 1 - 4, 7, 10 - 20, 31 | A0 - A16 | Address Inputs |
| 5 | $\overline{WE}$ | Write Enable |
| 6 | CE2 | Chip Enable |
| 8 | VCC | Power Supply |
| 9 | NC | No Connection |
| 21 - 23, 25 - 29 | $I/O_1$ - $I/O_8$ | Data Input/Outputs |
| 24 | GND | Ground |
| 30 | $\overline{CE1}$ | Chip Enable |
| 32 | $\overline{OE}$ | Output Enable |

### Recommended DC Operating Conditions

($T_A$ = -25°C to + 85°C)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Ground | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage | 2.2 | 3.5 | VCC + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | -0.3 | 0 | +0.8 | V |
| $C_L$ | Output Load | - | - | 30 | pF |
| TTL | Output Load | - | - | 1 | - |

### Absolute Maximum Ratings*

VCC to GND .....-0.5V to + 7.0V
IN, IN/OUT Volt to GND..... -0.5V to VCC + 0.5V
Operating Temperature, Topr ..... -25°C to + 85°C
Storage Temperature, Tstg..... -55°C to + 125°C
Temperature Under Bias, Tbias..... -10°C to + 85°C
Power Dissipation, $P_T$.....0.7W
Soldering Temp. & Time ..... 260°C, 10 sec

### *Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

### DC Electrical Characteristics ($T_A$ = -25°C to + 85°C, VCC = 5V ± 10%, GND = 0V)

| Symbol | Parameter | LP621024D-55LLT | | LP621024D-70LLT | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $\lvert I_{LI} \rvert$ | Input Leakage Current | - | 1 | - | 1 | µA | $V_{IN}$ = GND to VCC |
| $\lvert I_{LO} \rvert$ | Output Leakage Current | - | 1 | - | 1 | µA | $\overline{CE1}$ = $V_{IH}$ or CE2 = $V_{IL}$ or $\overline{OE}$ = $V_{IH}$ or $\overline{WE}$ = $V_{IL}$ $V_{I/O}$ = GND to VCC |
| $I_{CC}$ | Active Power Supply Current | - | 15 | - | 15 | mA | $\overline{CE1}$ = $V_{IL}$, CE2 = $V_{IH}$ $I_{I/O}$ = 0mA |
| $I_{CC1}$ | Dynamic Operating Current | - | 70 | - | 70 | mA | Min. Cycle, Duty = 100% $\overline{CE1}$ = $V_{IL}$, CE2 = $V_{IH}$ $I_{I/O}$ = 0mA |
| $I_{CC2}$ | | - | 15 | - | 15 | mA | $\overline{CE1}$ = $V_{IL}$, CE2 = $V_{IH}$ $V_{IH}$ = VCC, $V_{IL}$ = 0V f = 1MHz, $I_{I/O}$ = 0mA |

## DC Electrical Characteristics (continued)

| Symbol | Parameter | LP621024D-55LLT | | LP621024D-70LLT | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $I_{SB}$ | Standby Power Supply Current | - | 2 | - | 2 | mA | $\overline{CE1}$ = $V_{IH}$ or CE2 = $V_{IL}$ |
| $I_{SB1}$ | | - | 50 | - | 50 | μA | $\overline{CE1} \geq$ VCC - 0.2V<br>CE2 ≥ VCC - 0.2V<br>$V_{IN} \geq$ 0V |
| $I_{SB2}$ | | - | 50 | - | 50 | μA | CE2 ≤ 0.2V<br>$V_{IN} \geq$ 0V |
| $V_{OL}$ | Output Low Voltage | - | 0.4 | - | 0.4 | V | $I_{OL}$ = 2.1mA |
| $V_{OH}$ | Output High Voltage | 2.4 | - | 2.4 | - | V | $I_{OH}$ = -1.0mA |

## Truth Table

| Mode | $\overline{CE1}$ | CE2 | $\overline{OE}$ | $\overline{WE}$ | I/O Operation | Supply Current |
|---|---|---|---|---|---|---|
| Standby | H | X | X | X | High Z | $I_{SB}$, $I_{SB1}$ |
| | X | L | X | X | High Z | $I_{SB}$, $I_{SB2}$ |
| Output Disable | L | H | H | H | High Z | $I_{CC}$, $I_{CC1}$, $I_{CC2}$ |
| Read | L | H | L | H | $D_{OUT}$ | $I_{CC}$, $I_{CC1}$, $I_{CC2}$ |
| Write | L | H | X | L | $D_{IN}$ | $I_{CC}$, $I_{CC1}$, $I_{CC2}$ |

Note: X = H or L

## Capacitance ($T_A$ = 25°C, f = 1.0MHz)

| Symbol | Parameter | Min. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| $C_{IN}$* | Input Capacitance | | 6 | pF | $V_{IN}$ = 0V |
| $C_{I/O}$* | Input/Output Capacitance | | 8 | pF | $V_{I/O}$ = 0V |

* These parameters are sampled and not 100% tested.

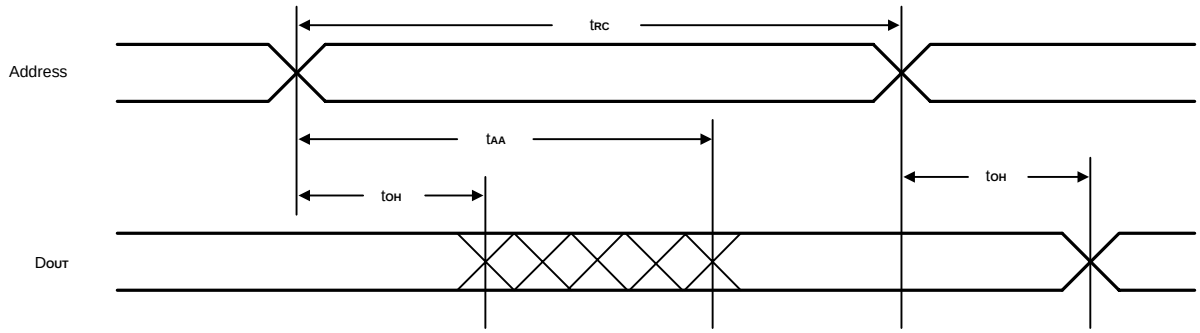
**AC Characteristics** ($T_A$ = -25°C to + 85°C, VCC = 5V ± 10%)

| Symbol | Parameter | | LP621024D-55LLT | | LP621024D-70LLT | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| Read Cycle | | | | | | | |
| $t_{RC}$ | Read Cycle Time | | 55 | - | 70 | - | ns |
| $t_{AA}$ | Address Access Time | | - | 55 | - | 70 | ns |
| $t_{ACE1}$ | Chip Enable Access Time | $\overline{CE1}$ | - | 55 | - | 70 | ns |
| $t_{ACE2}$ | | CE2 | - | 55 | - | 70 | ns |
| $t_{OE}$ | Output Enable to Output Valid | | - | 30 | - | 35 | ns |
| $t_{CLZ1}$ | Chip Enable to Output in Low Z | $\overline{CE1}$ | 10 | - | 10 | - | ns |
| $t_{CLZ2}$ | | CE2 | 10 | - | 10 | - | ns |
| $t_{OLZ}$ | Output Enable to Output in Low Z | | 5 | - | 5 | - | ns |
| $t_{CHZ1}$ | Chip Disable to Output in High Z | $\overline{CE1}$ | 0 | 20 | 0 | 25 | ns |
| $t_{CHZ2}$ | | CE2 | 0 | 20 | 0 | 25 | ns |
| $t_{OHZ}$ | Output Disable to Output in High Z | | 0 | 20 | 0 | 25 | ns |
| $t_{OH}$ | Output Hold from Address Change | | 5 | - | 5 | - | ns |
| Write Cycle | | | | | | | |
| $t_{WC}$ | Write Cycle Time | | 55 | - | 70 | - | ns |
| $t_{CW}$ | Chip Enable to End of Write | | 50 | - | 60 | - | ns |
| $t_{AS}$ | Address Setup Time | | 0 | - | 0 | - | ns |
| $t_{AW}$ | Address Valid to End of Write | | 50 | - | 60 | - | ns |
| $t_{WP}$ | Write Pulse Width | | 40 | - | 50 | - | ns |
| $t_{WR}$ | Write Recovery Time | | 0 | - | 0 | - | ns |
| $t_{WHZ}$ | Write to Output in High Z | | 0 | 25 | 0 | 30 | ns |
| $t_{DW}$ | Data to Write Time Overlap | | 25 | - | 30 | - | ns |
| $t_{DH}$ | Data Hold from Write Time | | 0 | - | 0 | - | ns |
| $t_{OW}$ | Output Active from End of Write | | 5 | - | 5 | - | ns |

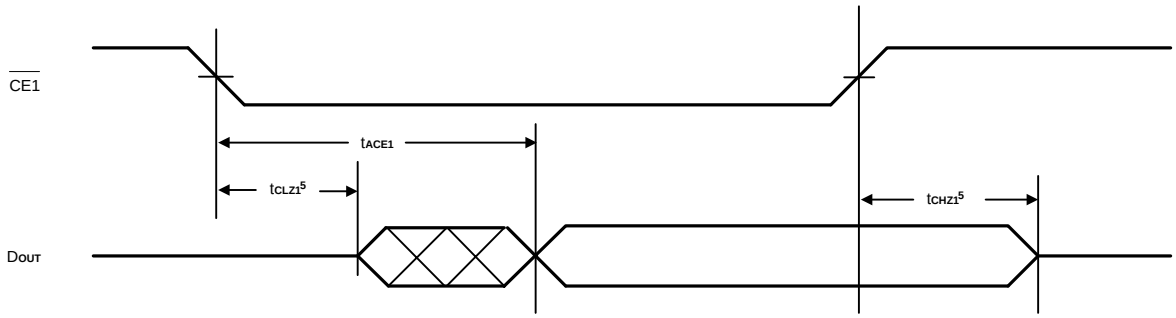
Notes: $t_{CHZ1}$, $t_{CHZ2}$, $t_{OHZ}$, and $t_{WHZ}$ are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

## Timing Waveforms

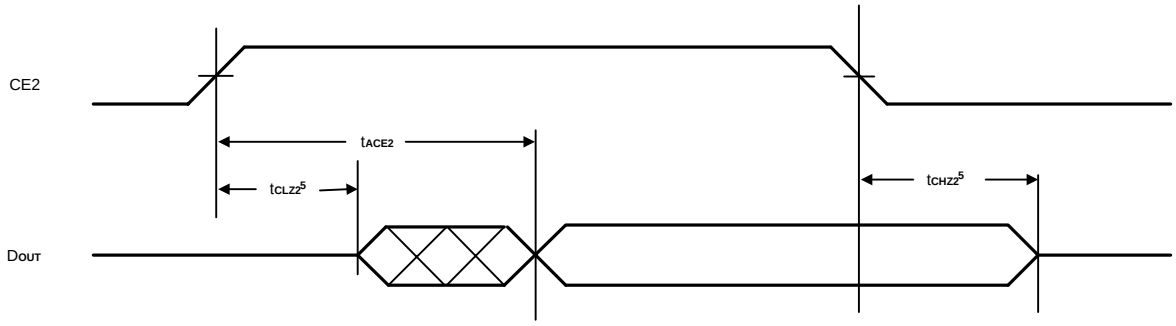
### Read Cycle 1 (1, 2, 4)




### Read Cycle 2 (1, 3, 4, 6)

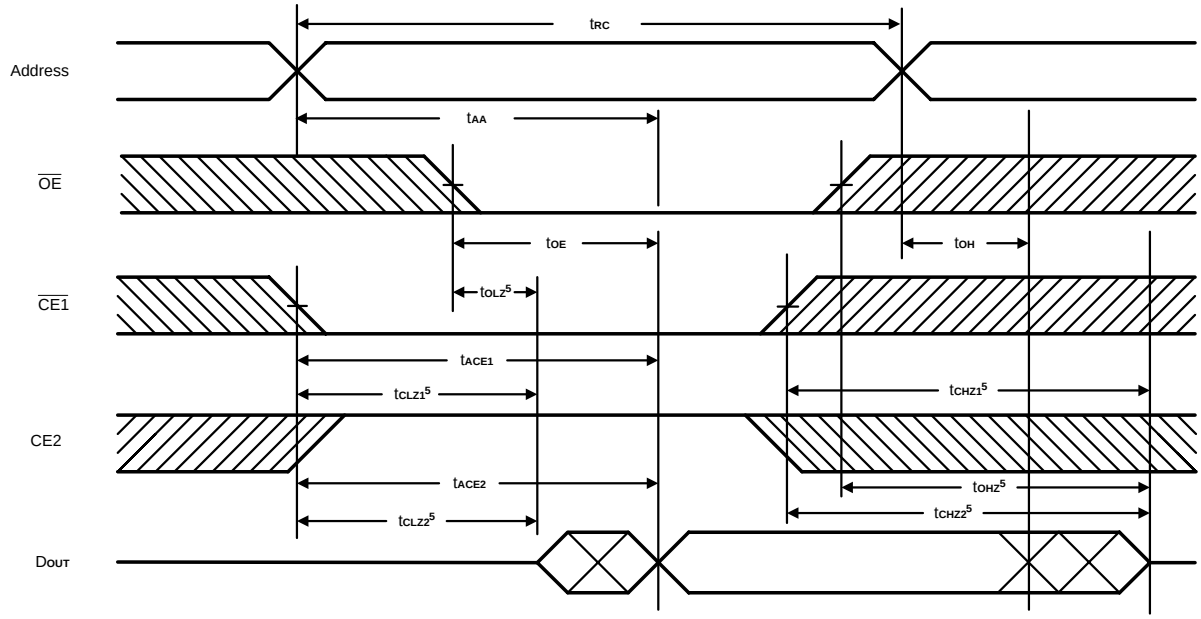



### Read Cycle 3 (1, 4, 7, 8)



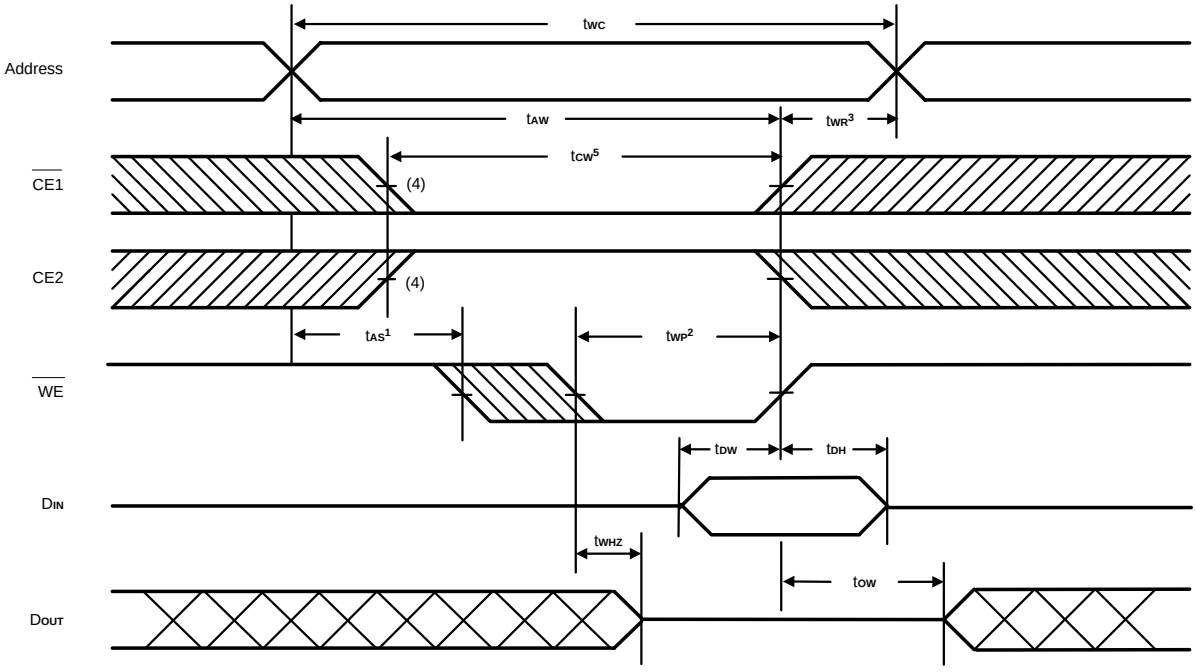
## Timing Waveforms (continued)

### Read Cycle 4 (1)



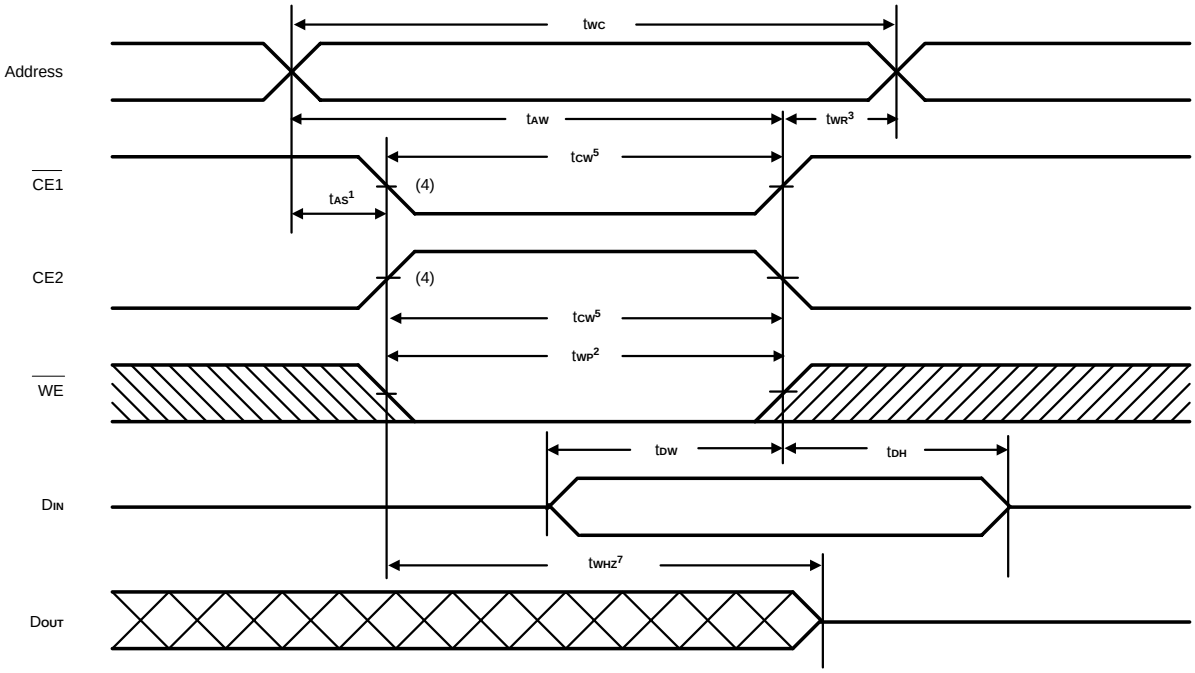

Notes: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled $\overline{CE1}$ = $V_{IL}$ and CE2 = $V_{IH}$.
3. Address valid prior to or coincident with $\overline{CE1}$ transition low.
4. $\overline{OE}$ = $V_{IL}$.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
6. CE2 is high.
7. $\overline{CE1}$ is low.
8. Address valid prior to or coincident with CE2 transition high.

### Write Cycle 1(6)
### (Write Enable Controlled)



## Timing Waveforms (continued)

### Write Cycle 2
### (Chip Enable Controlled)




Notes: 1. $t_{AS}$ is measured from the address valid to the beginning of Write.
2. A Write occurs during the overlap ($t_{WP}$) of a low $\overline{CE1}$, a high CE2 and a low $\overline{WE}$.
3. $t_{WR}$ is measured from the earliest of $\overline{CE1}$ or $\overline{WE}$ going high or CE2 going low to the end of the Write cycle.
4. If the $\overline{CE1}$ low transition or the CE2 high transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. $t_{CW}$ is measured from the later of $\overline{CE1}$ going low or CE2 going high to the end of Write.
6. $\overline{OE}$ is continuously low. ($\overline{OE}$ = $V_{IL}$)
7. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

### AC Test Conditions

| | |
|---|---|
| Input Pulse Levels | 0V to 3.0V |
| Input Rise and Fall Time | 5 ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | See Figures 1 and 2 |

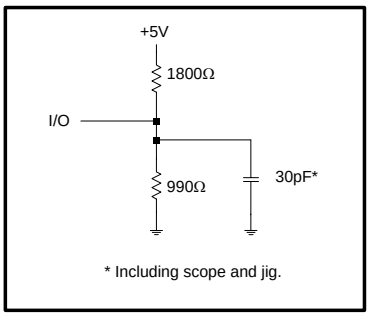



**Figure 1. Output Load**

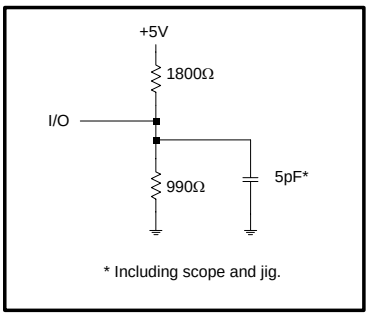


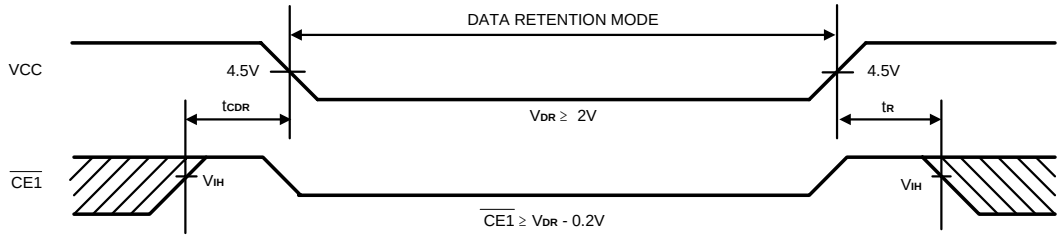

**Figure 2. Output Load for $t_{CLZ1}$, $t_{CLZ2}$, $t_{OHZ}$, $t_{OLZ}$, $t_{CHZ1}$, $t_{CHZ2}$, $t_{WHZ}$, and $t_{OW}$**

### Data Retention Characteristics ($T_A$ = -25°C to 85°C)

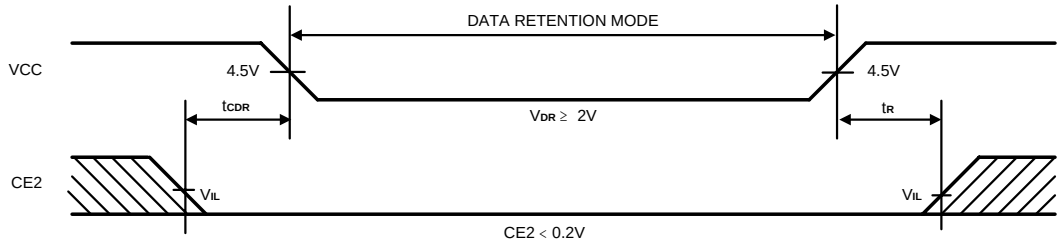
| Symbol | Parameter | | Min. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| $V_{DR1}$ | VCC for Data Retention | | 2.0 | 5.5 | V | $\overline{CE1} \geq$ VCC - 0.2V |
| $V_{DR2}$ | | | 2.0 | 5.5 | V | CE2 ≤ 0.2V<br>$\overline{CE1} \geq$ VCC - 0.2V or<br>$\overline{CE1} \leq$ 0.2V |
| $I_{CCDR1}$ | Data Retention Current | LL-Version | - | 20** | µA | VCC = 2.0V,<br>$\overline{CE1} \geq$ VCC - 0.2V<br>CE2 ≥ VCC - 0.2V<br>$V_{IN} \geq$ 0V |
| $I_{CCDR2}$ | | LL-Version | - | 20** | µA | VCC = 2.0V<br>CE2 ≤ 0.2V<br>$V_{IN} \geq$ 0V |
| $t_{CDR}$ | Chip Disable to Data Retention Time | | 0 | - | ns | See Retention Waveform |
| $t_R$ | Operation Recovery Time | | 5 | - | ms | |

** LP621024D-55LLT/70LLT $I_{CCDR}$: Max. 2µA at $T_A$ = 0°C to + 40 °C

### Low VCC Data Retention Waveform (1) ($\overline{CE1}$ Controlled)




### Low VCC Data Retention Waveform (2) (CE2 Controlled)



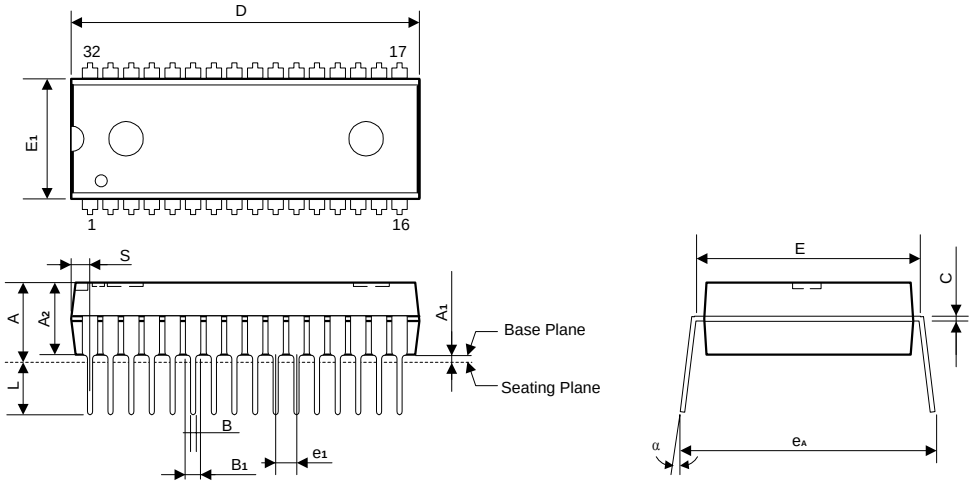
## Ordering Information

| Part No. | Access Time (ns) | Operating Current Max. (mA) | Standby Current Max. (μA) | Package |
|---|---|---|---|---|
| LP621024D-55LLTF | 55 | 70 | 50 | 32L Pb-Free DIP |
| LP621024DM-55LLTF | | 70 | 50 | 32L Pb-Free SOP |
| LP621024DV-55LLTF | | 70 | 50 | 32L Pb-Free TSOP |
| LP621024DX-55LLTF | | 70 | 50 | 32L Pb-Free TSSOP |
| LP621024D-70LLTF | 70 | 70 | 50 | 32L Pb-Free DIP |
| LP621024DM-70LLTF | | 70 | 50 | 32L Pb-Free SOP |
| LP621024DV-70LLTF | | 70 | 50 | 32L Pb-Free TSOP |
| LP621024DX-70LLTF | | 70 | 50 | 32L Pb-Free TSSOP |

## Package Information

### P-DIP 32L Outline Dimensions

unit: inches/mm



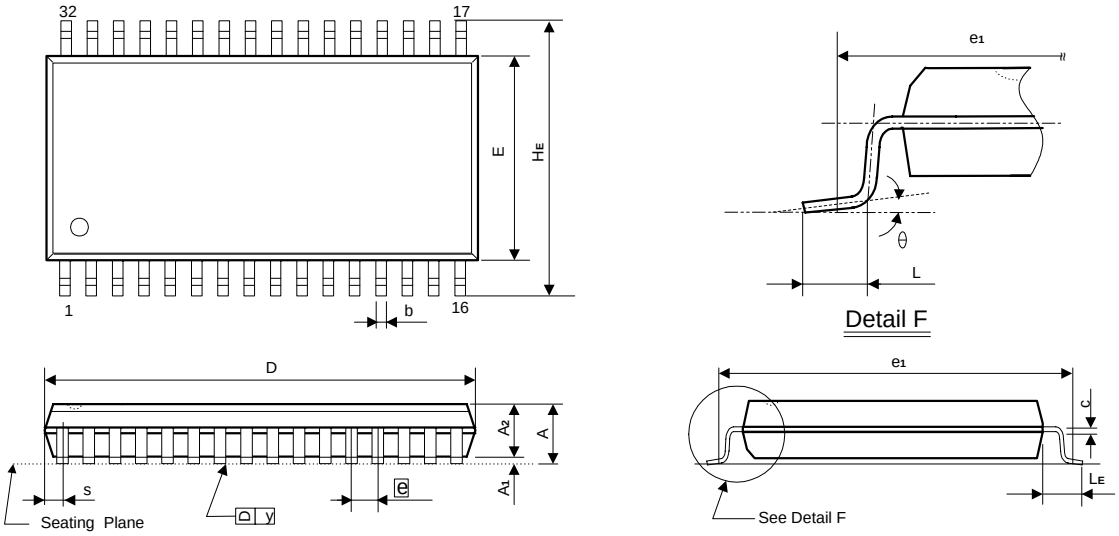

| Symbol | Dimensions in inches | Dimensions in mm |
|---|---|---|
| A | 0.210 Max. | 5.33 Max. |
| $A_1$ | 0.010 Min. | 0.25 Min. |
| $A_2$ | 0.155±0.010 | 3.94±0.25 |
| B | 0.018 +0.004 -0.002 | 0.46 +0.10 -0.05 |
| $B_1$ | 0.050 +0.004 -0.002 | 1.27 +0.10 -0.05 |
| C | 0.010 +0.004 -0.002 | 0.25 +0.11 -0.05 |
| D | 1.650 Typ. (1.670 Max.) | 41.91 Typ. (42.42 Max.) |
| E | 0.600±0.010 | 15.24±0.25 |
| $E_1$ | 0.550 Typ. (0.562 Max.) | 13.97 Typ. (14.27 Max.) |
| $e_1$ | 0.100±0.010 | 2.54±0.25 |
| L | 0.130±0.010 | 3.30±0.25 |
| α | 0° ~ 15° | 0° ~ 15° |
| $e_A$ | 0.655±0.035 | 16.64±0.89 |
| S | 0.090 Max. | 2.29 Max. |

**Notes:**
1. The maximum value of dimension D includes end flash.
2. Dimension $E_1$ does not include resin fins.
3. Dimension S includes end flash.

## Package Information

### SOP (W.B.) 32L Outline Dimensions

unit: inches/mm




| Symbol | Dimensions in inches | Dimensions in mm |
|---|---|---|
| A | 0.118 Max. | 3.00 Max. |
| $A_1$ | 0.004 Min. | 0.10 Min. |
| $A_2$ | 0.106±0.005 | 2.69±0.13 |
| b | 0.016 +0.004<br>-0.002 | 0.41 +0.10<br>-0.05 |
| c | 0.008 +0.004<br>-0.002 | 0.20 +0.10<br>-0.05 |
| D | 0.805 Typ. (0.820 Max.) | 20.45 Typ. (20.83 Max.) |
| E | 0.445±0.010 | 11.30±0.25 |
| e | 0.050 ±0.006 | 1.27±0.15 |
| $e_1$ | 0.525 NOM. | 13.34 NOM. |
| $H_E$ | 0.556±0.010 | 14.12±0.25 |
| L | 0.031±0.008 | 0.79±0.20 |
| $L_E$ | 0.055±0.008 | 1.40±0.20 |
| S | 0.044 Max. | 1.12 Max. |
| y | 0.004 Max. | 0.10 Max. |
| θ | 0° ~ 10° | 0° ~ 10° |

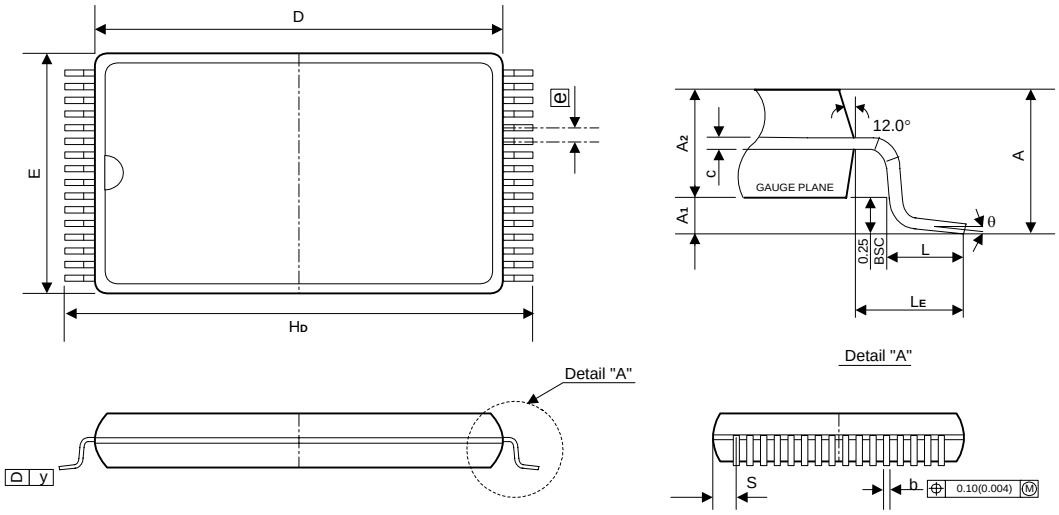
**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension $e_1$ is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

## Package Information

### TSOP 32L TYPE I (8 X 20mm) Outline Dimensions

unit: inches/mm




| Symbol | Dimensions in inches | Dimensions in mm |
|---|---|---|
| A | 0.047 Max. | 1.20 Max. |
| $A_1$ | 0.004±0.002 | 0.10±0.05 |
| $A_2$ | 0.039±0.002 | 1.00±0.05 |
| b | 0.008±0.001 | 0.20±0.03 |
| c | 0.006±0.001 | 0.15±0.02 |
| D | 0.724±0.004 | 18.40±0.10 |
| E | 0.315±0.004 | 8.00±0.10 |
| e | 0.020 TYP. | 0.50 TYP. |
| $H_D$ | 0.787±0.007 | 20.00±0.20 |
| L | 0.020±0.004 | 0.50±0.10 |
| $L_E$ | 0.031 TYP. | 0.80 TYP. |
| S | 0.0167 TYP. | 0.425 TYP. |
| Y | 0.004 Max. | 0.10 Max. |
| θ | 0° ~ 6° | 0° ~ 6° |

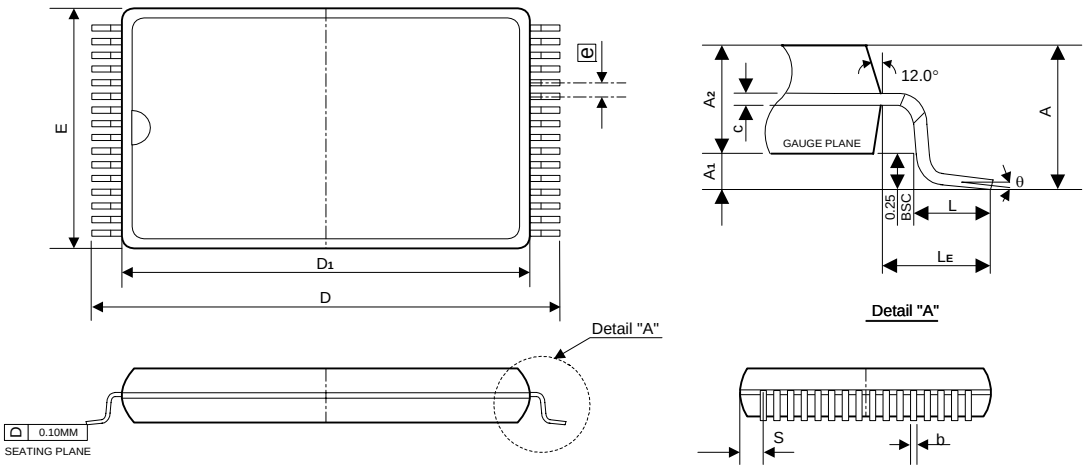
**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension $e_1$ is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

## Package Information

### TSSOP 32L TYPE I (8 X 13.4mm) Outline Dimensions

unit: inches/mm




| Symbol | Dimensions in inches | Dimensions in mm |
|---|---|---|
| A | 0.049 Max. | 1.25 Max. |
| $A_1$ | 0.002 Min. | 0.05 Min. |
| $A_2$ | 0.039±0.002 | 1.00±0.05 |
| b | 0.008±0.001 | 0.20±0.03 |
| c | 0.006±0.0003 | 0.15±0.008 |
| E | 0.315±0.004 | 8.00±0.10 |
| e | 0.020 TYP. | 0.50 TYP. |
| D | 0.528±0.008 | 13.40±0.20 |
| $D_1$ | 0.465±0.004 | 11.80±0.10 |
| L | 0.02±0.008 | 0.50±0.20 |
| $L_E$ | 0.0266 Min. | 0.675 Min. |
| S | 0.0109 TYP. | 0.278 TYP. |
| y | 0.004 Max. | 0.10 Max. |
| θ | 0° ~ 6° | 0° ~ 6° |

**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension $e_1$ is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.