

LH5332600

CMOS 32M (4M × 8/2M × 16) MROM

FEATURES

- 4,194,304 × 8 bit organization
(Byte mode: $\overline{\text{BYTE}} = V_{\text{IL}}$)
2,097,152 × 16 bit organization
(Word mode: $\overline{\text{BYTE}} = V_{\text{IH}}$)
- Access time: 100 ns (MAX.)
- Supply current:
 - Operating: 100 mA (MAX.)
 - Standby: 100 μA (MAX.)
- TTL compatible I/O
- Three-state output
- Single +5 V power supply
- Static operation
- Packages:
 - 44-pin, 600-mil SOP
 - 48-pin, 12 mm × 18 mm² TSOP (Type I)
- Others:
 - Non programmable
 - Not designed or rated as radiation hardened
 - CMOS process (P type silicon substrate)

DESCRIPTION

The LH5332600 is a 32M-bit mask-programmable ROM organized as 4,194,304 × 8 bits (Byte mode) or 2,097,152 × 16 bits (Word mode) that can be selected by a $\overline{\text{BYTE}}$ input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

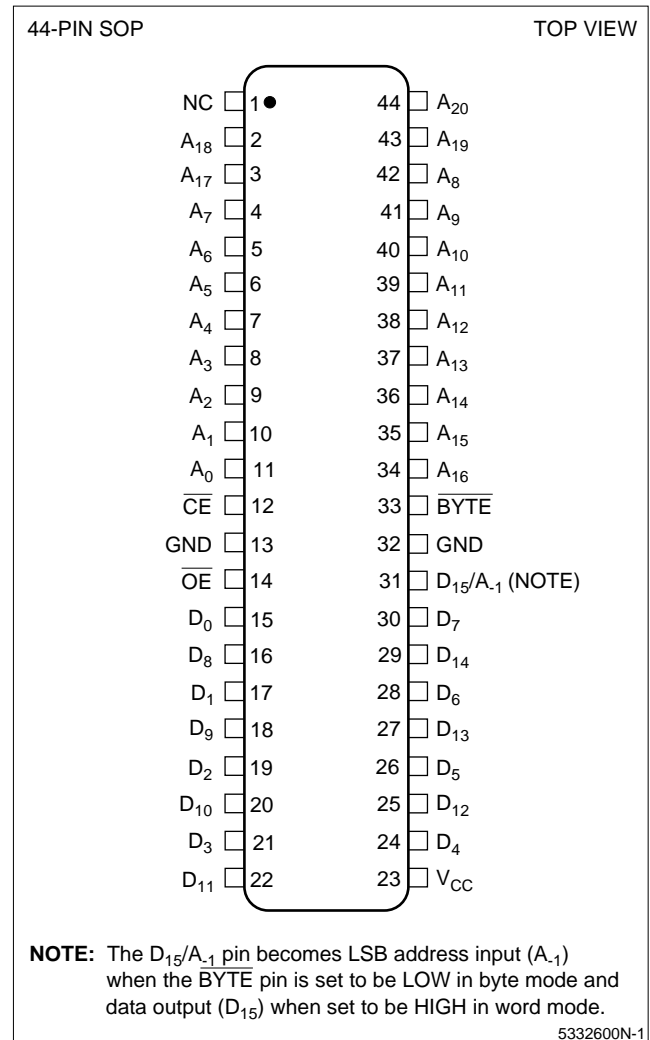


Figure 1. SOP Pin Connections

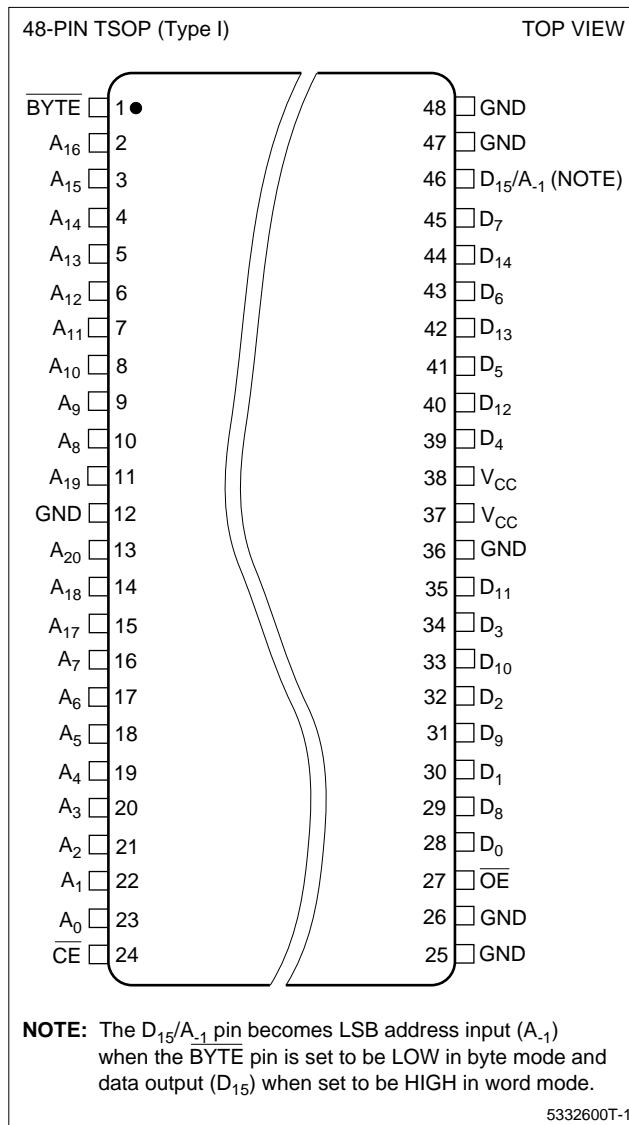
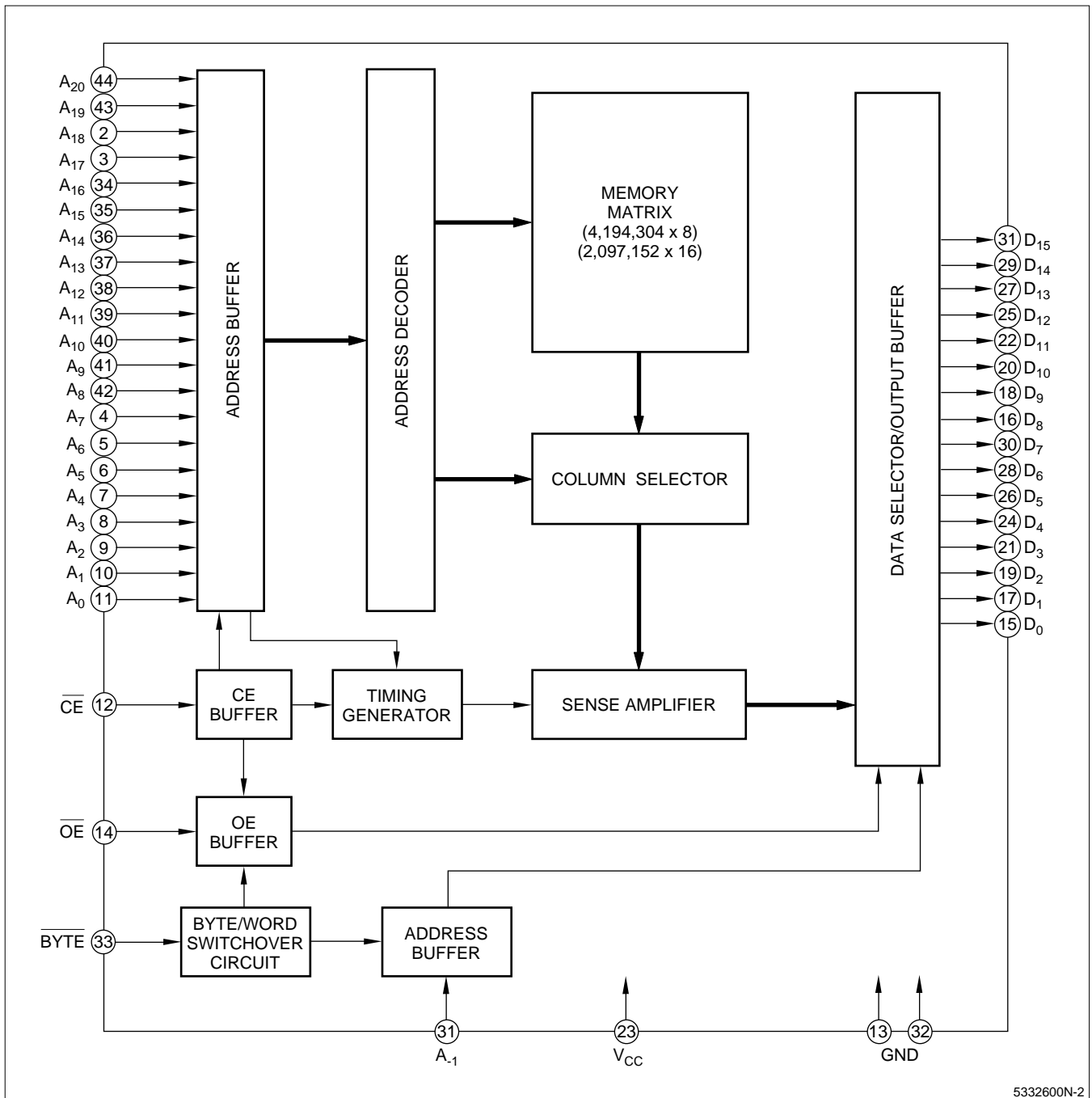


Figure 2. TSOP Pin Connections



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Figure 3. LH5332600 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A ₋₁ - A ₂₀	Address input
D ₀ - D ₁₅	Data output
BYTE	×8bit / ×16 bit (byte/word) mode select input
CE	Chip enable input

SIGNAL	PIN NAME
OE	Output enable input
V _{CC}	Power supply
GND	Ground
NC	No connection (Non wire bonding)

TRUTH TABLE

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{BYTE}}$	A-1 (D ₁₅)	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
				D ₀ - D ₇	D ₈ - D ₁₅	LSB	MSB	
H	X	X	X	High-Z	High-Z	—	—	Standby (I _{SB})
L	H	X	X	High-Z	High-Z	—	—	Operating
L	L	H	—	D ₀ - D ₇	D ₈ - D ₁₅	A ₀	A ₂₀	Operating
L	L	L	L	D ₀ - D ₇	High-Z	A-1	A ₂₀	Operating
L	L	L	H	D ₈ - D ₁₅	High-Z	A-1	A ₂₀	Operating

NOTES:

X = Don't care; High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V _{CC}	-0.3 to +7.0	V
Input voltage	V _{IN}	-0.3 to V _{CC} + 0.3	V
Output voltage	V _{OUT}	-0.3 to V _{CC} + 0.3	V
Operating temperature	T _{OPR}	0 to +70	°C
Storage temperature	T _{STG}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	4.5	5.0	5.5	V

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V _{IH}	—	2.2	V _{CC} + 0.3	V	—
Input 'Low' voltage	V _{IL}	—	-0.3	0.8	V	—
Output 'High' voltage	V _{OH}	I _{OH} = -400 μA	2.4	—	V	—
Output 'Low' voltage	V _{OL}	I _{OL} = 2.0 mA	—	0.4	V	—
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}	—	10	μA	—
Output leakage current	I _{LO}	V _{OUT} = 0 V to V _{CC}	—	10	μA	1
Operating current	I _{CC1}	t _{RC} = 100 ns	—	100	mA	2
	I _{CC2}	t _{RC} = 1 μs	—	90		
Standby current	I _{SB1}	CE = V _{IH}	—	2	mA	—
	I _{SB2}	CE = V _{CC} - 0.2 V	—	100		
Input capacitance	C _{IN}	f = 1 MHz, T _A = 25°C	—	10	pF	—
Output capacitance	C _{OUT}		—	10		

NOTES:

1. CE = V_{IH}, OE = V_{IH}
2. V_{IN} = V_{IH} or V_{IL}, CE = V_{IL}, output is open

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t _{RC}	100	—	ns	—
Address access time	t _{AA}	—	100	ns	—
Chip enable access time	t _{ACE}	—	100	ns	—
Output enable delay time	t _{OE}	—	50	ns	—
Output hold time	t _{OH}	5	—	ns	—
Output floating time	t _{CHZ}	—	40	ns	1
	t _{OHZ}	—	40	ns	

NOTE:

1. Determined by the time for the output to be opened. (Irrespective of output voltage)

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.4 V to 2.6 V
Input rise/fall time	10 ns
Input signal fall time	10 ns
Input reference level	1.5 V
Output reference level	1.5 V
Output load condition	1TTL + 100 pF

CAUTION

It is recommended that a decoupling capacitor be connected between V_{CC} and GND-Pin.

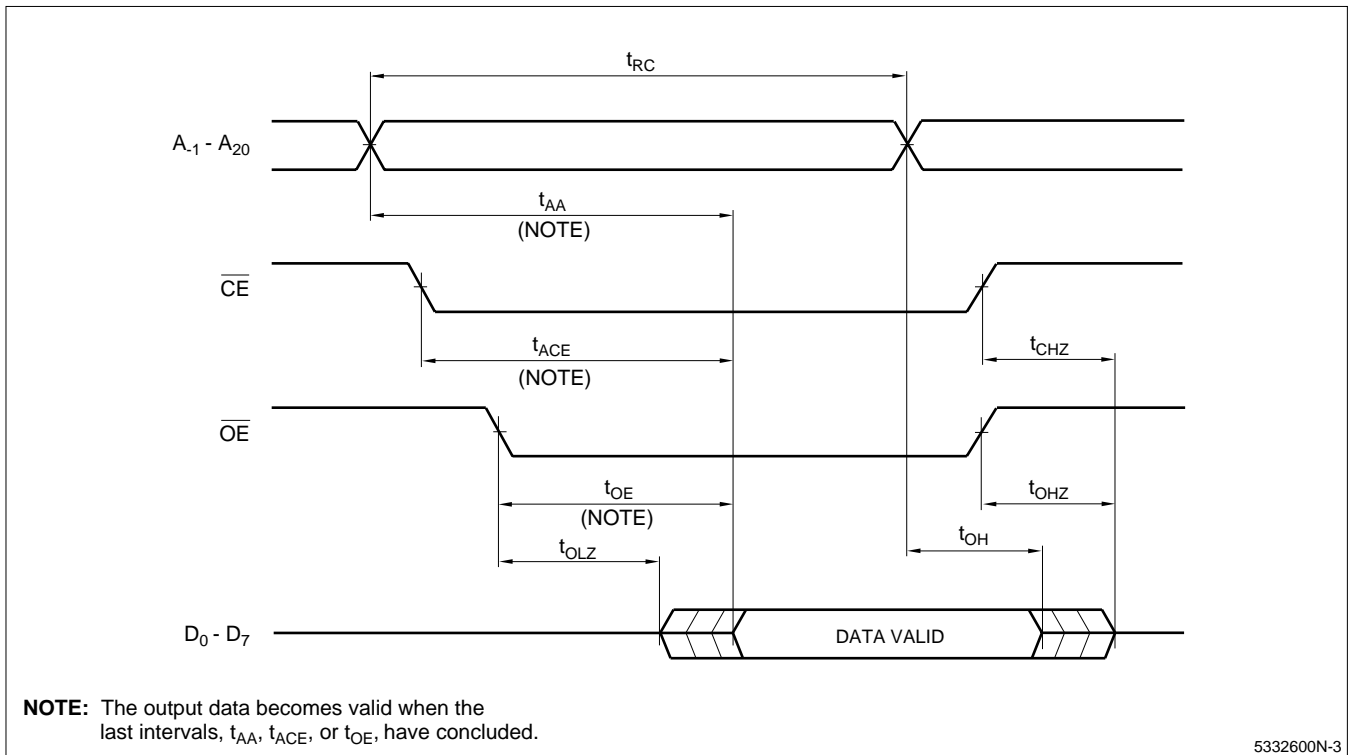


Figure 4. Byte Mode (BYTE = V_{IL})

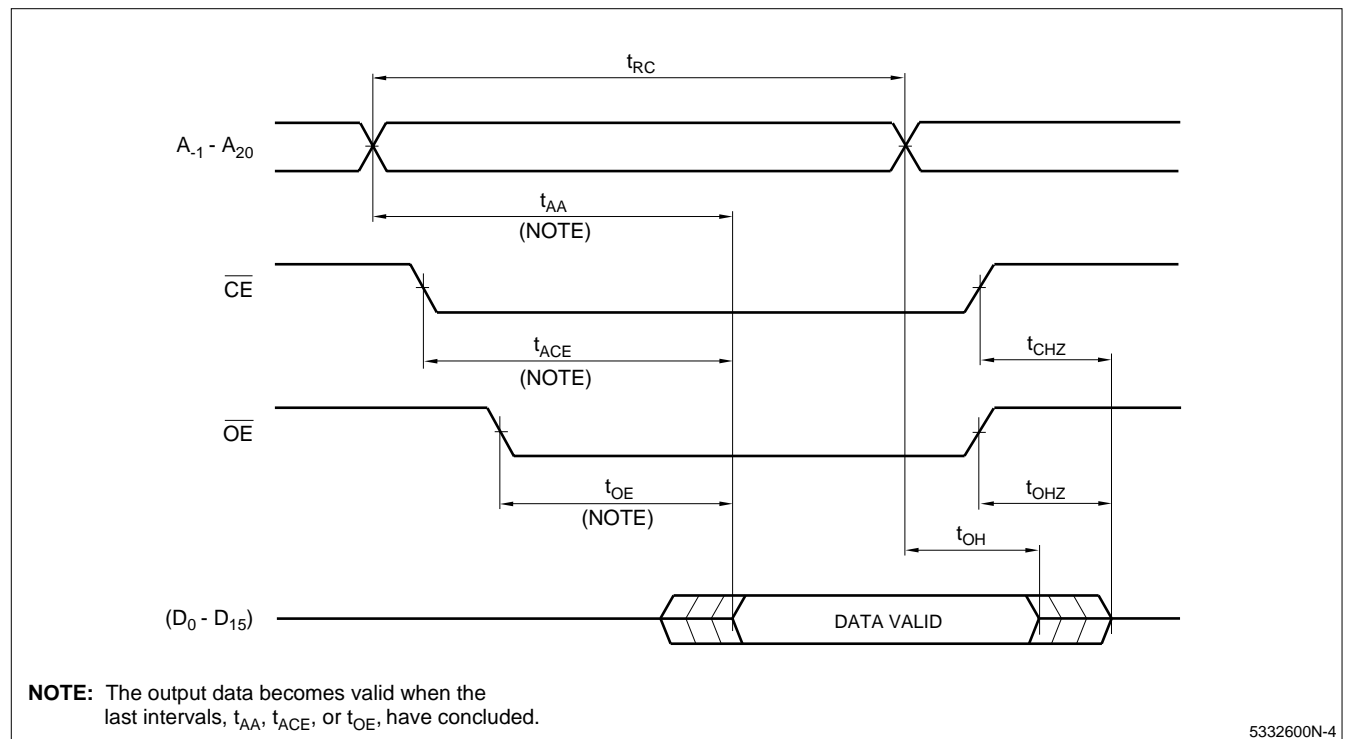
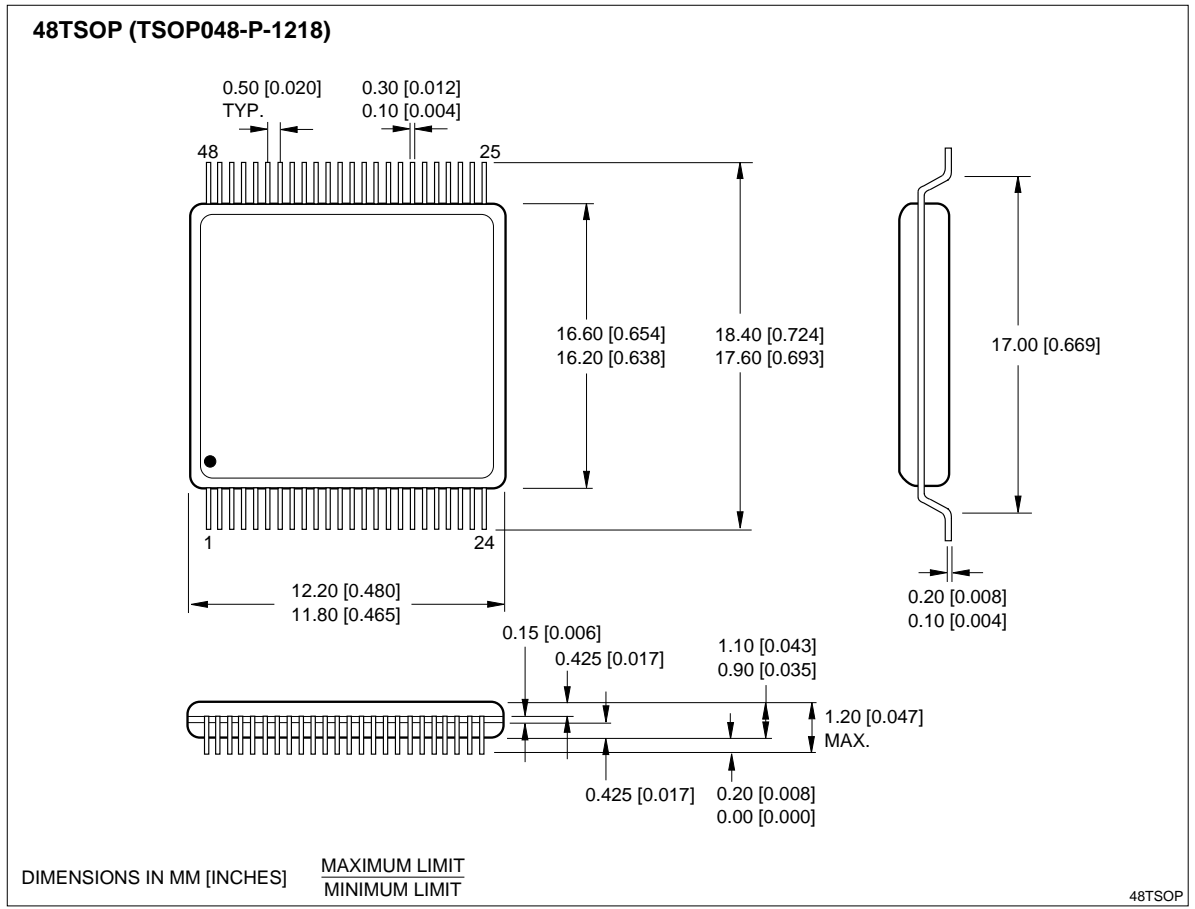
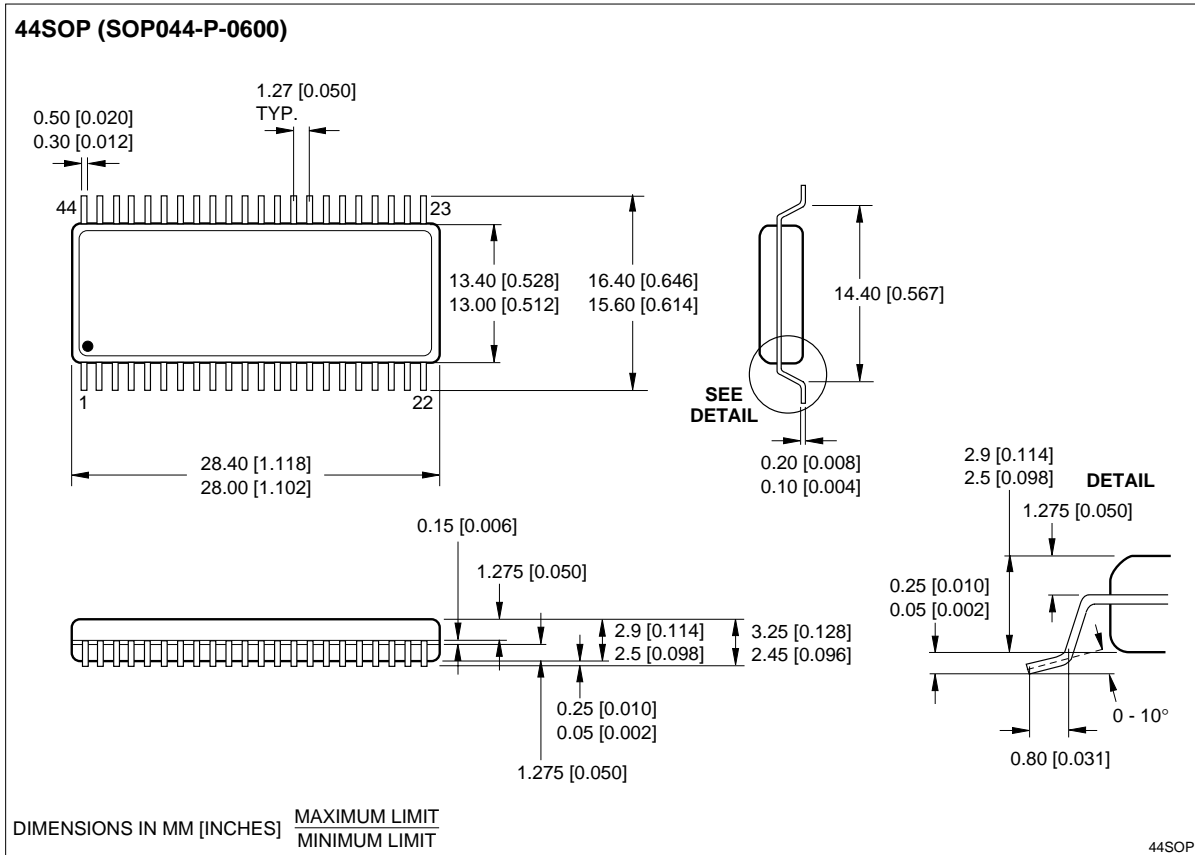


Figure 5. Word Mode (BYTE = V_{IH})

PACKAGE DIAGRAM



ORDERING INFORMATION

LH5332600
Device Type

X
Package

- N 44-pin, 600-mil SOP (SOP044-P-0600)
- T 48-pin, 12 mm x 18 mm² TSOP (Type I) (TSOP048-P-1218)

CMOS 32M (4M x 8 or 2M x 16) Mask-Programmable ROM

Example: LH5332600N (CMOS 32M (4M x 8 or 2M x 16) Mask-Programmable ROM, 44-pin, 600-mil SOP)

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