

# LH52D1000

CMOS 1M (128K × 8) Static Ram

## FEATURES

- Access time: 85 ns (MAX.),  
100 ns (MAX.)
- Current consumption:  
Operating: 40 mA (MAX.)  
6 mA (MAX.) ( $t_{RC}$ ,  $t_{WC} = 1 \mu s$ )  
Standby: 45  $\mu A$  (MAX.)
- Data Retention:  
1.0  $\mu A$  (MAX.  $V_{CCDR} = 3 V$ ,  $t_A = 25^\circ C$ )
- Single power supply: 2.7 V to 3.6 V
- Operating temperature:  $-40^\circ C$  to  $+85^\circ C$
- Fully-static operation
- Three-state output
- Not designed or rated as radiation hardened
- Packages:  
32-pin  $8 \times 20 \text{ mm}^2$  TSOP  
32-pin  $8 \times 13.4 \text{ mm}^2$  STSOP
- N-type bulk silicon

## DESCRIPTION

The LH52D1000 is a static RAM organized as  $131,072 \times 8$  bits which provides low-power standby mode. It is fabricated using silicon-gate CMOS process technology.

## PIN CONNECTIONS

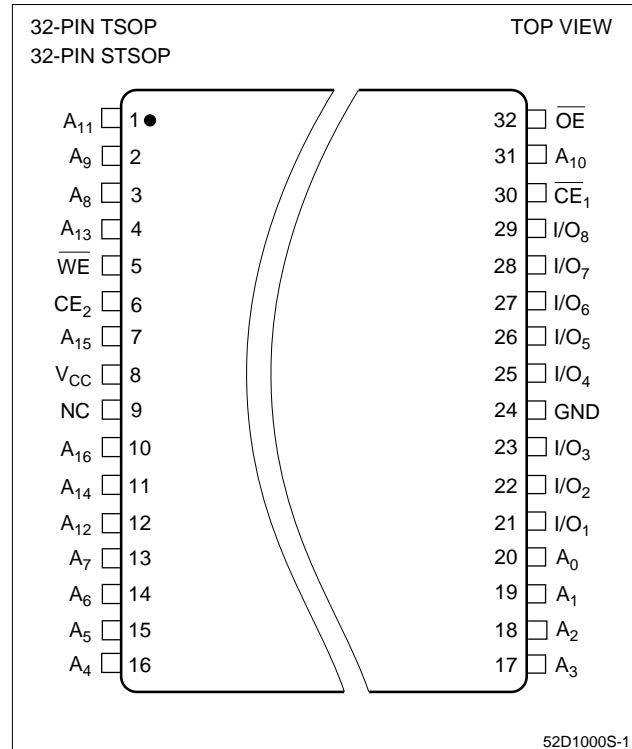


Figure 1. Pin Connections for TSOP and STSOP Packages

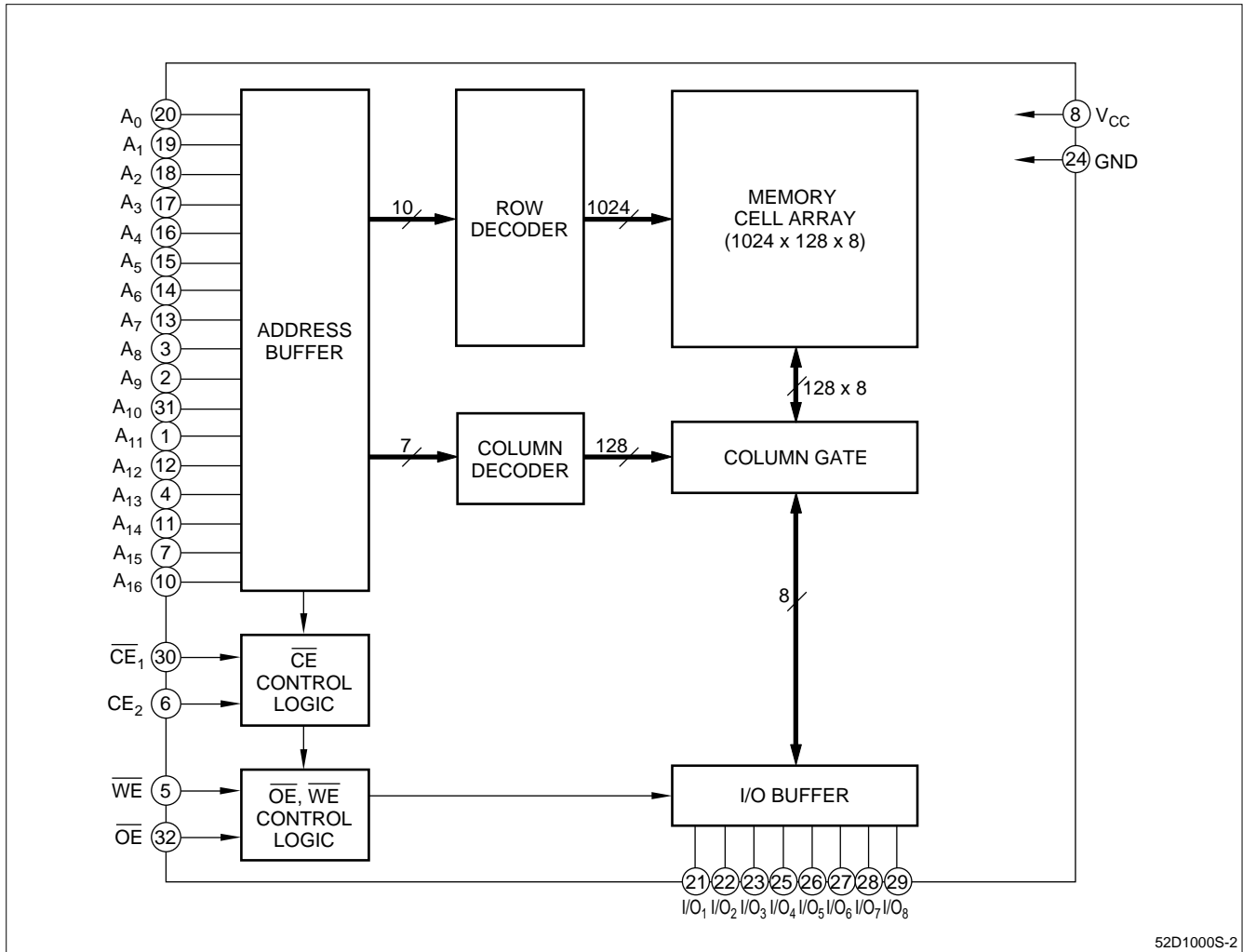


Figure 2. LH52D1000 Block Diagram

**PIN DESCRIPTION**

SIGNAL	PIN NAME
A <sub>0</sub> – A <sub>16</sub>	Address inputs
CE <sub>1</sub>	Chip enable 1
CE <sub>2</sub>	Chip enable 2
WE	Write enable
OE	Output enable

SIGNAL	PIN NAME
I/O <sub>1</sub> – I/O <sub>8</sub>	Data inputs and outputs
V <sub>CC</sub>	Power supply
GND	Ground
NC	No connection

## TRUTH TABLE

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	MODE	I/O <sub>1</sub> – I/O <sub>8</sub>	SUPPLY CURRENT	NOTE
H	—	—	—	Standby	High impedance	Standby (I <sub>SB</sub> )	1
—	L	—	—				
L	H	L	—	Write	Data input	Active (I <sub>CC</sub> )	1
L	H	H	L	Read	Data output	Active (I <sub>CC</sub> )	—
L	H	H	H	Output disable	High impedance	Active (I <sub>CC</sub> )	—

## NOTE:

- = Don't care  
L = Low  
H = High

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V <sub>CC</sub>	-0.3 to +4.6	V	1
Input voltage	V <sub>IN</sub>	-0.3 to V <sub>CC</sub> + 0.3	V	1, 2
Operating temperature	T <sub>OPR</sub>	-40 to +85	°C	—
Storage temperature	T <sub>STG</sub>	-55 to +150	°C	—

## NOTE:

- The maximum applicable voltage on any pin with respect to GND.
- Undershoot of -3.0 V is allowed width of pulse below 50 ns.

RECOMMENDED DC OPERATING CONDITIONS (T<sub>A</sub> = -40°C to +85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V <sub>CC</sub>	2.7	3.0	3.6	V	—
Input voltage	V <sub>IH</sub>	2.0	—	V <sub>CC</sub> + 0.3	V	—
	V <sub>IL</sub>	-0.3	—	0.6	V	1

## NOTE:

- Undershoot of -3.0 V is allowed width of pulse below 50 ns.

DC ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = -25°C to +85°C, V<sub>CC</sub> = 2.7 V to 3.6 V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = 0 to V <sub>CC</sub>	-1.0	—	1.0	μA
Output leakage current	I <sub>LO</sub>	CE <sub>1</sub> = V <sub>IH</sub> or CE <sub>2</sub> = V <sub>IL</sub> or OE = V <sub>IH</sub> or WE = V <sub>IL</sub> V <sub>IO</sub> = 0 V to V <sub>CC</sub>	-1.0	—	1.0	μA
Operating supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , CE <sub>1</sub> = V <sub>IL</sub> , WE = V <sub>IH</sub> CE <sub>2</sub> = V <sub>IH</sub> , I <sub>IO</sub> = 0 mA	—	—	40	mA
	I <sub>CC1</sub>	CE <sub>1</sub> = 0.2 V, V <sub>IN</sub> = 0.2 V or V <sub>CC</sub> - 0.2 V CE <sub>2</sub> , WE = V <sub>CC</sub> - 0.2 V, I <sub>IO</sub> = 0 mA	—	—	6	
Standby current	I <sub>SB</sub>	CE <sub>1</sub> = V <sub>CC</sub> - 0.2 V or CE <sub>2</sub> = 0.2 V	—	—	45	μA
	I <sub>SB1</sub>	CE <sub>1</sub> = V <sub>IH</sub> or CE <sub>2</sub> = V <sub>IL</sub>	—	—	2.0	mA
Output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA	—	—	0.4	V
	V <sub>OH</sub>	I <sub>OH</sub> = -0.5 mA	V <sub>CC</sub> - 0.5	—	—	V

## AC ELECTRICAL CHARACTERISTICS

### AC Test Conditions

PARAMETER	MODE	NOTE
Input pulse level	0.4 V to 2.4 V	—
Input rise and fall time	5 ns	—
Input and output timing Ref. level	1.5 V	—
Output load	100 pF + 1TTL	1

**NOTE:**

- Including scope and jig capacitance.

### READ CYCLE ( $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ , $V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$ )

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	$t_{RC}$	85		ns	—
Address access time	$t_{AA}$	—	85	ns	—
CE <sub>1</sub> access time	$t_{ACE1}$	—	85	ns	—
CE <sub>2</sub> access time	$t_{ACE2}$	—	85	ns	—
Output enable to output valid	$t_{OE}$	—	45	ns	—
Output hold from address change	$t_{OH}$	10	—	ns	—
CE <sub>1</sub> Low to output active	$t_{LZ1}$	5	—	ns	1
CE <sub>2</sub> High to output active	$t_{LZ2}$	5	—	ns	1
OE Low to output active	$t_{OLZ}$	0	—	ns	1
CE <sub>1</sub> High to output in High impedance	$t_{HZ1}$	0	35	ns	1
CE <sub>2</sub> Low to output in High impedance	$t_{HZ2}$	0	35	ns	1
OE High to output in High impedance	$t_{OHZ}$	0	35	ns	1

**NOTE:**

- Active output to High impedance and High impedance to output active tests specified for a  $\pm 200\text{ mV}$  transition from steady state levels into the test load.

### WRITE CYCLE ( $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ , $V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$ )

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Write cycle time	$t_{WC}$	85	—	ns	—
CE <sub>1</sub> Low to end of write	$t_{CW1}$	75	—	ns	—
CE <sub>2</sub> High to end of write	$t_{CW2}$	75	—	ns	—
Address setup time	$t_{AS}$	0	—	ns	—
Write pulse width	$t_{WP}$	60	—	ns	—
Write recovery time	$t_{WR}$	0	—	ns	—
Input data setup time	$t_{DW}$	35	—	ns	—
Input data hold time	$t_{DH}$	0	—	ns	—
WE High to output active	$t_{OW}$	0	—	ns	1
WE Low to output in High impedance	$t_{WZ}$	0	—	ns	1
OE High to output in High impedance	$t_{OHZ}$	0	35	ns	1

**NOTE:**

- Active output to High impedance and High impedance to output active tests specified for a  $\pm 200\text{ mV}$  transition from steady state levels into the test load.

**DATA RETENTION CHARACTERISTICS ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )**

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP	MAX.	UNIT	NOTE
Data retention supply voltage	$V_{CCDR}$	$CE_2 \leq 0.2\text{ V}$ or $CE_1 \geq V_{CCDR} - 0.2\text{ V}$	2.0	—	3.6	V	1
Data retention supply current	$I_{CCDR}$	$V_{CCDR} = 3.0\text{ V}$ $CE_2 \leq 0.2\text{ V}$ or $CE_1 \geq V_{CCDR} - 0.2\text{ V}$					
			$T_A = 25^{\circ}\text{C}$	—	—	1.0	$\mu\text{A}$ 1
			$T_A = 40^{\circ}\text{C}$	—	—	3.0 35	
Chip enable setup time	$t_{CDR}$	—	0	—	—	ms	—
Chip enable hold time	$t_R$	—	5	—	—	ms	—

**NOTE:**

- $CE_2 \geq V_{CCDR} - 0.2\text{ V}$  or  $CE_2 \leq 0.2\text{ V}$
- Typical values at  $T_A = 25^{\circ}\text{C}$

**PIN CAPACITANCE ( $T_A = 25^{\circ}\text{C}$ ,  $f = 1\text{ MHz}$ )**

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input capacitance	$C_{IN}$	$V_{IN} = 0\text{ V}$	—	—	10	pF	1
I/O capacitance	$C_{I/O}$	$V_{I/O} = 0\text{ V}$	—	—	10	pF	1

**NOTE:**

- This parameter is sampled and not production tested.

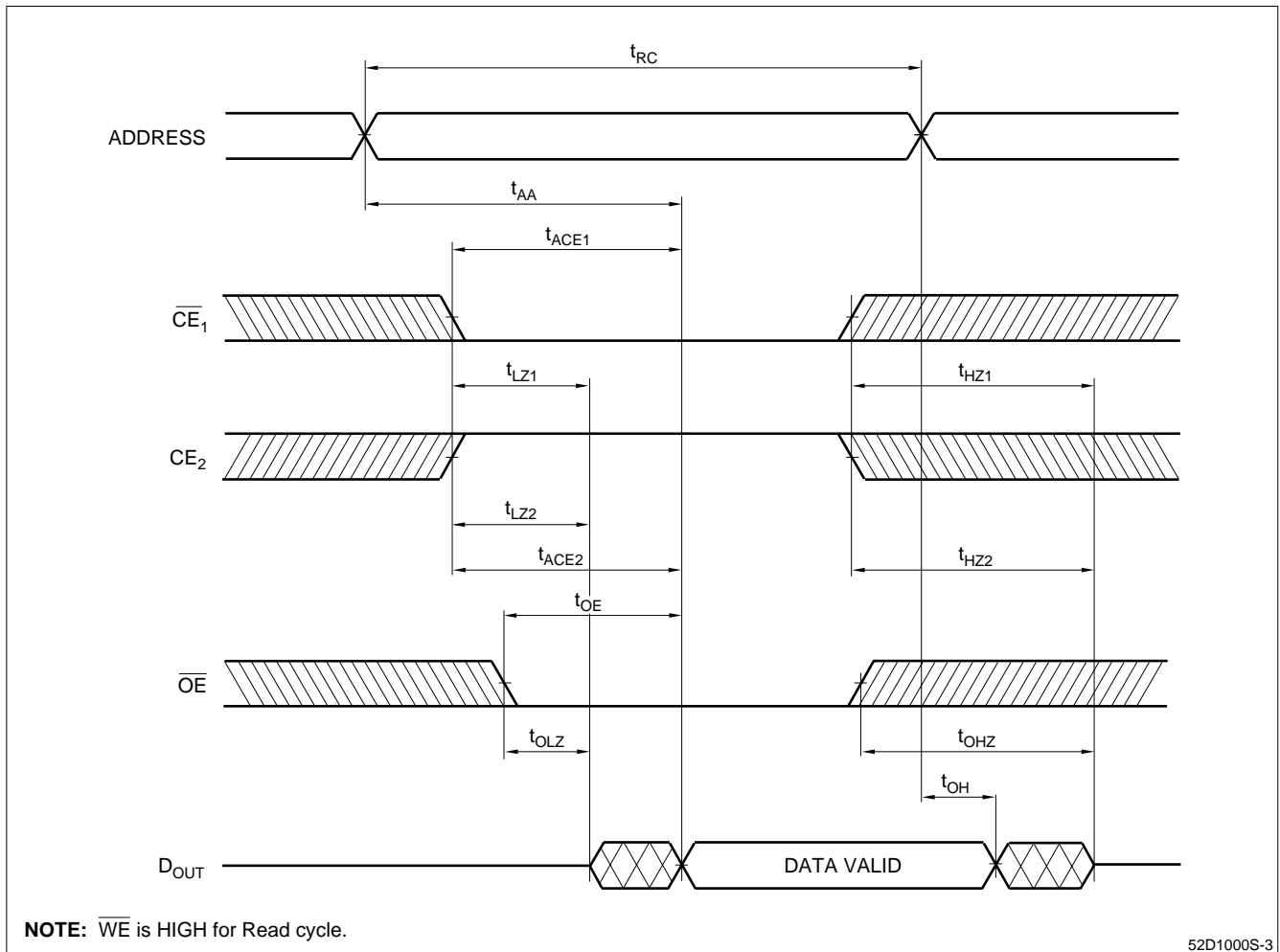
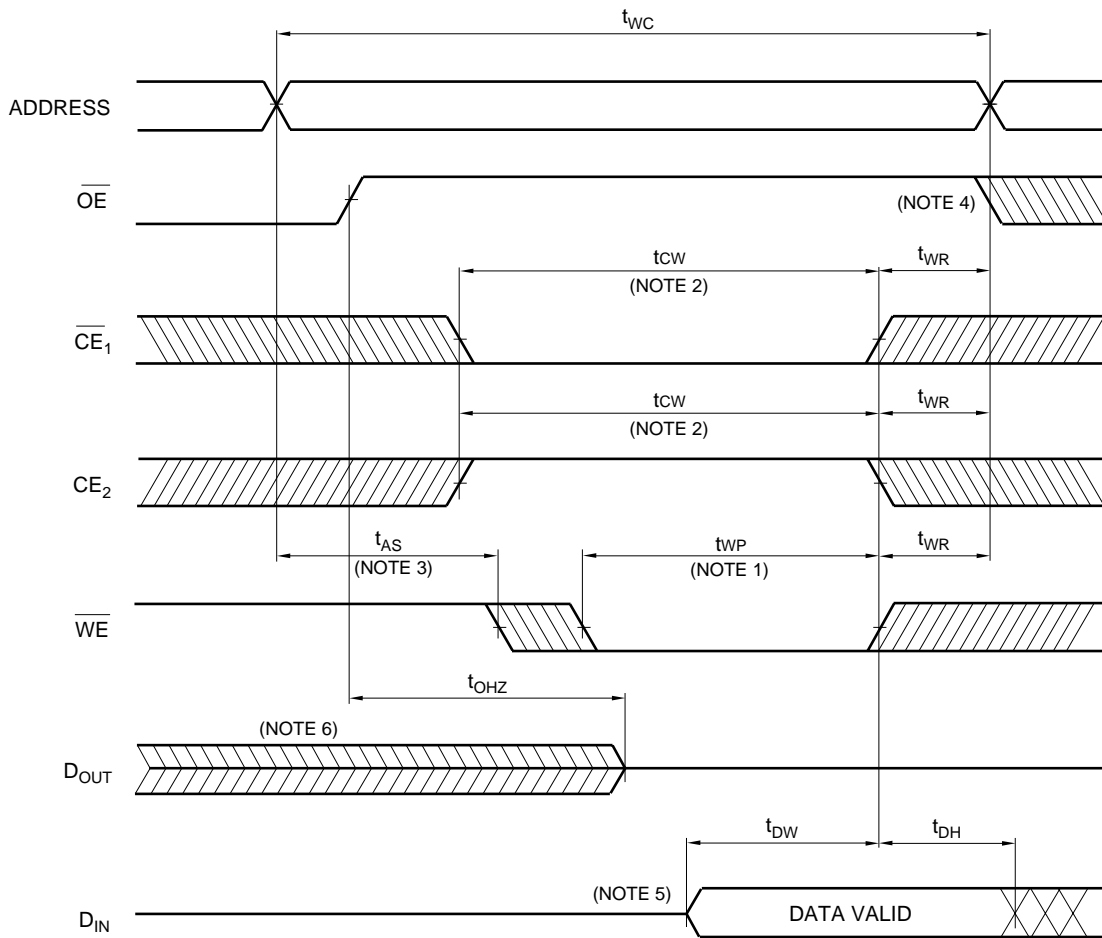


Figure 3. Read Cycle

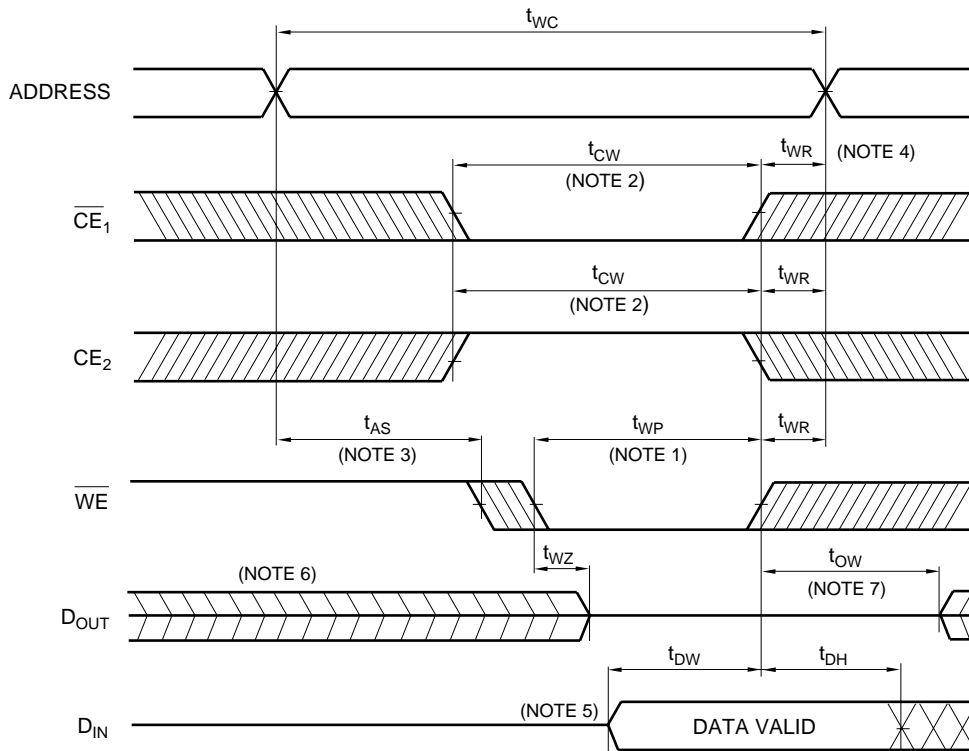


**NOTES:**

1. A write occurs during the overlap of a LOW  $\overline{CE}_1$ , a HIGH  $CE_2$  and a LOW  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CE}_1$  going LOW,  $CE_2$  going HIGH and  $\overline{WE}$  going LOW. A write ends at the earliest transition among  $\overline{CE}_1$  going HIGH,  $CE_2$  going LOW and  $\overline{WE}$  going HIGH.  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the later of  $\overline{CE}_1$  going LOW or  $CE_2$  going HIGH to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR1}$  applies in case a write ends at  $\overline{CE}_1$  or  $\overline{WE}$  going HIGH.  $t_{WR2}$  applies in case a write ends at  $CE_2$  going LOW.
5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. If  $\overline{CE}_1$  goes LOW simultaneously with  $\overline{WE}$  going LOW or after  $\overline{WE}$  going LOW, the outputs remain in high impedance state.
7. If  $\overline{CE}_1$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH or before  $\overline{WE}$  going HIGH, the outputs remain in high impedance state.

52D1000S-4

**Figure 4. Write Cycle (OE Controlled)**



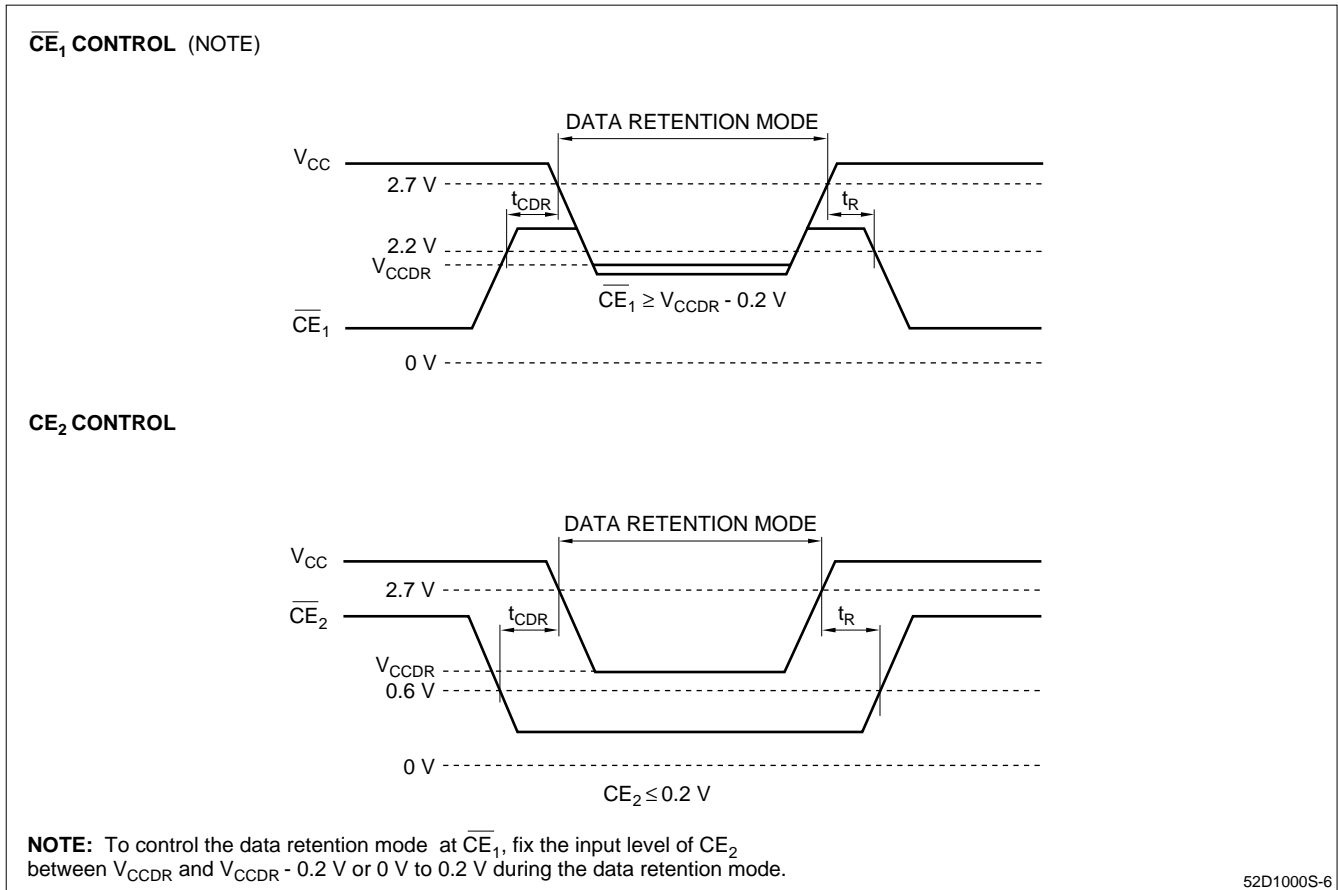
**NOTES:**

1. A write occurs during the overlap of a LOW  $\overline{CE}_1$ , a HIGH  $CE_2$  and a LOW  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CE}_1$  going LOW,  $CE_2$  going HIGH and  $\overline{WE}$  going LOW. A write ends at the earliest transition among  $\overline{CE}_1$  going HIGH,  $CE_2$  going LOW and  $\overline{WE}$  going HIGH.  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the later of  $\overline{CE}_1$  going LOW or  $CE_2$  going HIGH to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR1}$  applies in case a write ends at  $\overline{CE}_1$  or  $\overline{WE}$  going HIGH.  $t_{WR2}$  applies in case a write ends at  $CE_2$  going LOW.
5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. If  $\overline{CE}_1$  goes LOW simultaneously with  $\overline{WE}$  going LOW or after  $\overline{WE}$  going LOW, the outputs remain in high impedance state.
7. If  $\overline{CE}_1$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH or before  $\overline{WE}$  going HIGH, the outputs remain in high impedance state.

52D1000S-5

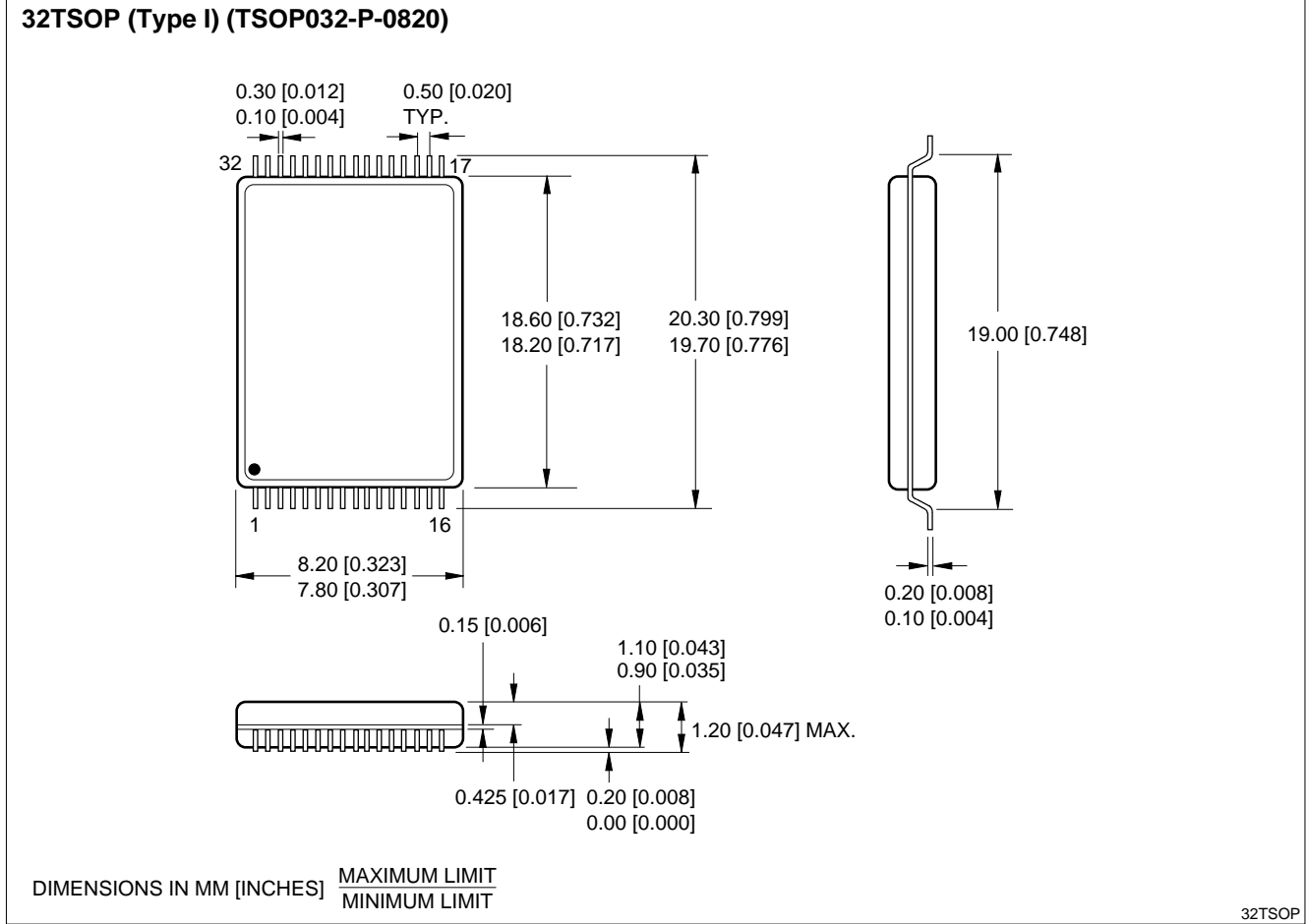
**Figure 5. Write Cycle ( $\overline{OE}$  Low Fixed)**



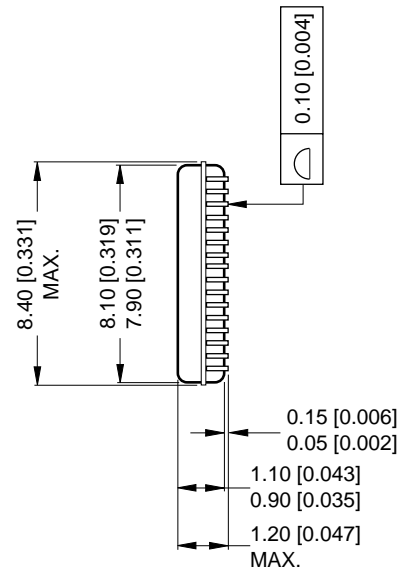
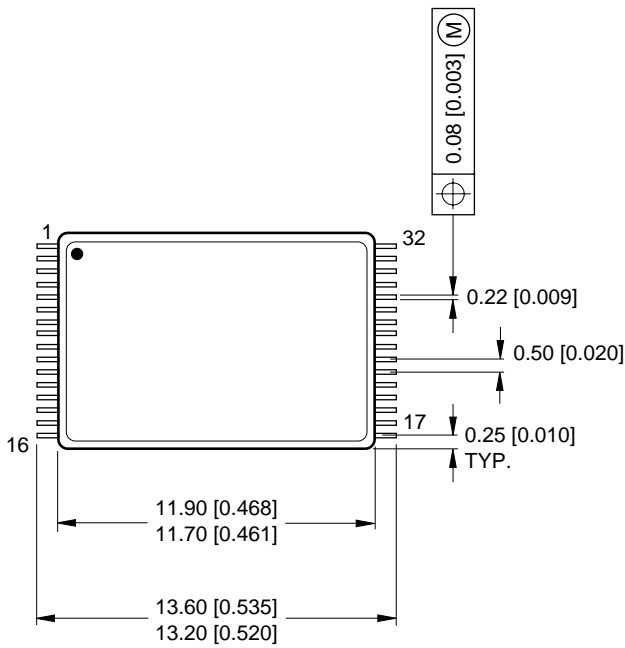


**Figure 6. Data Retention  
( $\overline{CE}_1$  Controlled)**

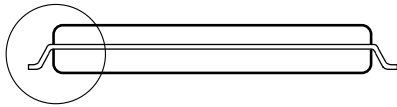
PACKAGE DIAGRAM



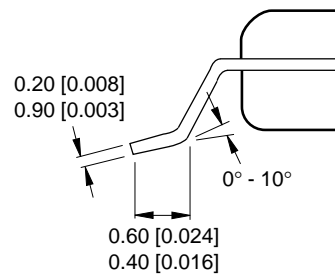
32TSOP (TSOP032-P-0813)



SEE DETAIL



DETAIL

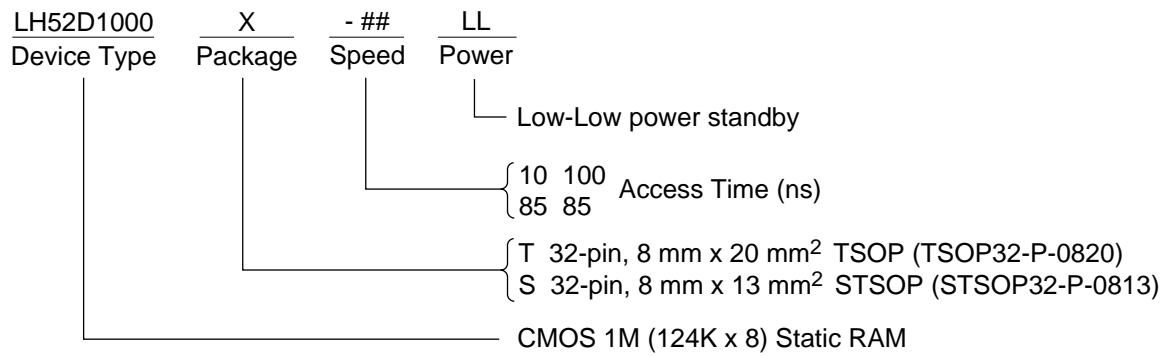


DIMENSIONS IN MM [INCHES] 

MAXIMUM LIMIT
MINIMUM LIMIT

32STSOP

## ORDERING INFORMATION



**Example:** LH52D1000T-85LL (CMOS 1M (124K x 8) Static RAM, 85 ns, Low-Low power standby, 32-pin TSOP)

52D1000S-7