High Power Factor Flyback LED Controller with HV Start-up

REV. 01

General Description

The LD7838 is a 700V HV start-up active PFC Flyback controller, specially designed for LED lighting application. This device operates in transition or boundary mode and integrates with completed protections required. It minimizes the components counts in either SOP-7 package. Those make it easy to design with for cost-effective applications.

With High Voltage start-up technology, power factor correction and boundary mode switching control, the start-up time and resistor loss could be minimized efficiently. The circuit can easily achieve power factor is upper 0.92 to meet most of the international requirements as IEC61000-3-2 standard certifications.

With completed protection built inside this IC, such as over voltage protection (OVP), over current protection (OCP), over load protection (OLP), over temperature protection (OTP), and short circuit protection (SCP), pin open / short protection. It enables the circuit to meet most safety requirements in both normal and abnormal test

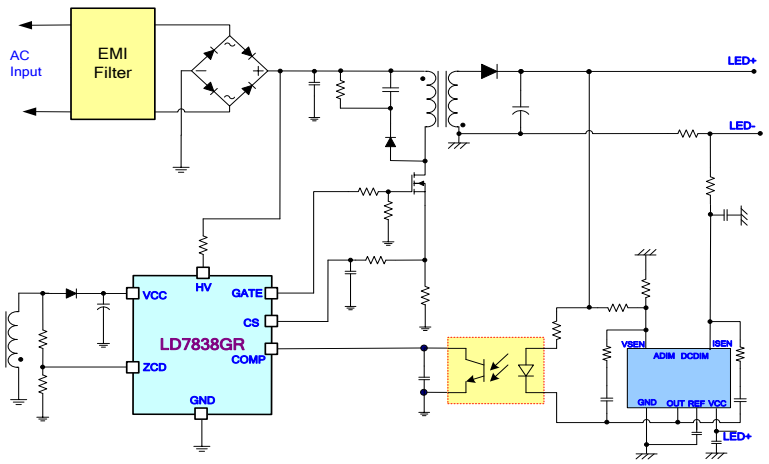
Features

- High voltage (700V) startup circuit by HV pin for 85~305V_{AC} input range
- High Power Factor (> 0.92)
- High-efficiency Transition mode operation
- Lower Power Saving (< 0.5W)
- Accurate OLP Compensation for High/ Low Line
- Built in BNI/ BNO Function
- Wide UVLO (16Von and 8 Voff) range
- Built in VCC Over Voltage Protection
- Built in Over Load Protection
- Adjustable Over Output Current Protection (Cycle by Cycle Current Limiting)
- Internal Over temperature protection

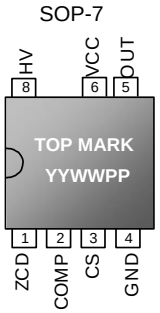
Applications

- Lighting Driver module
- Active Power Factor Correction Power Supply

Typical Application



Pin Configuration



YY: Year code
WW: Week code
PP: Production code

Ordering Information

Part number	Package	Top Mark	Shipping
LD7838	SOP-7	LD7838 GR	2500 /tape & reel

The LD7838 is ROHS compliant/ green packaged.

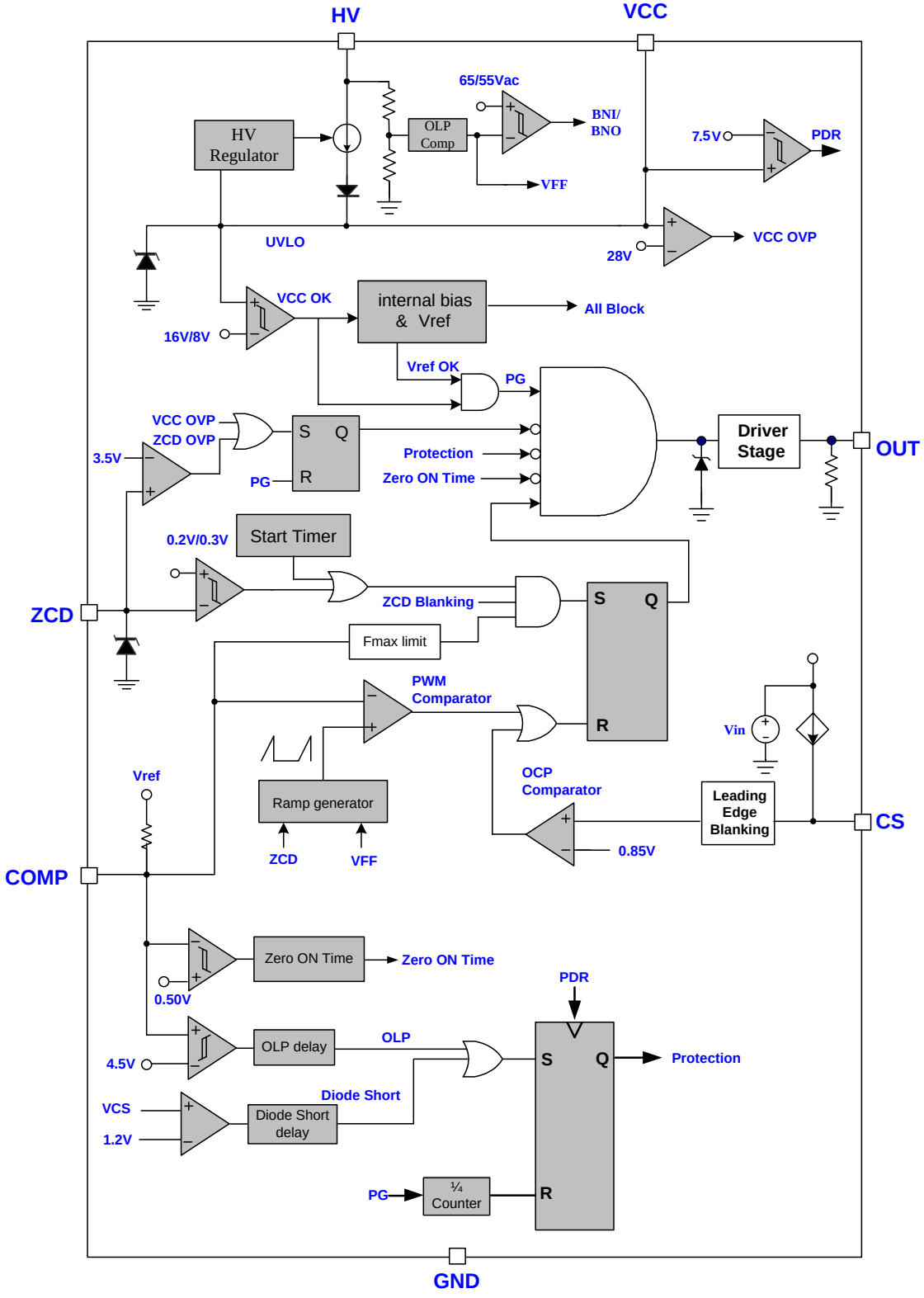
Protection Mode

Part number	BNI/BNO	VCC_OVP	ZCD_OVP	OLP/ output Short	Output diode Short
LD7838	Yes	Auto recovery	Auto recovery	Auto recovery	Auto recovery

Pin Descriptions

Pin	NAME	FUNCTION
1	ZCD	Quasi resonance detector and programmable maximum ON-time.
2	COMP	Feedback pin. Connect a photo-coupler to close the control loop to achieve regulation.
3	CS	Current sense pin, connect it to sense the MOSFET current for OCP
4	GND	Ground
5	OUT	Gate drive output to drive the external MOSFET
6	VCC	Power source VCC pin
8	HV	Connect this pin to positive terminal of main bulk cap to provide the startup current for controller. When Vcc is UVLO on, the HV loop will open and turn off internal current source to minimize the power loss.

Block Diagram



Absolute Maximum Ratings

Supply Voltage, VCC	-0.3V~30V
High voltage pin, HV	-0.3V~700V
OUT	-0.3V~VCC +0.3V
COMP, ZCD,CS	-0.3V~6V
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C ~ 150°C
Package Thermal Resistance (SOP-7, θ_{JA})	160°C/W
Power Dissipation (SOP-7, at Ambient Temperature = 85°C)	250mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (Except HV pin)	2.5KV
ESD Voltage Protection, Machine Model	250 V

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Supply VCC Voltage	9.5	27.5	V
VCC pin capacitor	4.7	22	μF
Operating Junction Temperature	-40	125	°C
Comp pin capacitor	0.22	4.7	μF
CS pin filter capacitance	100	680	pF
CS pin filter resistance	100	1k	Ω

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF~0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible.
2. The VCC capacitor is only for IC used and cannot parallel with other devices.
3. Connecting a capacitor to COMP pin is also essential to filter out the undesired switching noise for stable operation.
4. The small signal components should be placed close to IC pin as possible.

Electrical Characteristics

(V_{CC}=15.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
High voltage Supply(HV Pin)						
High-voltage current Source	HV = 180 V_{DC} V_{CC} = 4V	I_{HV}	1.5	1.8	2.1	mA
Off-state Leakage current	V_{CC} > V_{UV_ON},HV=500 V_{DC}	I_{HV_OFF}			30	μA
Brown-in Level	V_{CC} > V_{UV_ON}, ZCD = 0	V_{HVBI}		90	100	V_{DC}
HV Pin Hysteresis	V_{HVBI} - V_{HVBO}	ΔV_{HV}		10		V_{DC}
Supply Voltage (VCC Pin)						
Startup Current	V_{CC} < V_{UV_ON}	I_{ST}		75	95	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP} = 0V, ZCD = 0	I_{OP_LO}		1		mA
	V_{COMP} = 3V, ZCD = 0	I_{OP_HI}		1.5		mA
	V_{CC}/ ZCD OVP, OLP, CS short, Diode short	I_{OP_PRO}		0.3		mA
UVLO (OFF)		V_{UV_OFF}	7	8	9	V
UVLO (ON)		V_{UV_ON}	15	16	17	V
HV Self Bias		V_{LDO_LO}	9.1	9.8	10.5	V
De-Latch VCC Voltage	PDR(Power Down Reset)	V_{PDR}	6.8	7.5	8.2	V
VCC OVP Level		V_{CC_OVP}	27		29	V
VCC/ ZCD OVP De-bounce Time	*	T_{DEB_OVP}		250		μs
Voltage Feedback(Comp Pin)						
Short circuit current	V_{COMP}=0	I_{COMP}	0.4	0.5	0.6	mA
Open loop voltage		V_{CMP_OPEN}	5.0		5.8	V
Over load protection Trip Level		V_{OLP}	4.45	4.6	4.75	V
Zero ON-time Threshold		V_{CMP_ZOT}		0.5		V
Over load protection Delay Time	*	T_{DEB_OLP}		285		ms

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Zero Current Detector (ZCD Pin)						
Upper Clamp Voltage	I_{DET}=100μA	V_{ZH}	-	4.7	-	V
Lower Clamp Voltage	$I_{DET=}$-2mA	V_{ZL}	0		-0.3	V
Input Voltage Threshold		V_{ZCD}	0.15	0.2	0.25	V
	Hysteresis	VH_{ZCD}		0.1		V
Input bias current	V_{ZCD}=1V~4V, OUT is Low level	I_{ZCD_BIAS}	0.0		1.0	μA
ZCD OVP Threshold		V_{ZCD_OVP}	3.3	3.5	3.7	V
ZCD OVP De-bounce	*	T_{DEB_OVP}		250		μs
Minimum (ON+OFF)-Time						
Minimum (ON+OFF)-Time	Fmax(300kHz),	T_{F_MAX}		3.3		μs
Gate Drive Output (OUT Pin)						
Output Low Level	V_{CC}=15V, I_{SINK}=20mA	V_{G_LO}	0		0.5	V
Output High Level	V_{CC}=15V, I_{SOURCE}=20mA	V_{G_HI}	10		14	V
Rising Time	V_{CC} =15V, CL=1000pF(*)	T_{G_RISE}		250		ns
Falling Time	V_{CC} =15V, CL=1000pF(*)	T_{G_FALL}		50		ns
Current Sensing (CS Pin)						
Soft Start Time	*			10		ms
Leading edge blanking time	*			425		ns
Over Current Limit		V_{OCP_H}	0.8	0.85	0.9	*V*
OCP Compensation Current	I_{OCP}=1/500K*HV	I_{OCP}		200		μA/100V
Current Limit-2 for diode short protection		V_{OCP2}	1	1.2	1.4	V
Delay Time of Diode Short Protection	*	T_{DEB_DSP}		7		Times
Internal OTP (Over Temp. Protection)						
OTP Trip level	*			140		°C
OTP Hysteresis	*			30		°C

Note: (*) Guaranteed by Design.

Typical Performance Characteristics

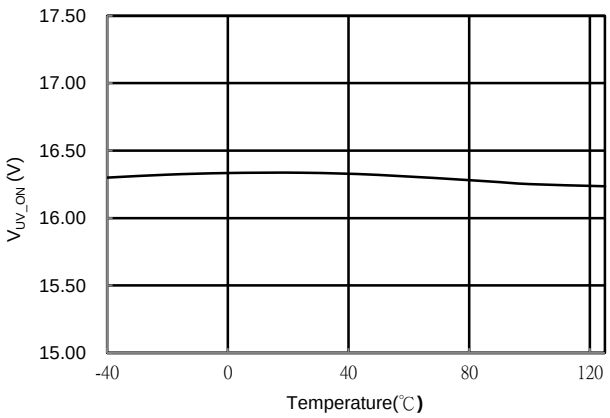


Fig. 1 V_{UV_ON} vs. Temperature

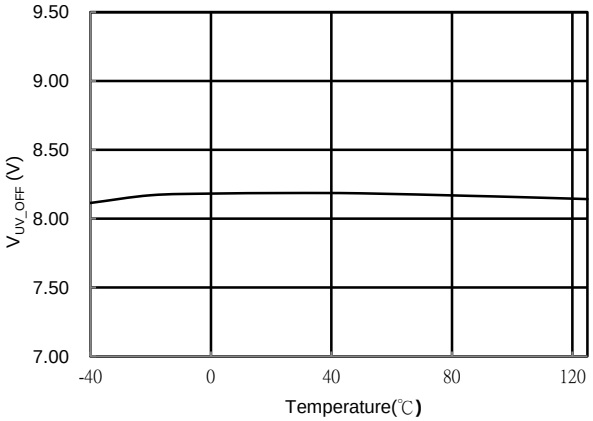


Fig. 2 V_{UV_OFF} vs. Temperature

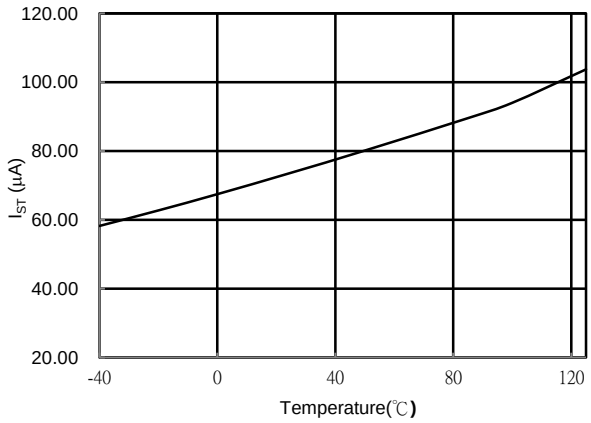


Fig. 3 I_{ST} vs. Temperature

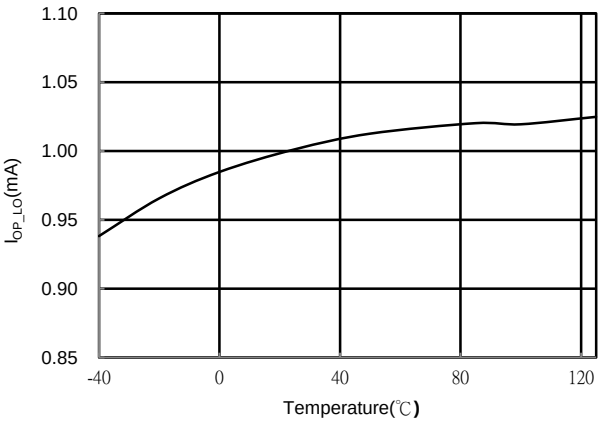


Fig. 4 I_{OP_LO} vs. Temperature

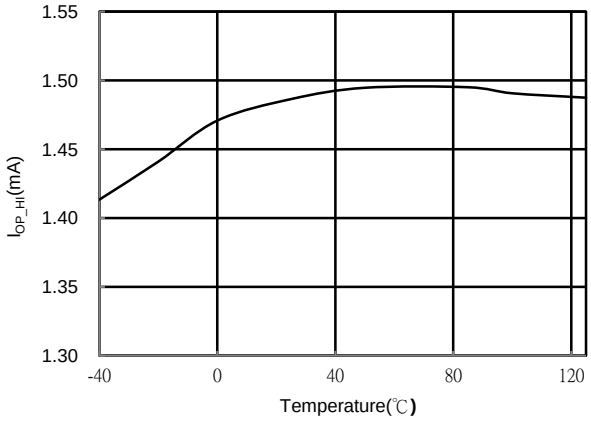


Fig. 5 I_{OP_HI} vs. Temperature

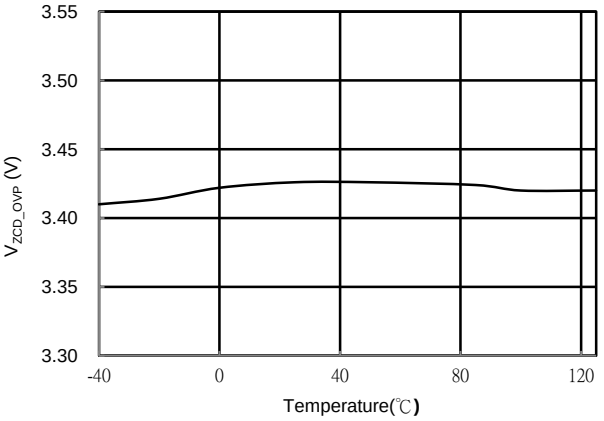


Fig. 6 V_{ZCD_OVP} vs. Temperature

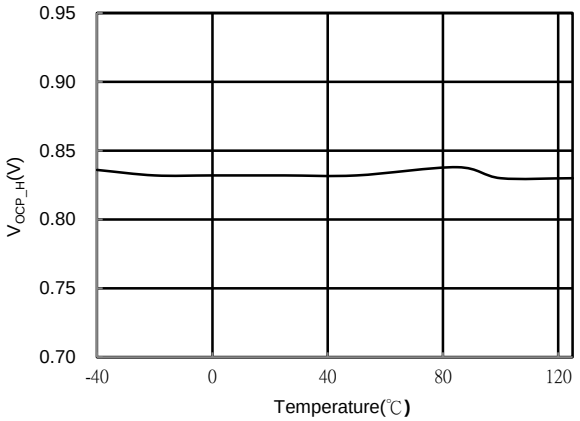


Fig. 7 V_{OCP_H} vs. Temperature

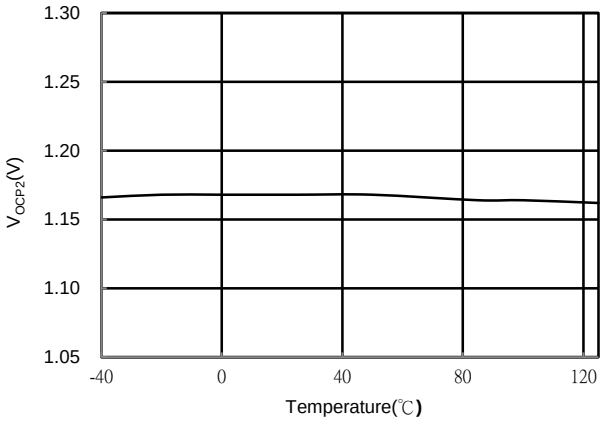


Fig. 8 V_{OCP2} vs. Temperature

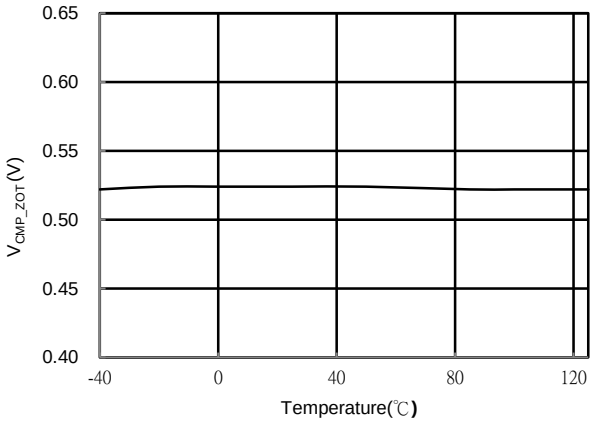


Fig. 9 V_{CMP_ZOT} vs. Temperature

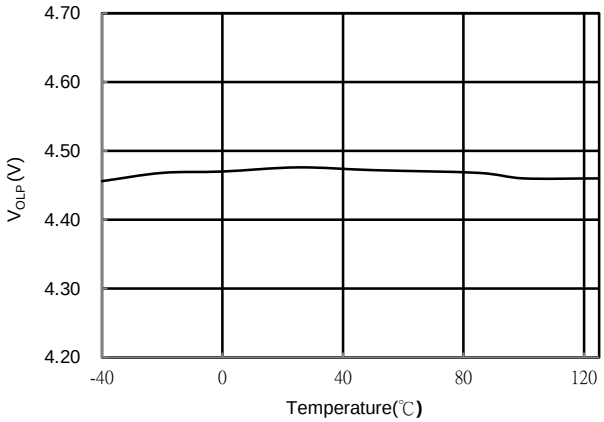


Fig. 10 V_{OLP} vs. Temperature

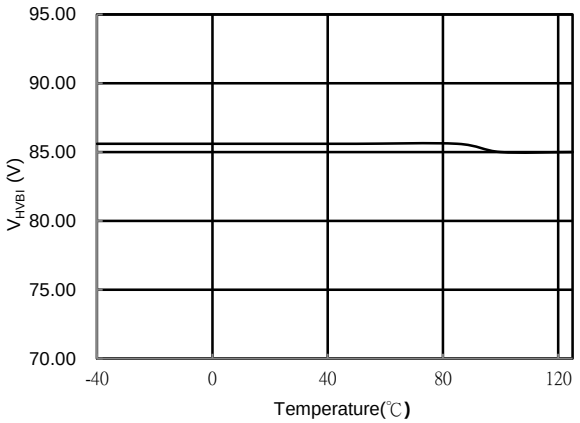


Fig. 11 V_{HVBI} vs. Temperature

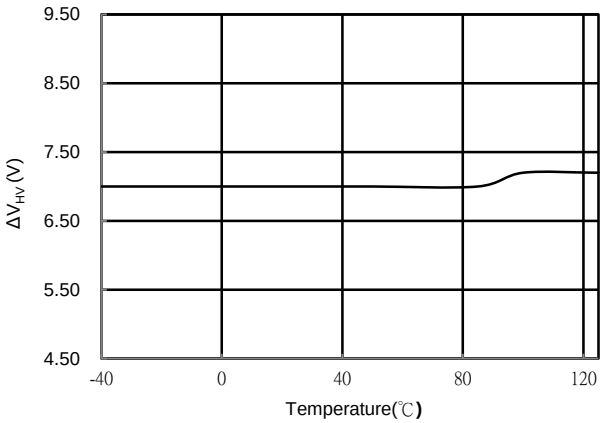


Fig. 12 ΔV_{HV} vs. Temperature

Application Information

Operation Overview

The LD7838 is a 700V HV start-up active PFC Flyback controller for LED lighting applications. It integrates more functions to reduce the external components counts and the size. Its major features are described as below.

The LD7838 is a voltage-mode TM PFC controller. The turn-on time of the switch is fixed while the turn-off time is varied in steady state. Therefore, the switching frequency varies in accordance with the input voltage variation. The LD7838 features over load protection, over voltage protection, over current protection, under voltage lockout and leading edge blinking time of the current sensing. Also, the LD7838 requires no mains voltage sensing unlike what the other traditional current mode PFC controllers behave for power saving.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The traditional circuit provides the startup current through a startup resistor to power up the PWM controller. However, it consumes significant power to meet the power saving requirement. In most cases, startup resistors carry large resistance. And, a larger resistor will spend more time to start up.

To achieve optimized topology, as shown in Fig. 13, LD7838 is implemented with a high-voltage startup circuit to enhance it. During startup, a high-voltage current source sinks current from the full-bridge rectifier to provide the startup current and charge Vcc capacitor C1 at the same time. On condition of VCC below UVLO(ON), the charge current will increases to 1.8mA once V_{CC} rises above UVLO(ON) voltage threshold during start up. Meanwhile, it consumes only 75μA for V_{CC} supply current, that most of the HV current is reserved to charge the V_{CC} capacitor. In using such configuration, the turn-on delay time will be almost no difference either in low-line or high-line conditions.

Once the V_{CC} voltage rises higher than UVLO(on) to power on the LD7838 and further to deliver the gate drive signal, the high-voltage current source will be disabled and the supply current is provided from the auxiliary winding of the transformer. Therefore, it would eliminate the power loss on the startup circuit and perform highly power saving.

An UVLO comparator is embedded to detect the voltage on the Vcc pin to ensure the supply voltage enough to power on the LD7838 PWM controller and in addition to drive the power MOSFET. As shown in Fig. 14, a hysteresis is provided to prevent the shutdown from the voltage dip during startup.

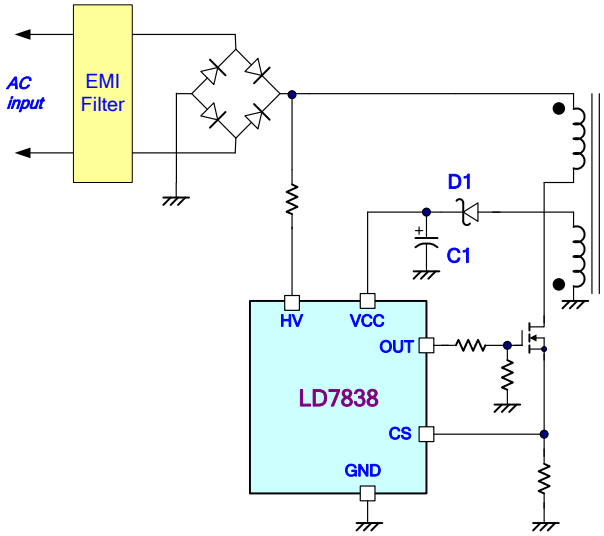


Fig. 13 High voltage start up circuit

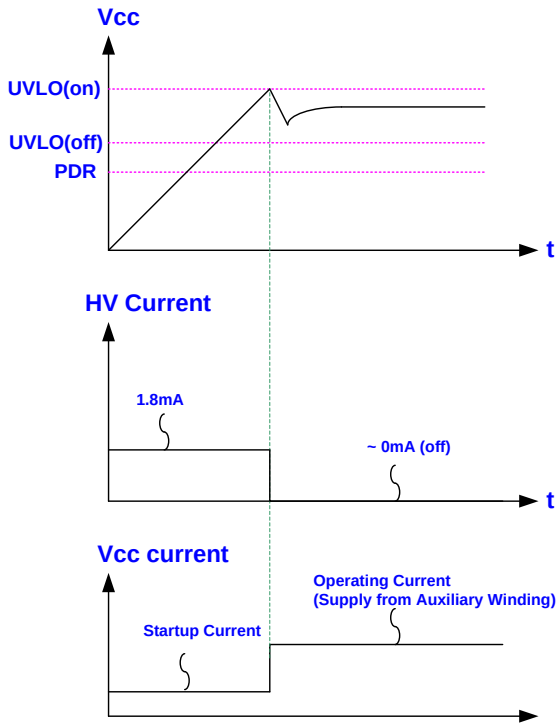


Fig. 14 High voltage start up sequence

Ramp Generator Block and Zero Current Detection (ZCD)

Fig. 15 shows typical ramp generator block and ZCD block. The comp pin voltage and the output of the ramp generator block are compared to determine the MOSFET ON-time, as shown in Fig. 16.

A greater comp voltage produces more ON-time. Using an external resistor connected to ZCD pin to set the desired slope of the internal ramp, the user may program the maximum ON-time. Alternatively, the ON-time will also achieve its maximum when COMP pin voltage trip OLP trigger point.

The maximum ON-time should be set according to the condition of the transformer, lowest AC line voltage, and maximum output power. A choice of optimum resistor value would result in best performance.

It shuts down the drive output if COMP pin voltage falls below zero ON-time threshold. This optimizes the efficiency in power saving in most conditions.

The Zero Current Detection block will detect auxiliary winding signal to drive MOSFET as ZCD pin voltage drops to 0.2V. As ZCD pin voltage drop to 0.2V, the current through the transformer is below zero. This feature enables transition-mode operation. The ZCD comparator would not operate if ZCD pin voltage remains at above 0.3V. Once it drops below 0.2V, the zero current detector will act to turn on the MOSFET.

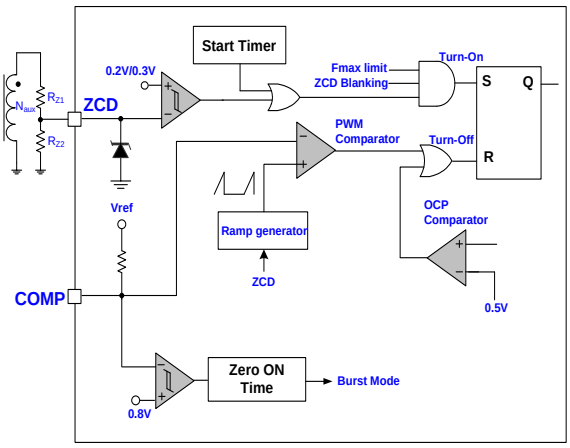


Fig. 15

Fig. 16 shows typical ZCD-related waveforms. Since ZCD pin carries some capacitance, it produces some delay to the turn-on time caused from Rz1. During delay time, the junction capacitor of the MOSFET resonates with the primary inductor of the transformer and the drain-source voltage (V_{DS}) decreases accordingly. So, the MOSFET consumes less voltage to turn on and it therefore minimizes the power dissipation.

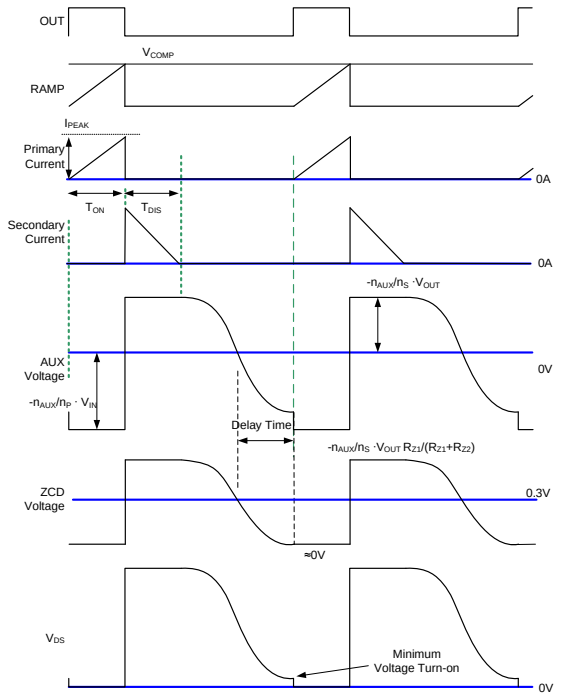


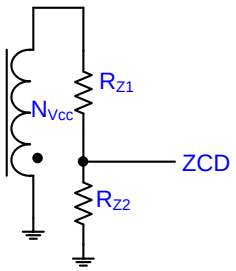
Fig. 16 ZCD related waveforms

Brown in/out Protection

The LD7838 features Burn-in/out function on HV pin. As the built-in comparator detects the DC voltage half wave rectify line voltage condition, it will shut off the controller to prevent from any damage. When $V_{HV} < V_{HVBO}$, the gate output will remain off even when the V_{CC} already reaches UVLO(ON). It therefore forces the V_{CC} hiccup between UVLO(ON) and UVLO(OFF). Unless the line voltage rises over V_{HVBI}, the gate output will not start switching even as the next UVLO(ON) is tripped. A hysteresis is implemented to prevent the false-triggering during turn-on and turn-off.

Programming Maximum ON-time

LD7838 features adjustable maximum ON-time to limit power output in abnormal operation. The selection of maximum ON-time is subject to ZCD resistance as shown in Fig. 17. ZCD resistance can be obtained from below:



$$R_{ZCD} = \frac{R_{Z1} \cdot R_{Z2}}{R_{Z1} + R_{Z2}}$$

Fig. 17

The following table is a suggestion for maximum ON-time setting.

R_{ZCD}	Max. Ton (Typ.)	R_{ZCD} Suggestion
43k < R_{ZCD}	25μs	47k
22k < R_{ZCD} < 33k	20μs	27k
10k < R_{ZCD} < 20k	16μs	14k
R_{ZCD} < 8k	10μs	6k

Output OVP on ZCD

When the LED string open circuit occurs, the reflected output voltage of aux winding will cause ZCD voltage up. If the ZCD voltage runs up to 3.5V, LD7838 will enforce the gate off until the 2nd cycle of Vcc hiccup is tripped, The selection of output over voltage (V_{OVP})trigger level is subject to ZCD divide resistance as the below equation:

$$V_{OVP} \times \frac{N_{VCC}}{N_S} \times \frac{R_{Z2}}{R_{Z1}+R_{Z2}} = 3.5V$$

Output Drive Stage

With typical 125mA/-500mA driving capability, an output stage of a CMOS buffer is incorporated to drive a power MOSFET directly. The output voltage is clamped at

13V to protect the MOSFET gate even when the VCC voltage is higher than 13V.

Current Sensing and Leading-edge Blanking

The LD7838 detects the primary MOSFET current from the CS pin, which is for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.85V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. In the low power application, if the total pulse width of the turn-on spikes is less than and the negative spike on the CS pin doesn't exceed -0.3V, it could eliminated the R-C filter.

However, the total pulse width of the turn-on spike is determined by the output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter for higher power application to avoid the CS pin being damaged by the negative turn-on spike.

Adjustable OCP Compensation

In general, the power converter can deliver more current at high input voltage than at low input voltage. To compensate this, an offset voltage is added to the CS signal by an internal current source (IOCP) and an external resistor (R_{CS}) in series between the sense resistor (Rs) and the CS pin, as shown in Fig. 18.

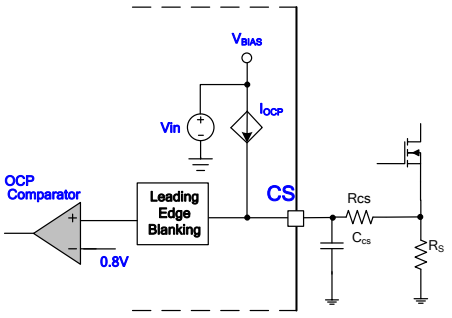


Fig. 18 Current sense for over current protection

By selecting a proper value of the resistor in series with the CS pin, the amount of compensation can be adjusted.

Over Load Protection (OLP) - Auto Recovery

To protect the circuit from damage due to overload condition or output short condition, a smart OLP function is implemented in the LD7838 for it. The OLP function is an auto-recovery type protection. Fig. 19 shows the waveforms of the OLP operation. Under such fault condition, the feedback system will force the voltage loop toward saturation and thus pull up the voltage of COMP pin (VCOMP). If the VCOMP trips the OLP threshold of 4.5V and stays for over OLP delay time, the protection will be activated to turn off the gate output and to shut down the switching of power circuit. The OLP delay time is to prevent the false-trigger during the power-on and turn-off transient.

A divided-by-4 counter is implemented to reduce the average power consumption under OLP behavior.

Whenever OLP is activated, the output is latched off and the divided-by-4 counter starts to count the number of UVLO(off). The latch will be released if the 4nd UVLO(off) point is counted, and then the output recovers switching again.

By using such protection mechanism, the average input power can be reduced to a very low level so that the component temperature and stress can be controlled within a safe operating area.

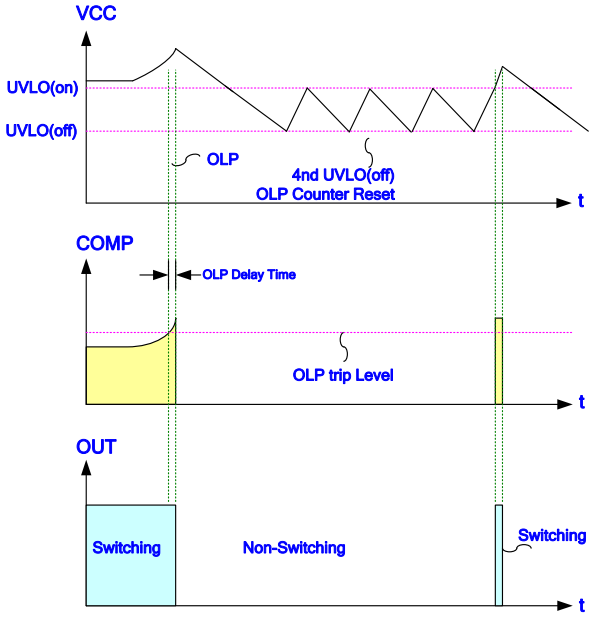


Fig. 19 Over load protection sequence

OVP (Over Voltage Protection) on Vcc

The maximum rating of the VCC pin is limited below 29V. To prevent VCC from the fault condition, the LD7838 is implemented with OVP function on Vcc pin. As soon as the Vcc voltage is over OVP threshold voltage, the output gate drive circuit will be shutdown simultaneously thus to stop the switching of the power MOSFET until the next UVLO(on). The Vcc over voltage function of the LD7838 is an auto-recovery protection. The Fig. 20 shows its operation. Upon removal of the OVP condition will resume the Vcc level and the output operation

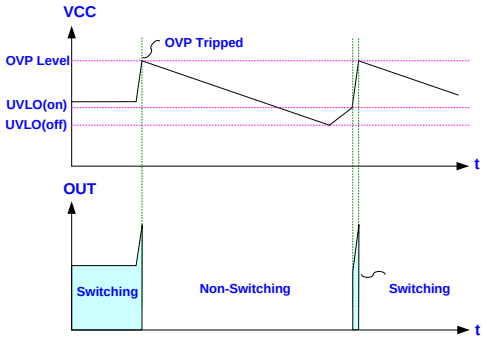
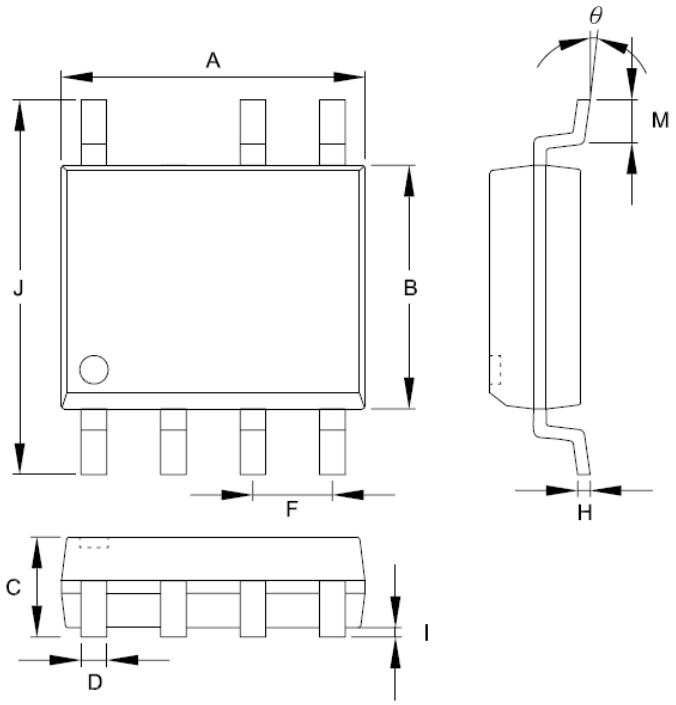


Fig. 20 Over voltage protection on VCC pin

Package Information

SOP-7



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

REV.	Date	Change Notice
00	10/31/2016	Original Specification.
01	11/22/2016	Update EC table