LD1512

12 Channel Output LED Driver
with 8/12/16 bit PWM Controller

Ver. 1.0 / Dec. 2009

LDT Inc. Mplaza 3F, 538, Dujeong-dong, Seobuk-gu, Cheonan, Chungnam, 331-958, Korea
TEL 82 41 520 7300 FAX 82 41 520 7337 www.ldt.co.kr

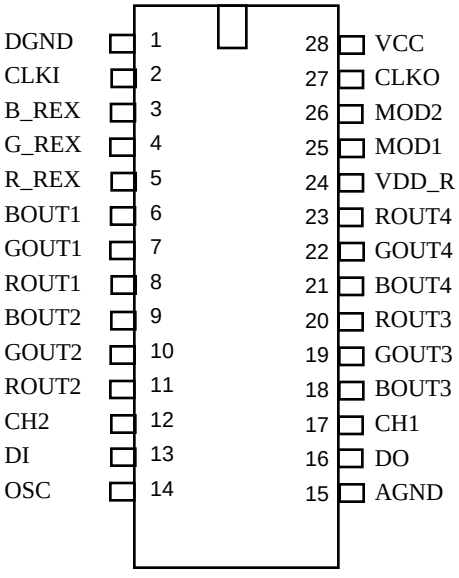
DESCRIPTION

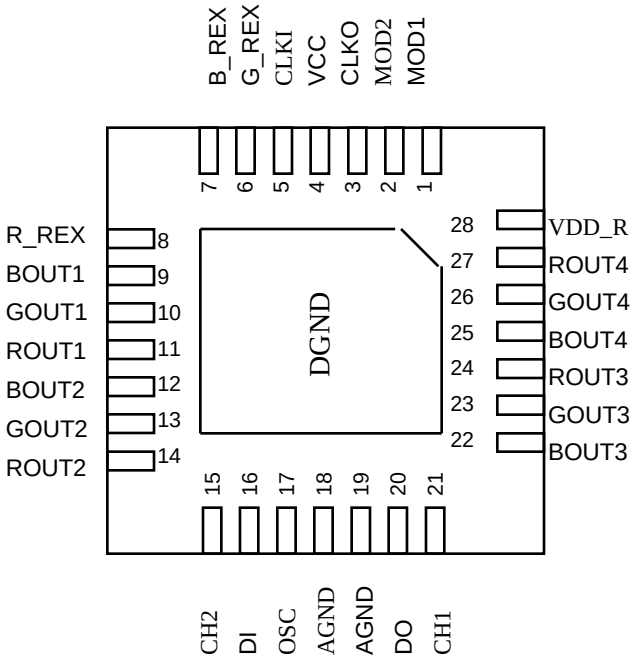
The LD1512 is specifically designed for LED lighting or display applications. The 12-channel constant output current is controlled by 3 external resistors (IOUT = 5mA to 60mA). The device consists of 16 x 12 bit shift register, latches, built-in OSC, 12 constant current drivers and 8/12/16 bit PWM controller.
The main applications are decorative LED lighting, indoor/outdoor LED video or message display systems.

FEATURES

- 12 constant output channels
- 8/12/16bit grayscale PWM control
- Output current : set-up at 5mA to 60mA with three external resistors
- Maximum sinking output voltage : **40V**
- CMOS compatible input
- Package : SOP28, SSOP28, 28QFN
- Maximum serial input frequency : 20MHz
- Built in internal RC oscillator : 10MHz

PIN CONFIGURATION





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PIN DESCRIPTION

PIN NO.		PIN NAME	DESCRIPTION
28SOP	28QFN		
2	5	CLKI	Clock input pin for Data shift When MOD2=1, MOD1=1 Clk Pin be to connet to vss
13	16	DI	Serial data input terminal or Output Enable/Disable Serial data input When MOD2=0, MOD1=0 MOD2=0, MOD1=1 MOD2=1, MOD1=0 Output Enable/ disable When MOD2=1, MOD1=1 DI=1 is Output Disable. DI=0 is Output Enable MOD Pin must be connected vss or VDD_R.
14	17	OSC	Test Only Pin. TEST pin should be not connected
26,25	2, 1	MOD2,1	Input data transfer mode selection 0, 0 : 8bit luminance data transfer 0, 1 : 12bit luminance data transfer 1, 0 : 16bit luminance data transfer 1, 1 : All LED driver are only on /off by DI signal. MOD Pin must be connected vss or VDD_R.
24	28	VDD_R	Regulator output voltage
5. 4. 3	8, 7, 6	R_REX,G_REX,B_REX	External resistors connected between those pins and GND for driver current setting.
1	Thermal Pad	DGND	GND terminal
8,7,6 11, 10 ,9 20, 19, 18 23, 22, 21	11,10,9, 14,13,12, 24,23,22, 27,26,25	ROUT1,GOUT1,BOUT1 ROUT2,GOUT2,BOUT2 ROUT3,GOUT3,BOUT3 ROUT4,GOUT4,BOUT4	Constant current output terminals
15	18, 19	AGND	Power Ground
28	4	VCC	LED driving voltage

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PIN DESCRIPTION

PIN NO.		PIN NAME	DESCRIPTION
28SOP	28QFN		
12,17	15, 21	CH2, CH1	LED driver channel mode selection 0,0 : 12 Channel 0,1 : 6 Channel (ROUT1=ROUT2,GOUT1=GOUT2, BOUT1=BOUT2 ROUT3=ROUT4, GOUT3=GOUT4, BOUT3=BOUT4) 1,0 : 3 Channel (ROUT1=ROUT2=ROUT3=ROUT4 GOUT1=GOUT2=GOUT3=GOUT4 BOUT1=BOUT2=BOUT3=BOUT4) 1,1 : Inhibit CH Pin must be connected vss or VDD_R.
27	3	CLKO	Serial clock output terminal
16	20	DO	Serial data output when CLKI is 'Rising", strobe transmit after 10us from CLKI rising edge When MOD2=1, MOD1=1 DO pin become Output Enable Output pin

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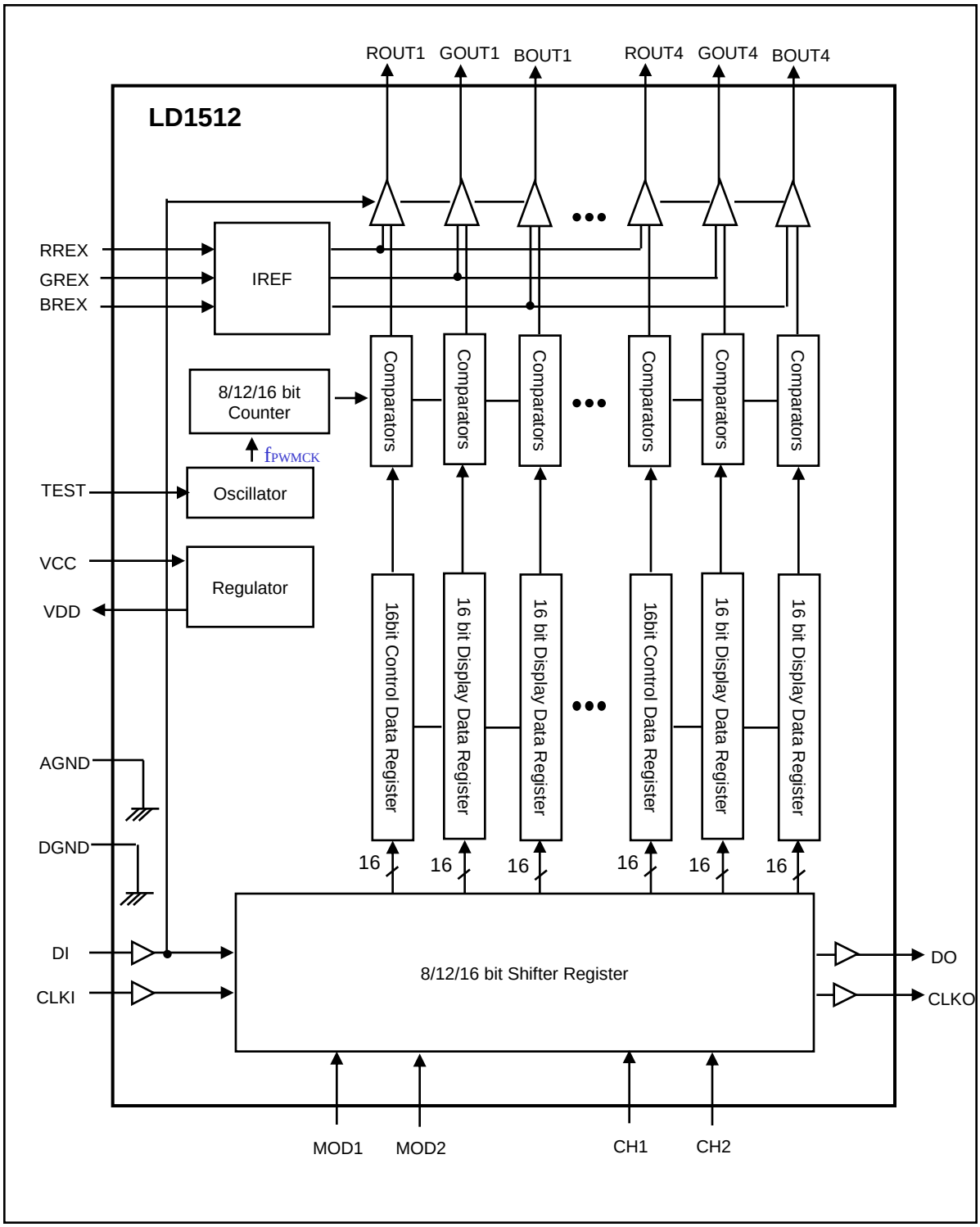
BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	0~40	V
Regulator Voltage	V_{DD}	0~6.5	V
Output Voltage	V_{OUT}	-0.5~30	V
Output Current	I_{OUT}	60	mA
Input Voltage	V_{IN}	-0.4~V_{DD}+0.4	V
GND Terminal Current	I_{GND}	960	mA
CLKI Frequency	f_{CK}	20	MHz
Internal PWM Clock Frequency	fPWMCK	12	MHz
Power Dissipation	P_D	1.4	W
Operating Temperature	T_{opr}	-40~85	°C
Storage Temperature	T_{stg}	-55~150	°C

(Note) Ambient temperature delated above 25°C in the proportion of 14.2mW/ °C

RECOMMENDED OPERATING CONDITIONS

DC CHARACTERISTICS		SYMBOL	MIN.	TYP.	MAX.	UNIT
VCC Supply Voltage		V_{cc}	4.5	-	40	V
LED Driver Output Voltage		V_{OUT}			40	V
VDD Regulator Voltage or External Supply Voltage		V_{DD}	4.5	5.0	5.5	V
Input Voltage	"H" Level	V_{IH}	0.7V_{DD}	-	V_{DD}	V
	"L" Level	V_{IL}	GND	-	0.3V_{DD}	
Output Voltage	DO,CLKO, IOH = -10mA IOL = 10mA	V_{OL}	-	-	0.2V_{DD}	V
		V_{OH}	0.8V_{DD}	-	-	
High Level Output Current, VO = 0.8VDD		I_{OH}	-10			mA
Low Level Output Current, VO = 0.2VDD		I_{OL}			10	mA
LED Driver Output Current		I_{OUT}			60	mA
Operating Free-air Temperature Range			-40		85	°C
AC CHARACTERISTICS		**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
CLKI Frequency		f_{CK}			20	MHz
Internal PWM Clock Frequency		f_{PWMCK}	8	10	12	MHz
Pulse Width	CLKI	t_{WH0} / t_{WL0}	20			ns
Setup Time		t_{setup}	-10			ns
Hold Time		t_{hold}	40			ns

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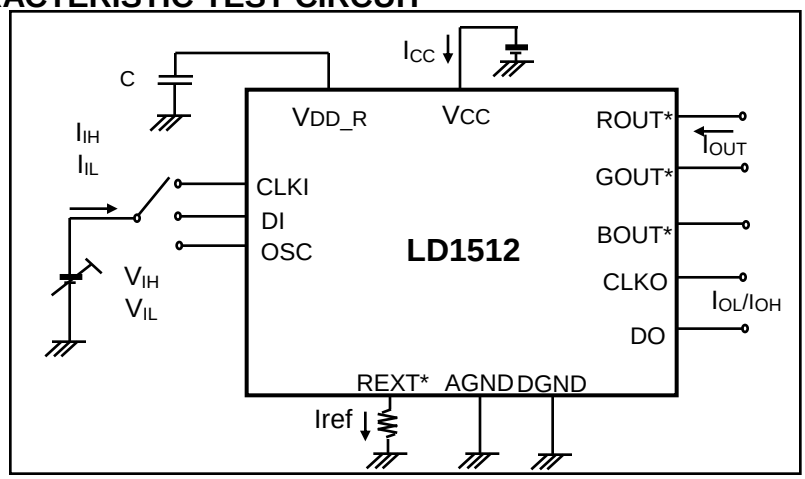
ELECTRICAL CHARACTERISTICS (VDD = VDD_R = 5V, Ta = 25°C)

PARAMETER		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VCC Supply Voltage		VCC		4.5	-	40	V
VDD Regulator Voltage or External Supply Voltage		VDD		4.5	5.0	5.5	V
Input Voltage	H Level	VIH	-	0.7VDD		VDD	V
	L Level	VIL	-	GND		0.3VDD	
Output Leakage Current		IOZ	VOH=6.0V			1	uA
Output Voltage	DO,CLKO	VOL	IOL=10mA			0.2VDD	V
		VOH	IOH=-10mA	0.8VDD			
Output Current1 Pin to Pin Deviation		IOLPP1	REXT=1.6KΩ IOUT=60㎃, VOUT=1.5V		±1.5	±3.0	%
Output Current2 Pin to Pin Deviation		IOLPP2	REXT=3.2KΩ IOUT=30㎃, VOUT=1.5V		±1.5	±3.0	%
Output Current1 Chip to Chip Deviation		IOLCC1	REXT=1.6KΩ IOUT=60㎃, VOUT=1.5V		±3.0	±6.0	%
Output Current1 Chip to Chip Deviation		IOLCC2	REXT=3.2kΩ IOUT=30㎃, VOUT=1.5V		±3.0	±6.0	%
Supply Current		I_{CC1}	REXT=Open, OUTn=OFF PWM=Gray0	-	1.0	2.0	mA
		I_{CC2}	REXT=1.6KΩ, OUTn=OFF PWM=Gray0	-	7.0	15.0	
		I_{CC3}	REXT=3.2KΩ, OUTn=OFF PWM=Gray0	-	5.0	10.0	

DC CHARACTERISTIC TEST CIRCUIT



*) REXT = RREX,GREX,BREX, ROUT = ROUT1~4, GOUT=GOUT1~4, BOUT= BOUT1~4

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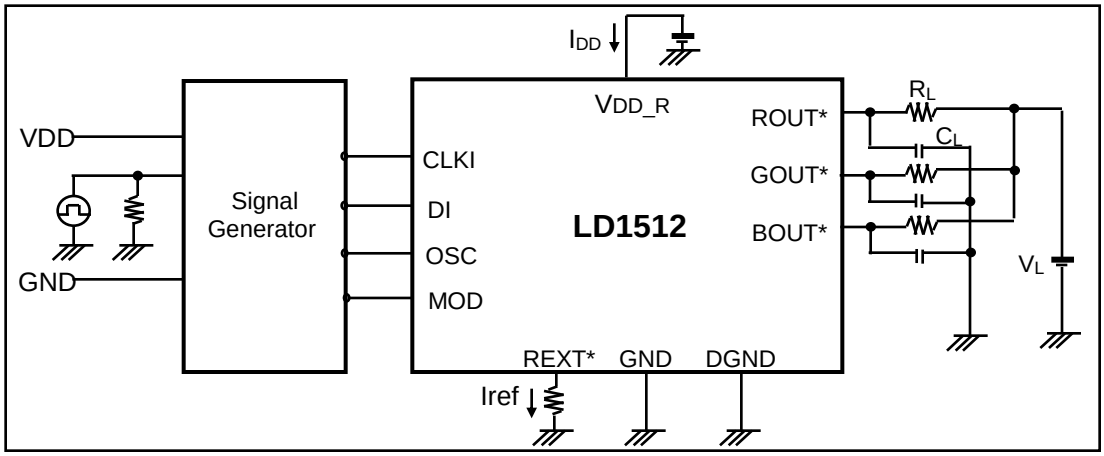
AC CHARACTERISTIC TEST CIRCUIT



*) REXT = RREX,GREX,BREX, ROUT = ROUT1~4, GOUT=GOUT1~4, BOUT= BOUT1~4

SWITCHING CHARACTERISTICS (Ta = 25°C unless otherwise noted)

PARAMETER		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	CLKI-DO	t_{PLH}	V_{DD} = 5.0V V_{IH} = VDD V_{IL} = GND f_{CK} = 10MHz R_{EXT} = 3.2kΩ I_{OUT} = 30mA C_L = 10.0pF R_L = 100Ω VL = 4.5V	-	20	30	ns
Propagation Delay Time ("H" to "L")	CLKI-DO	t_{PHL}		-	20	30	ns
Maximum CLKI Frequency		f_{CKMAX} (*1)		-	8	20	MHz
Pulse Width	CLKI	t_{WH0} / t_{WL0}		25	-	-	ns
		t_{WH1}		25	-	-	ns
Data Setup Time		t_{setup}		- 10 *1)	-		ns
Data Hold Time		t_{hold}		40	-	-	
DI Width		twsh		200	-	-	ns
		twsl		200	-	-	
		twss		10,000 (*2)	-	-	
Clock Delay	CLKO	t_{CKD}		-	13	-	ns
Clock Width	CLKO	t_W		-	25	-	ns
Clock Cycle	CLKO	t_{CY}		100	-	2000	ns
Maximum Clock Rise Time		t_r		-	-	10	ns
Maximum Clock Fall Time		t_f		-	-	10	
Minimum Output Rise Time		t_{or}		-	50		ns
Minimum Output Fall Time		t_{of}		-	50		

*1 : DI should be set at the rising of CLKI .
*2 : N= 1000ea

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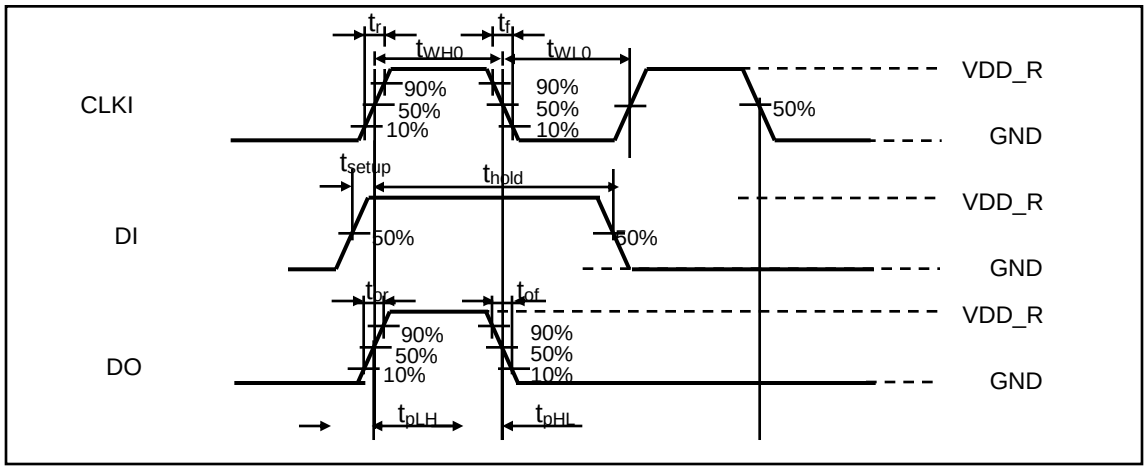
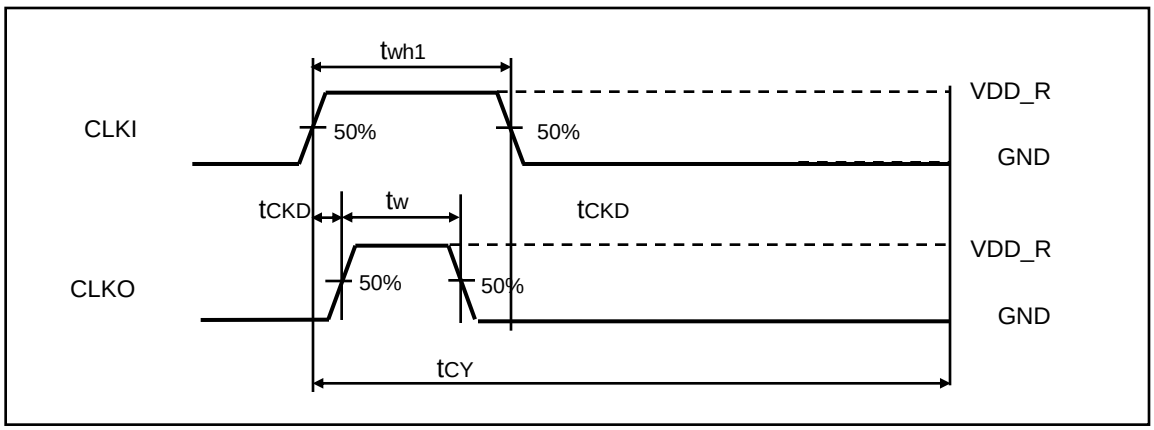
TIMING WAVEFORM

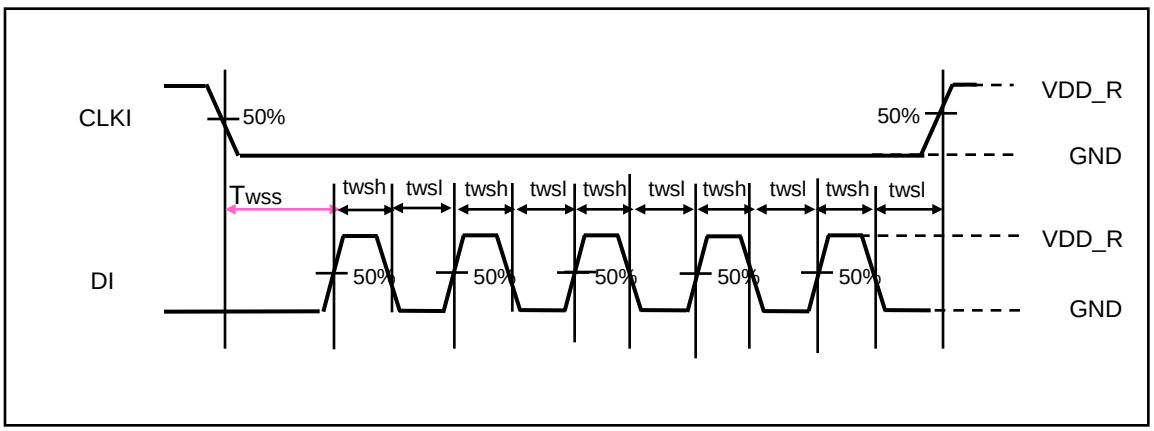
CLKI, DI, DO (Data Transmit)



CLKI, CLKO



CLKI, DI (Strobe Transmit)



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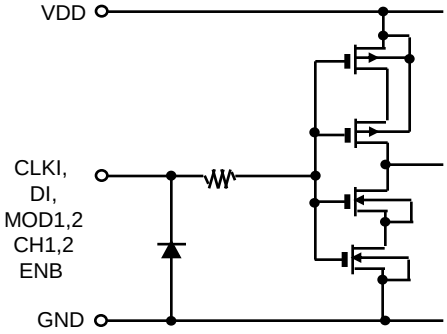
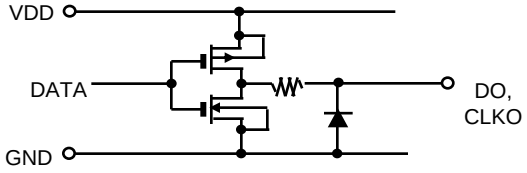
EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

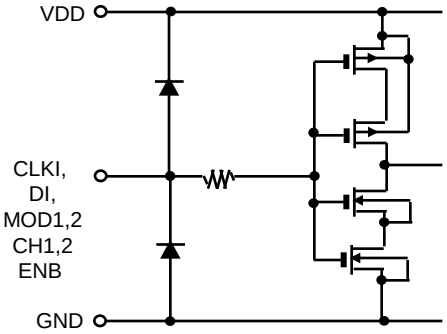
1. CLKI, DI terminal



2. DO, CLKO terminal



3. MOD1, MOD2, CH1, CH2 **terminal**



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ADJUSTING OUTPUT CURRENT

The output current is determined by an external resistor. The relationship between I_{OUT} and R_{EXT} is as follows;

When VDD_R = 5V

$$I_{OUT}[A] = \{1.16/(30+R_{EXT})\} * 82$$

OUTPUT CURRENT AND REXT RESISTOR

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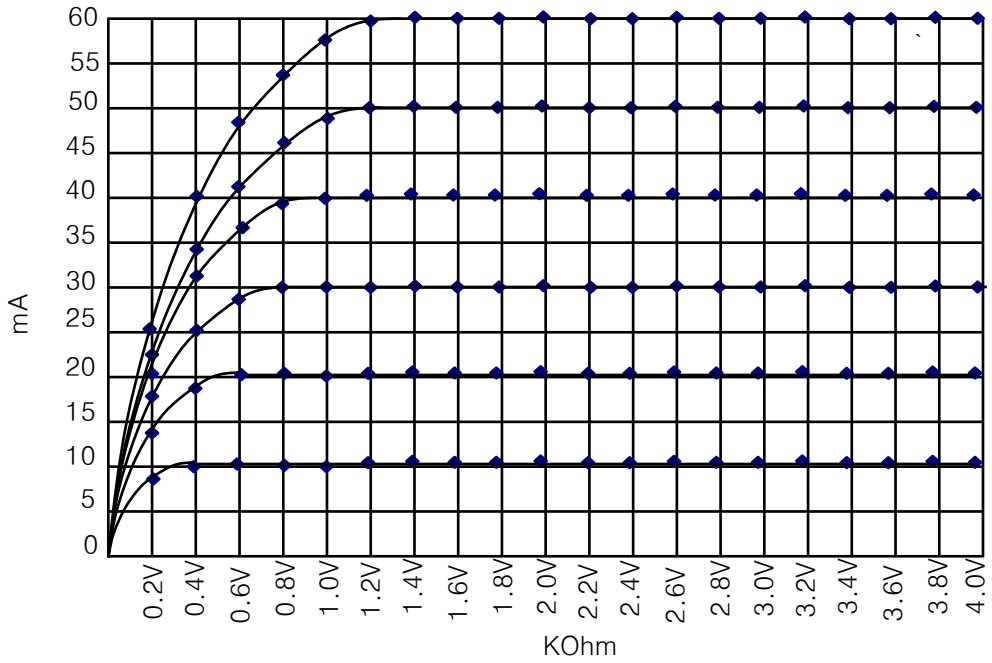
CONSTANT OUTPUT CURRENT

The LD1512 provides a constant current output characteristics for LED display application. ;



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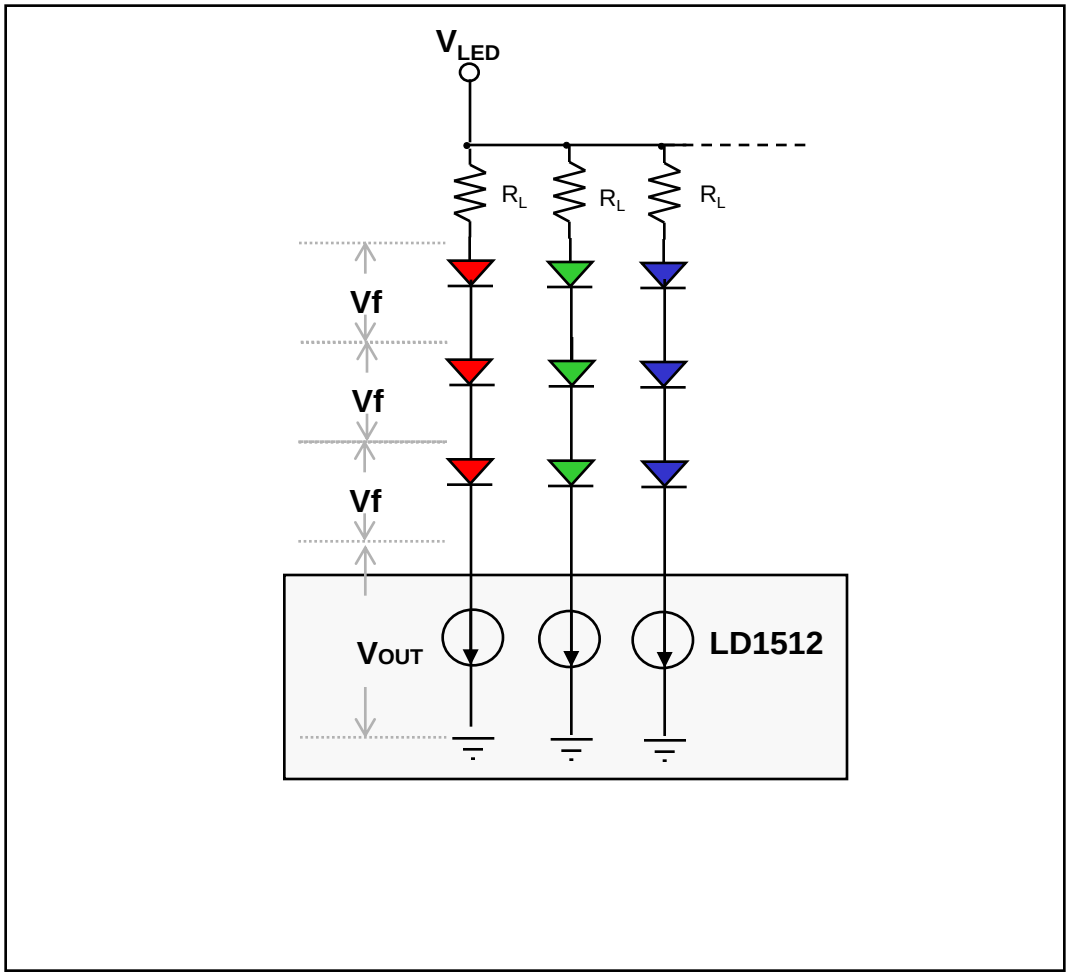
LED SUPPLY VOLTAGE(VLED)



It is very important to select the proper value of Load Resistor(RL). Because the optimal VOUT value guarantees the constant output current and long life time of LED driver IC without over power consumption.

For example, let's calculate the Load Resistor value at VLED=12V, Iout=50mA, LED Forward Voltage(Vf)=3V and LED = 3ea.

1) The full current of LD1512 = 50mA x 12 (channels) = 600mA
2) The power consumption is 600mA x VOUT voltage.
   - when VOUT = 1V, the power consumption is 600mW.
   - when VOUT= 2V, the power consumption is 1200mW.

Therefore, the Load Resistor (RL) = (VLED – VOUT– Vfx3) / Iout
= (12V – VOUT – 9V) / 50mA
= 40Ω (When VOUT = 1V)

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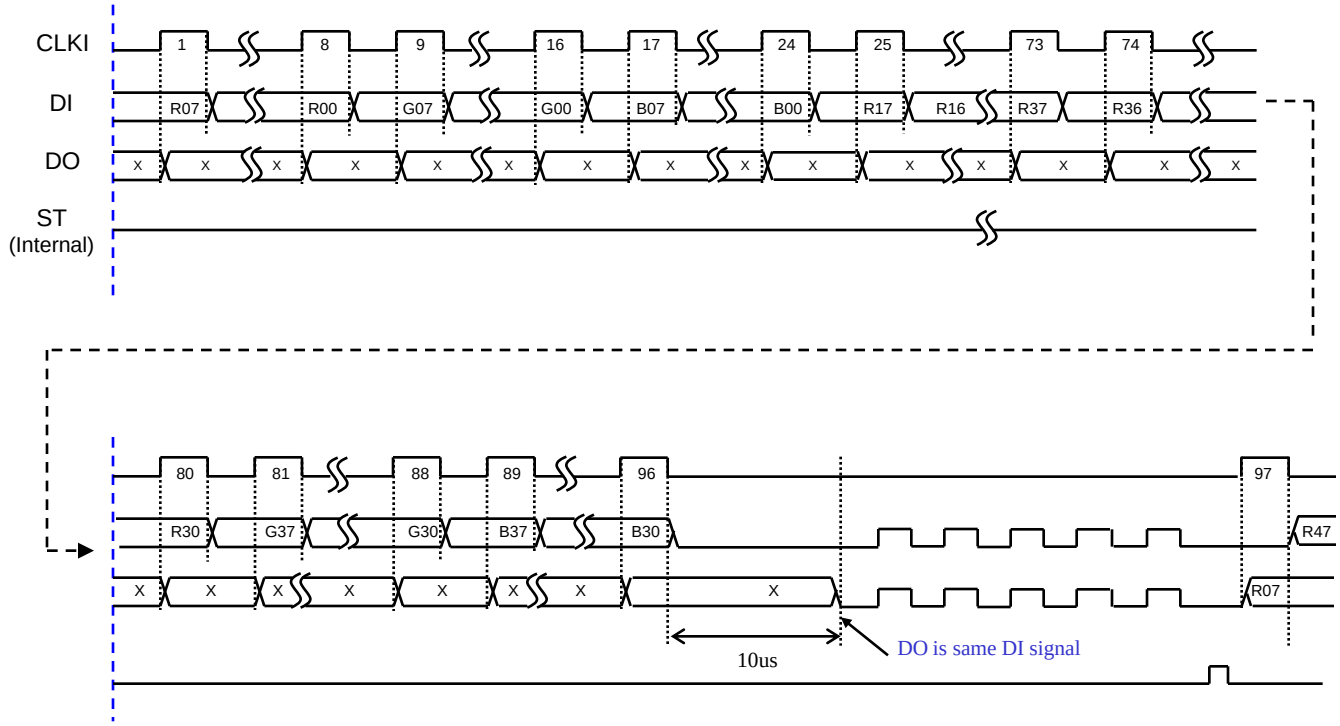
FUNCTIONAL DESCRIPTION

COMMUNICATION MODE TIMING DIAGRAM

8bit Mode, 12 Channel (MOD2 = L, MOD1=L, CH2 =L, CH1 = L)



When 2 chips are connected in series, strobe signal shall be applied after 192ea of clock input.

When more than 2 chips are connected in series, strobe signal shall be applied

after N x 96ea of clock input. ('N' is the number of chip.)

**Note) Apply the strobe signal after minimum 10us from the last clock (e.g. 192th clock in 2 chips)

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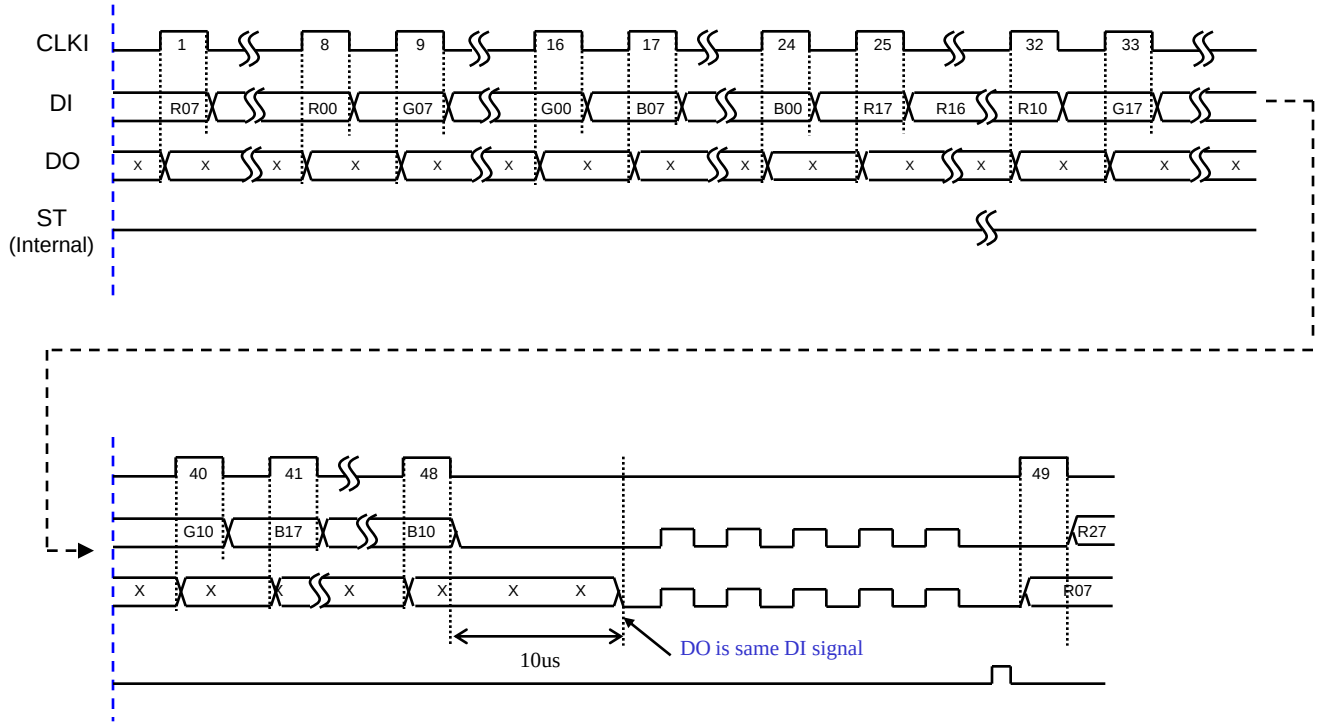
FUNCTIONAL DESCRIPTION

COMMUNICATION MODE TIMING DIAGRAM

8bit Mode, 6 Channel (MOD2 = L, MOD1=L, CH2 =L, CH1 = H)



When 2 chips are connected in series, strobe signal shall be applied after 96ea of clock input.

When more than 2 chips are connected in series, strobe signal shall be applied

after N x 48ea of clock input. ('N' is the number of chip.)

**Note) Apply the strobe signal after minimum 10us from the last clock (e.g. 96th clock in 2 chips)

ROUT1=ROUT2, GOUT1=GOUT2, BOUT1=BOUT2

ROUT3=ROUT4, GOUT3=GOUT4, BOUT3=BOUT4

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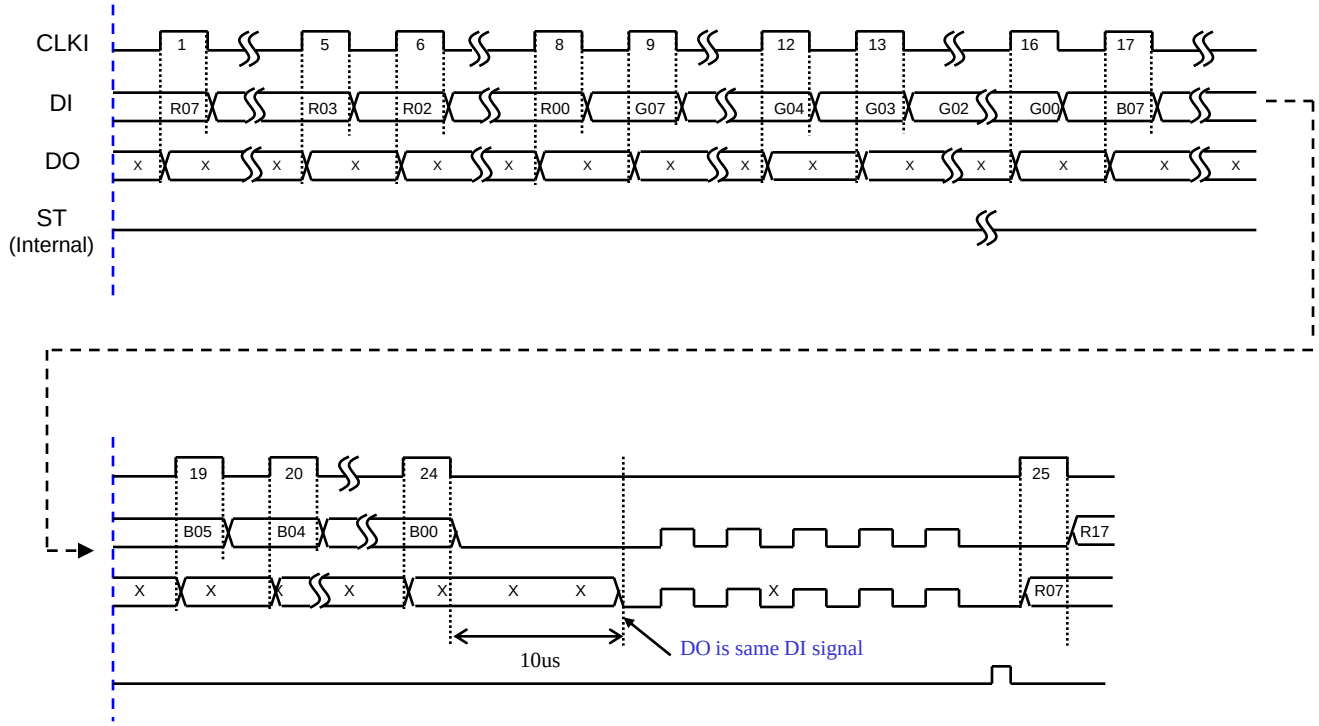
FUNCTIONAL DESCRIPTION

COMMUNICATION MODE TIMING DIAGRAM

8bit Mode, 3 Channel (MOD2 = L, MOD1=L, CH2 =H, CH1 = L)



When 2 chips are connected in series, strobe signal shall be applied after 48ea of clock input.

When more than 2 chips are connected in series, strobe signal shall be applied

after N x 24ea of clock input. ('N' is the number of chip.)

**Note) Apply the strobe signal after minimum 10us from the last clock (e.g. 48th clock in 2 chips)

ROUT1=ROUT2=ROUT3=ROUT4

GOUT1=GOUT2=GOUT3=GOUT4

BOUT1=BOUT2=BOUT3=BOUT4

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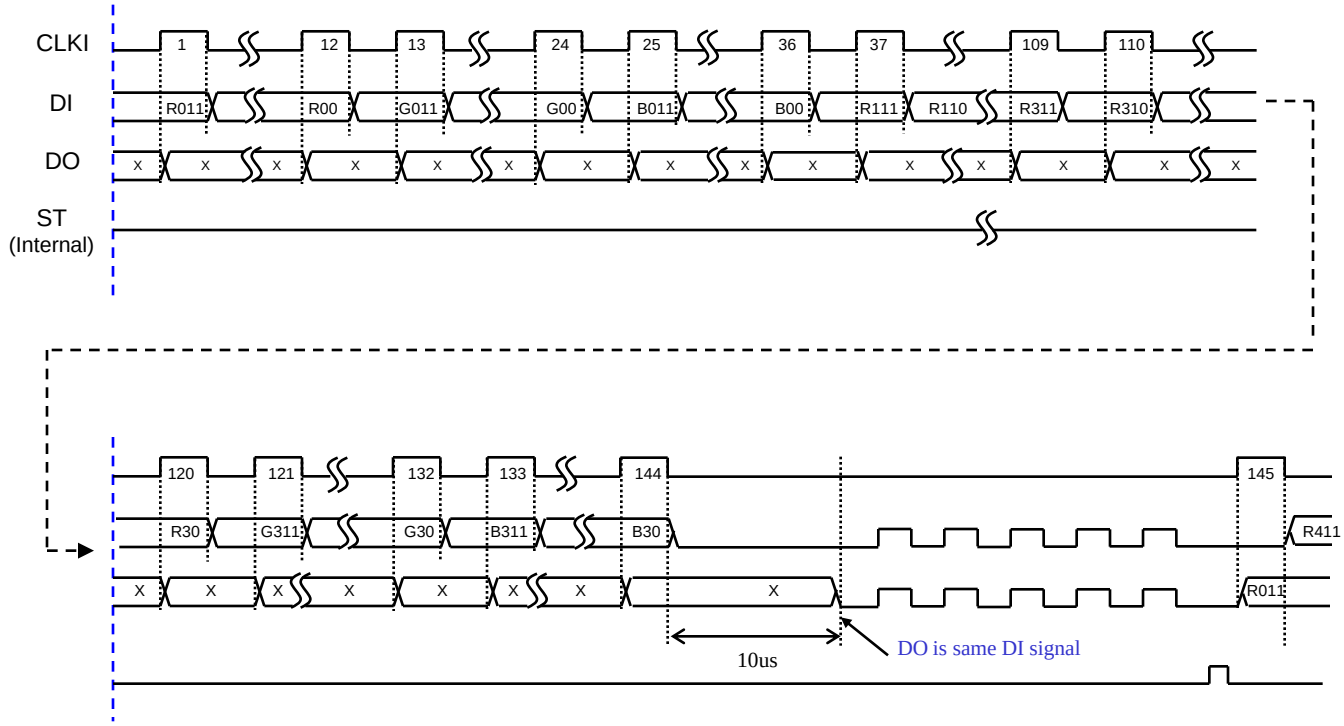
FUNCTIONAL DESCRIPTION

COMMUNICATION MODE TIMING DIAGRAM

12bit Mode, 12 Channel (MOD2= L, MOD1 = H, CH2 = L, CH1 = L)



When 2 chips are connected in series, strobe signal shall be applied after 288ea of clock input.

When more than 2 chips are connected in series, strobe signal shall be applied

after N x 144ea of clock input. (‘N’ is the number of chip.)

**Note) Apply the strobe signal after minimum 10us from the last clock (e.g. 288th clock in 2 chips)

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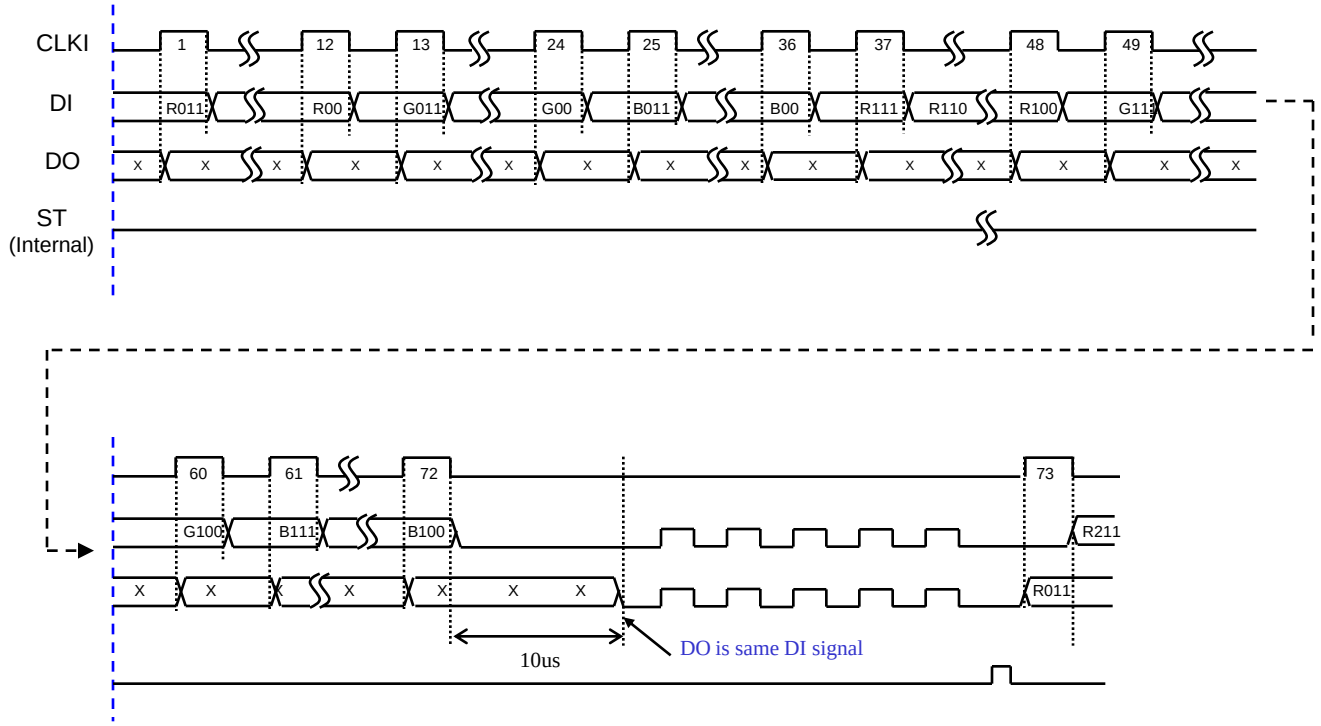
FUNCTIONAL DESCRIPTION

COMMUNICATION MODE TIMING DIAGRAM

12bit Mode, 6 Channel (MOD2= L, MOD1 = H, CH2 = L, CH1 = H)



When 2 chips are connected in series, strobe signal shall be applied after 144ea of clock input.

When more than 2 chips are connected in series, strobe signal shall be applied

after N x 72ea of clock input. ('N' is the number of chip.)

**Note) Apply the strobe signal after minimum 10us from the last clock (e.g. 144th clock in 2 chips)

ROUT1=ROUT2, GOUT1=GOUT2, BOUT1=BOUT2
ROUT3=ROUT4, GOUT3=GOUT4, BOUT3=BOUT4

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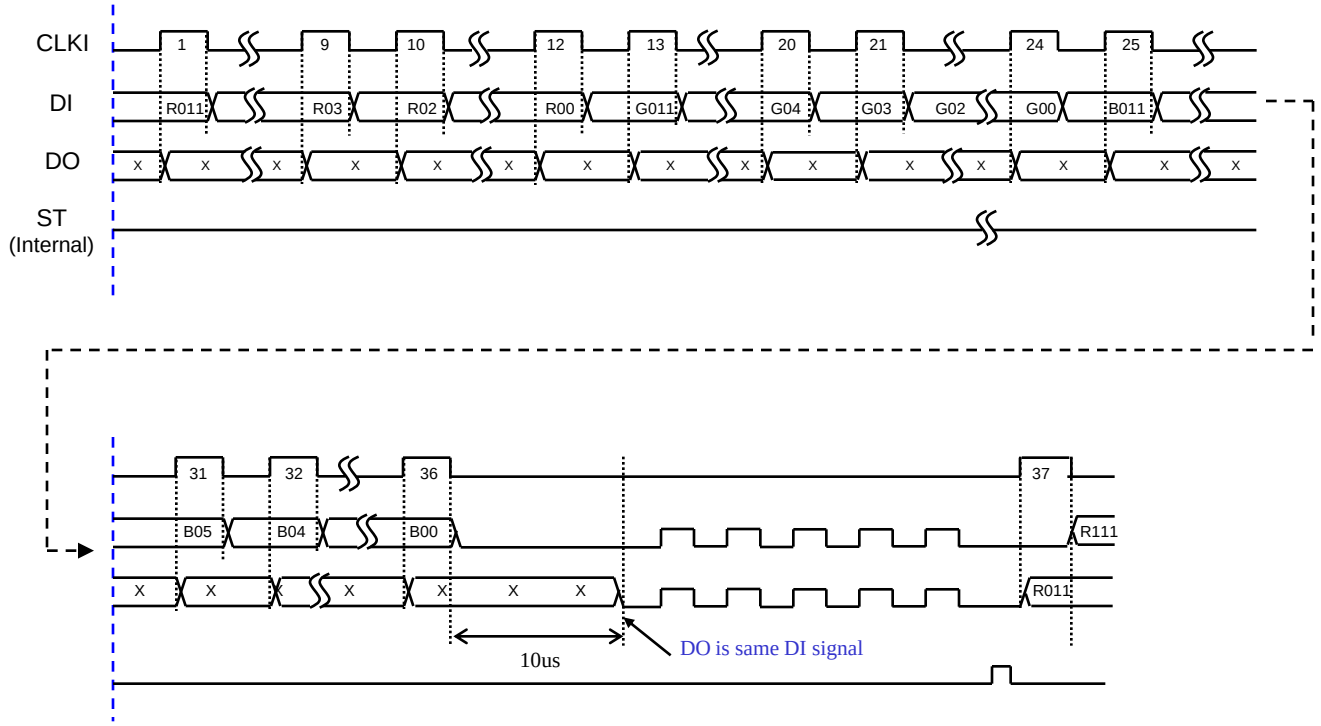
FUNCTIONAL DESCRIPTION

COMMUNICATION MODE TIMING DIAGRAM

12bit Mode, 3 Channel (MOD2= L, MOD1 = H, CH2 = H, CH1 = L)



When 2 chips are connected in series, strobe signal shall be applied after 72ea of clock input.

When more than 2 chips are connected in series, strobe signal shall be applied

after N x 36ea of clock input. ('N' is the number of chip.)

**Note) Apply the strobe signal after minimum 10us from the last clock (e.g. 72th clock in 2 chips)

ROUT1=ROUT2=ROUT3=ROUT4
GOUT1=GOUT2=GOUT3=GOUT4
BOUT1=BOUT2=BOUT3=BOUT4

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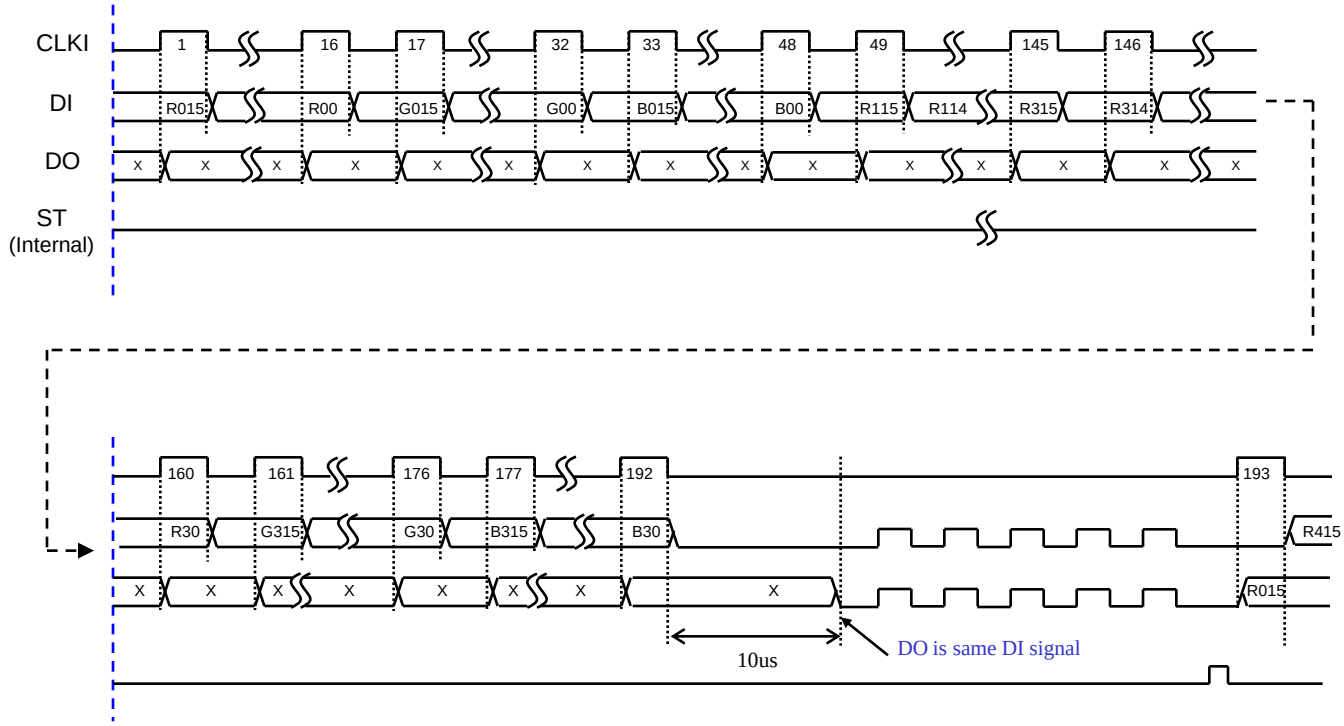
FUNCTIONAL DESCRIPTION

COMMUNICATION MODE TIMING DIAGRAM

16bit Mode, 12 Channel (MOD2= H, MOD1 = L, CH2= L, CH1 = L)



When 2 chips are connected in series, strobe signal shall be applied after 384ea of clock input.

When more than 2 chips are connected in series, strobe signal shall be applied

after N x 192ea of clock input. (‘N’ is the number of chip.)

**Note) Apply the strobe signal after minimum 10us from the last clock (e.g. 284th clock in 2 chips)

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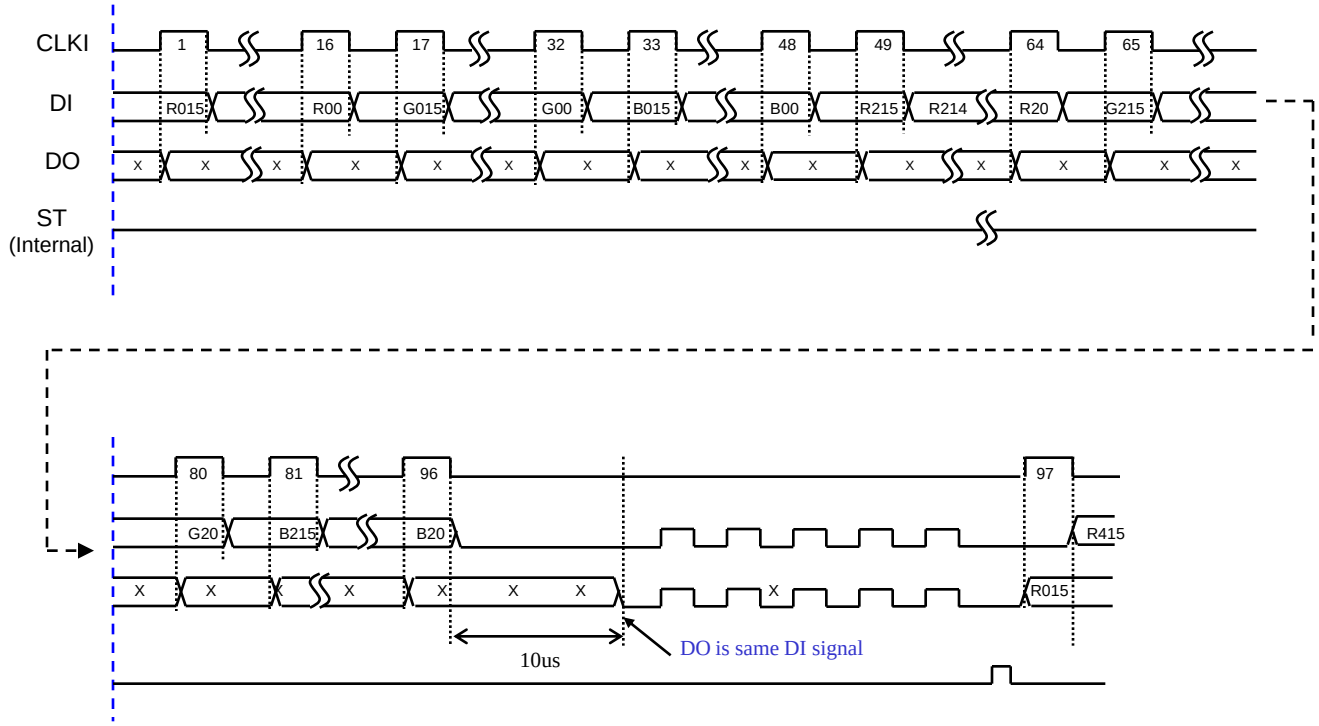
FUNCTIONAL DESCRIPTION

COMMUNICATION MODE TIMING DIAGRAM

16bit Mode, 6 Channel (MOD2= H, MOD1 = L, CH2= L, CH1 = H)



When 2 chips are connected in series, strobe signal shall be applied after 192ea of clock input.

When more than 2 chips are connected in series, strobe signal shall be applied

after N x 96ea of clock input. ('N' is the number of chip.)

**Note) Apply the strobe signal after minimum 10us from the last clock (e.g. 192th clock in 2 chips)

ROUT1=ROUT2, GOUT1=GOUT2, BOUT1=BOUT2
ROUT3=ROUT4, GOUT3=GOUT4, BOUT3=BOUT4

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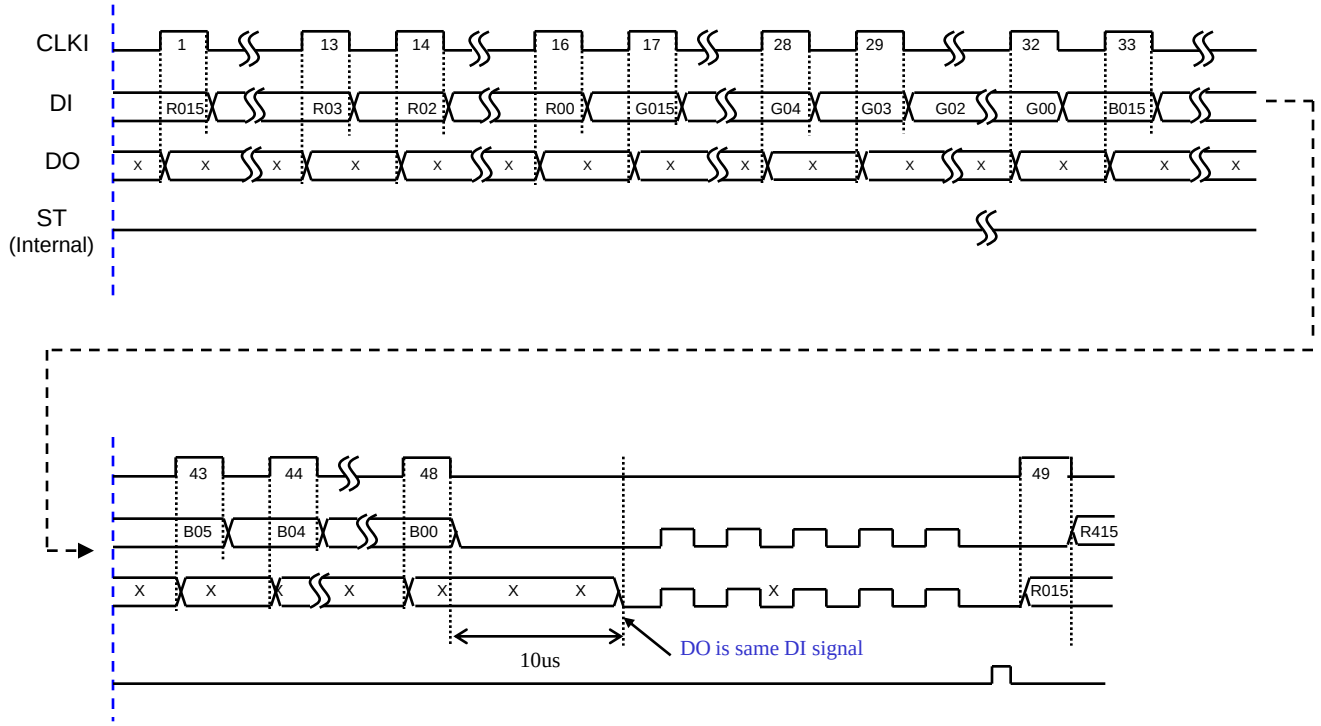
FUNCTIONAL DESCRIPTION

COMMUNICATION MODE TIMING DIAGRAM

16bit Mode, 3 Channel (MOD2= H, MOD1 = L, CH2= H, CH1 = L)



When 2 chips are connected in series, strobe signal shall be applied after 96ea of clock input.

When more than 2 chips are connected in series, strobe signal shall be applied

after N x 48ea of clock input. ('N' is the number of chip.)

**Note) Apply the strobe signal after minimum 10us from the last clock (e.g. 96th clock in 2 chips)

$$ROUT1=ROUT2=ROUT3=ROUT4$$
$$GOUT1=GOUT2=GOUT3=GOUT4$$
$$BOUT1=BOUT2=BOUT3=BOUT4$$

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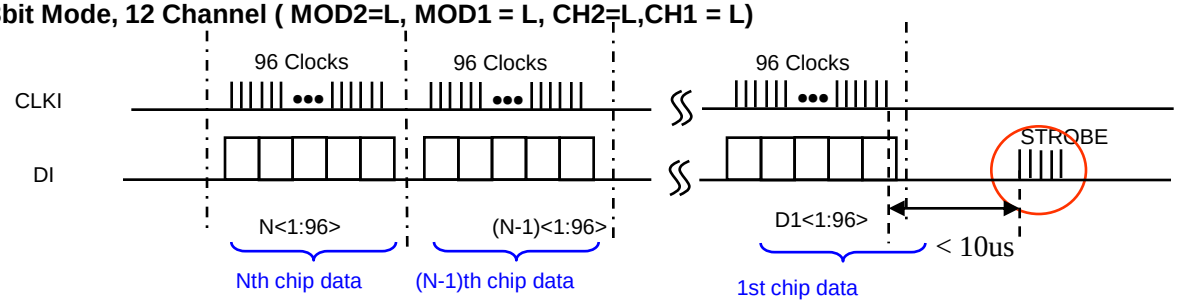
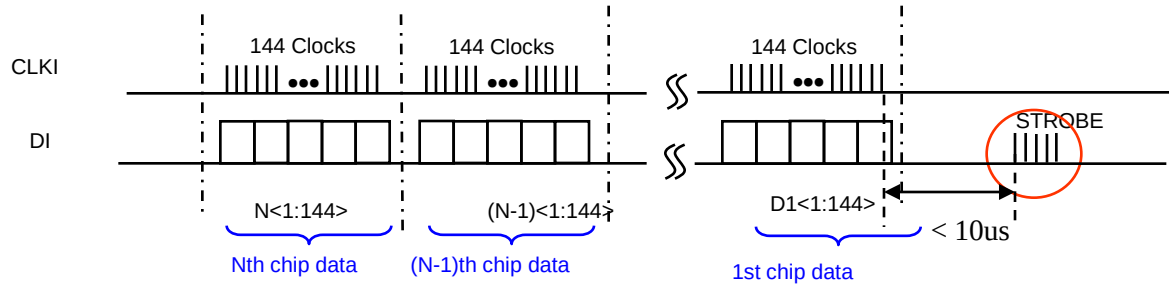
COMMUNICATION MODE TIMING DIAGRAM

Case of N chips

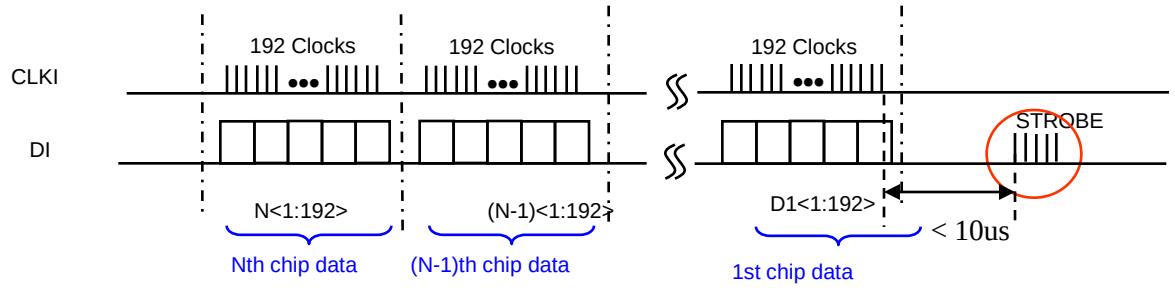
8bit Mode, 12 Channel (MOD2=L, MOD1 = L, CH2=L,CH1 = L)



12bit Mode, 12 Channel (MOD2 = L, MOD1=H, CH2 = L, CH1 = L)



16bit Mode, 12 Channel (MOD2 = H, MOD1=L, CH2 = L, CH1 = L)



When multichips are connected in series, strobe signal shall be applied after Nchip X Nbit X 12 ea of clock input.

**Note) Apply the strobe signal after minimum 10us from the rising edge of last clock

ROUT1, ROUT2, ROUT3, ROUT4
GOUT1, GOUT2, GOUT3, GOUT4
BOUT1,BOUT2, BOUT3, BOUT4

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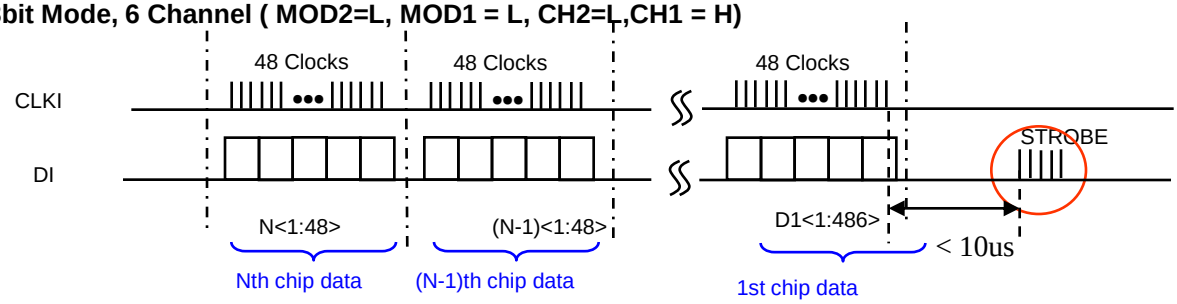
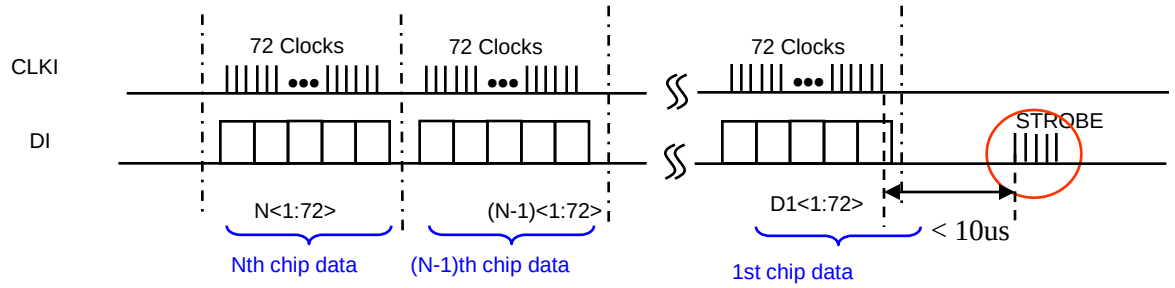
COMMUNICATION MODE TIMING DIAGRAM

Case of N chips

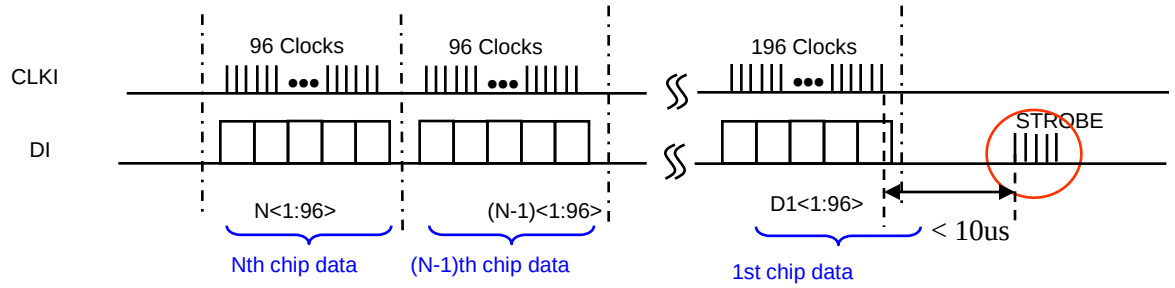
8bit Mode, 6 Channel (MOD2=L, MOD1 = L, CH2=L,CH1 = H)



12bit Mode, 6 Channel (MOD2 = L, MOD1=H, CH2 = L, CH1 = H)



16bit Mode, 6 Channel (MOD2 = H, MOD1=L, CH2 = L, CH1 = H)



When multichips are connected in series, strobe signal shall be applied after Nchip XNbit X 6 ea of clock input.

**Note) Apply the strobe signal after minimum 10us from the rising edge of last clock

ROUT1= ROUT2, ROUT3= ROUT4
GOUT1= GOUT2, GOUT= GOUT4
BOUT1=BOUT2, BOUT3= BOUT4

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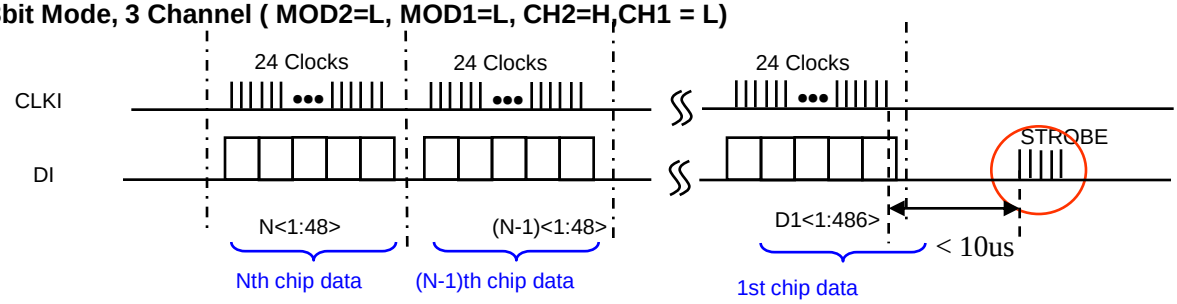
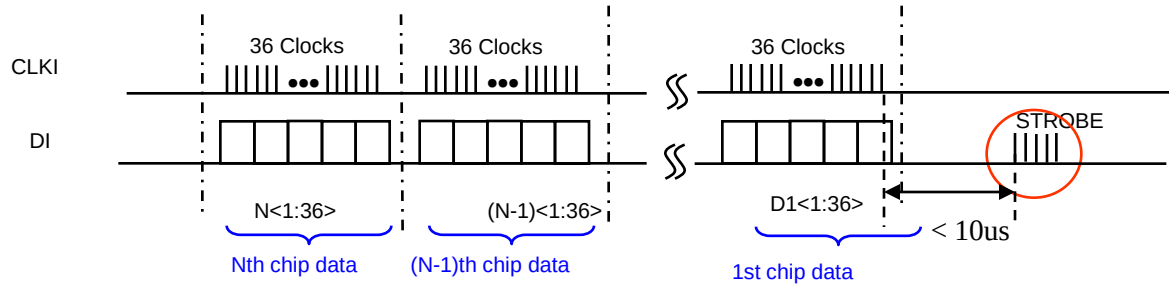
COMMUNICATION MODE TIMING DIAGRAM

Case of N chips

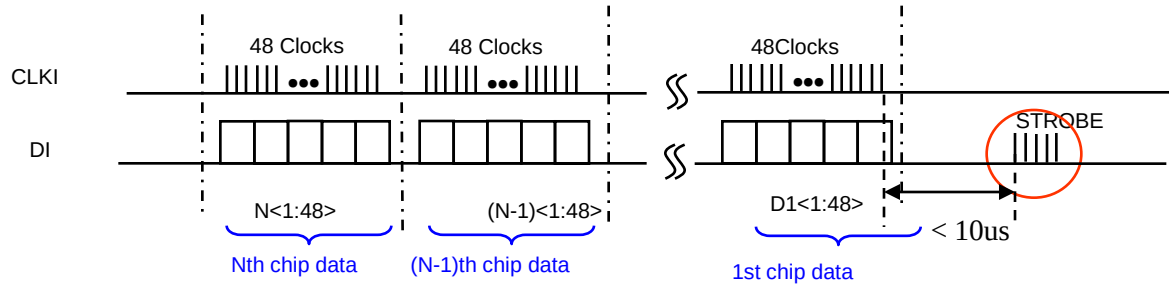
8bit Mode, 3 Channel (MOD2=L, MOD1=L, CH2=H,CH1 = L)



12bit Mode, 3 Channel (MOD2 = L, MOD1=H, CH2 = H, CH1 = L)



16bit Mode, 3 Channel (MOD2 = H, MOD1=L, CH2 = H, CH1 = L)



When multichips are connected in series, strobe signal shall be applied after Nchip X Nbit X 3 ea of clock input.

**Note) Apply the strobe signal after minimum 10us from the rising edge of last clock

ROUT1= ROUT2=ROUT3= ROUT4
GOUT1= GOUT2=GOUT= GOUT4
BOUT1=BOUT2=BOUT3= BOUT4

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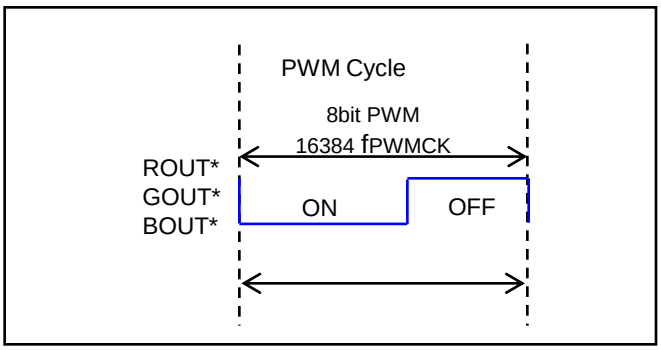
PWM DISPLAY CYCLE

The LD1512 implements the 8bit/12bit/16bit gray level of each output port using the 4 PWM sub cycles. Sub-cycle is consisted of 4096 fPWMCK clocks. This enhancement provides a excellent energy distribution in lighting the LED and increases the visual refresh rate and reduces the flickers.

8bit Operation

D[7:0] : Display Data(8 bit Gray Scale Data)



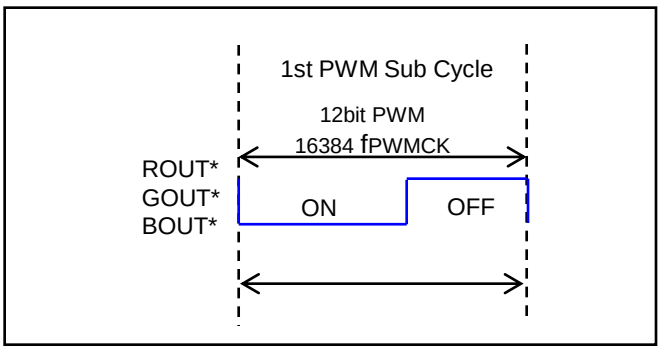
*) ROUT = ROUT1~4, GOUT=GOUT1~4, BOUT= BOUT1~4

64 fPWMCK=1Bit

12bit Operation

D[11:0] : Display Data(12 bit Gray Scale Data)

The following examples show the PWM timing diagram for different display data.



*) ROUT = ROUT1~4, GOUT=GOUT1~4, BOUT= BOUT1~4

4 fPWMCK=1Bit

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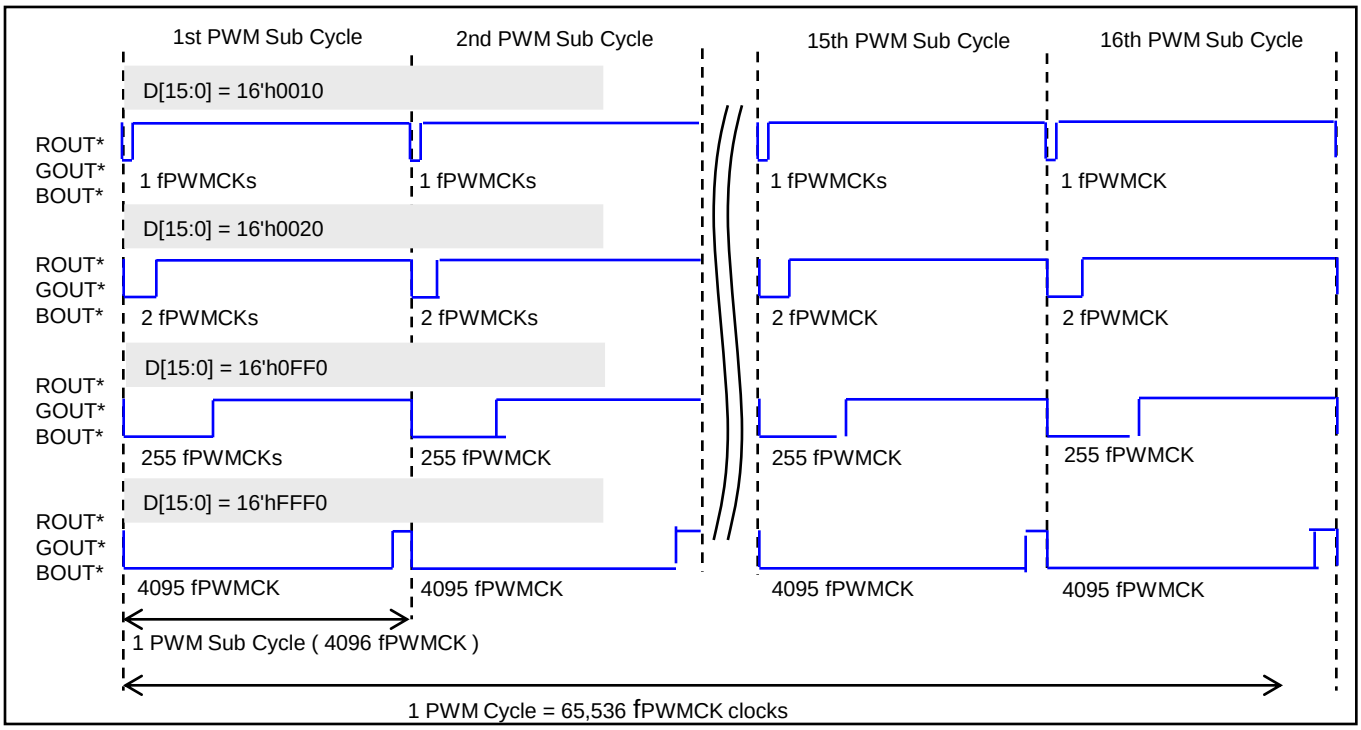
16bit Operation

D[15:0] : Display Data(16 bit Gray Scale Data)

The following examples show the PWM timing diagram for different display data.
1PWM Cycle is made by 16 sub cycle.



*) ROUT = ROUT1~4, GOUT=GOUT1~4, BOUT= BOUT1~4

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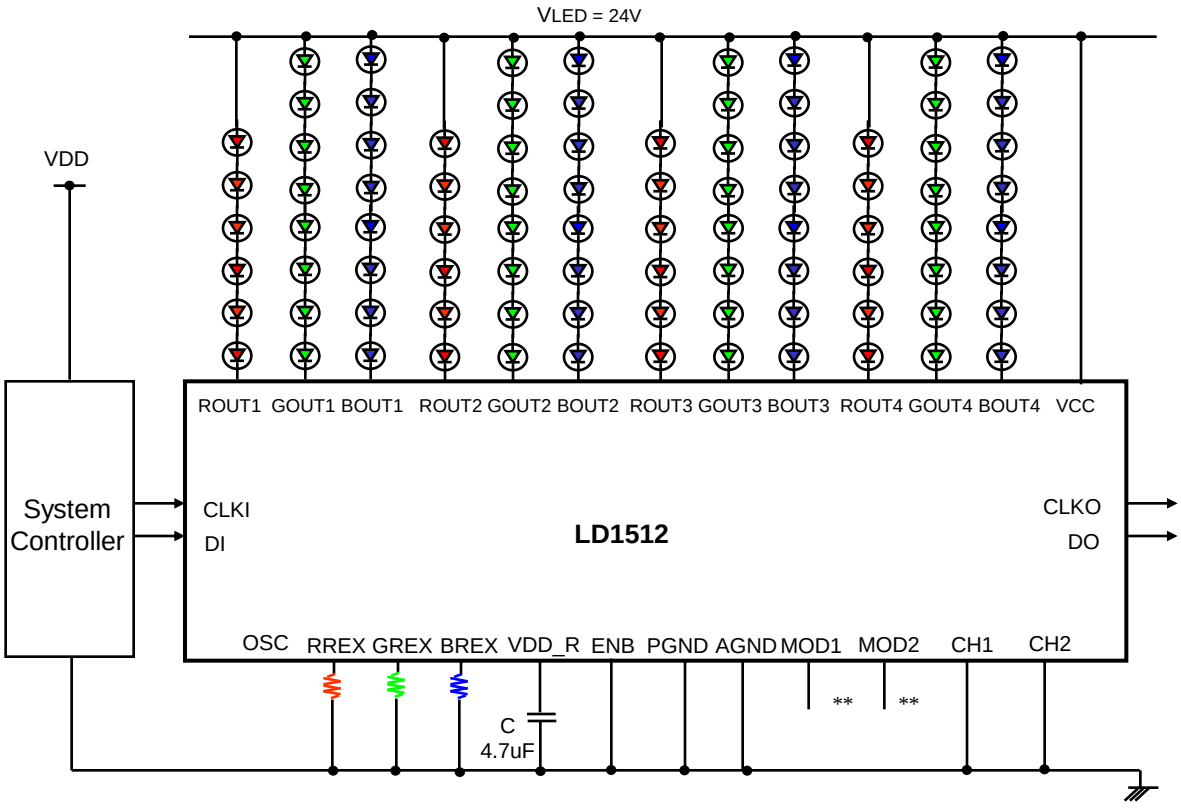
TYPICAL APPLICATION

1) VLED = 24V, 8bit/12bit/16bit PWM, 12Channel (if RLED VF=3.4V, GLED VF=2.8V, BLED VF=2.6V)



주(**)

8bit PWM Mode

MOD2=GND, MOD1=GND

12 bit PWM Mode

MOD2=GND, MOD1=VDD_R

16 bit PWM Mode

MOD2=VDD_R, MOD1=VDD_R

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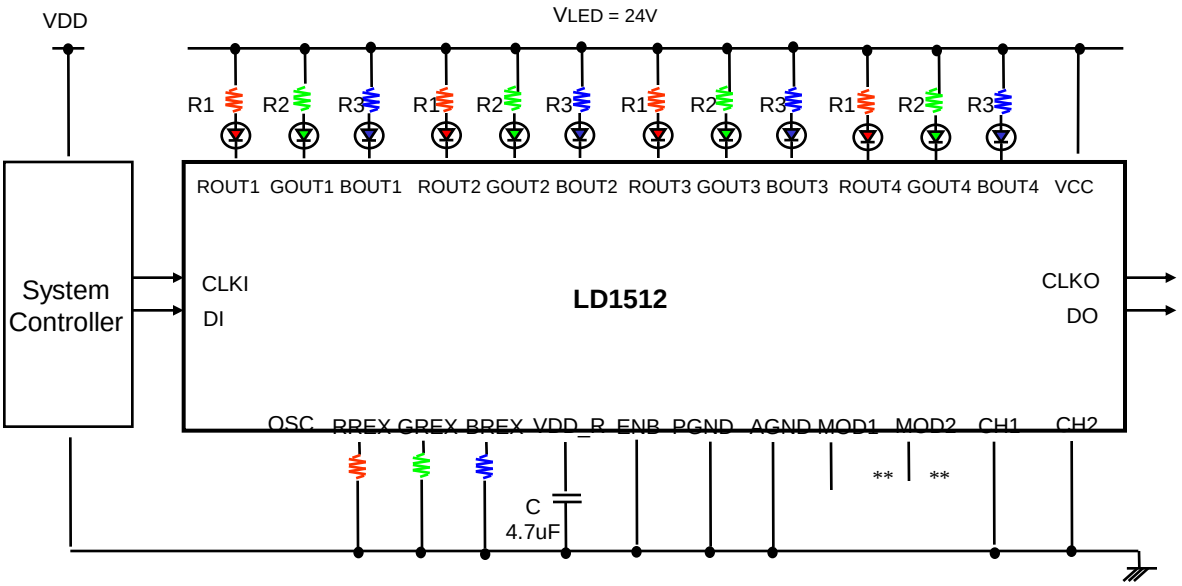
TYPICAL APPLICATION

2) VLED = 24V, 8bit PWM, 12Channel (if RLED VF=3.4V, GLED VF=2.8V, BLED VF=2.6V)



주(**)

8bit PWM Mode

MOD2=GND, MOD1=GND

12 bit PWM Mode

MOD2=GND, MOD1=VDD_R

16 bit PWM Mode

MOD2=VDD_R, MOD1=VDD_R

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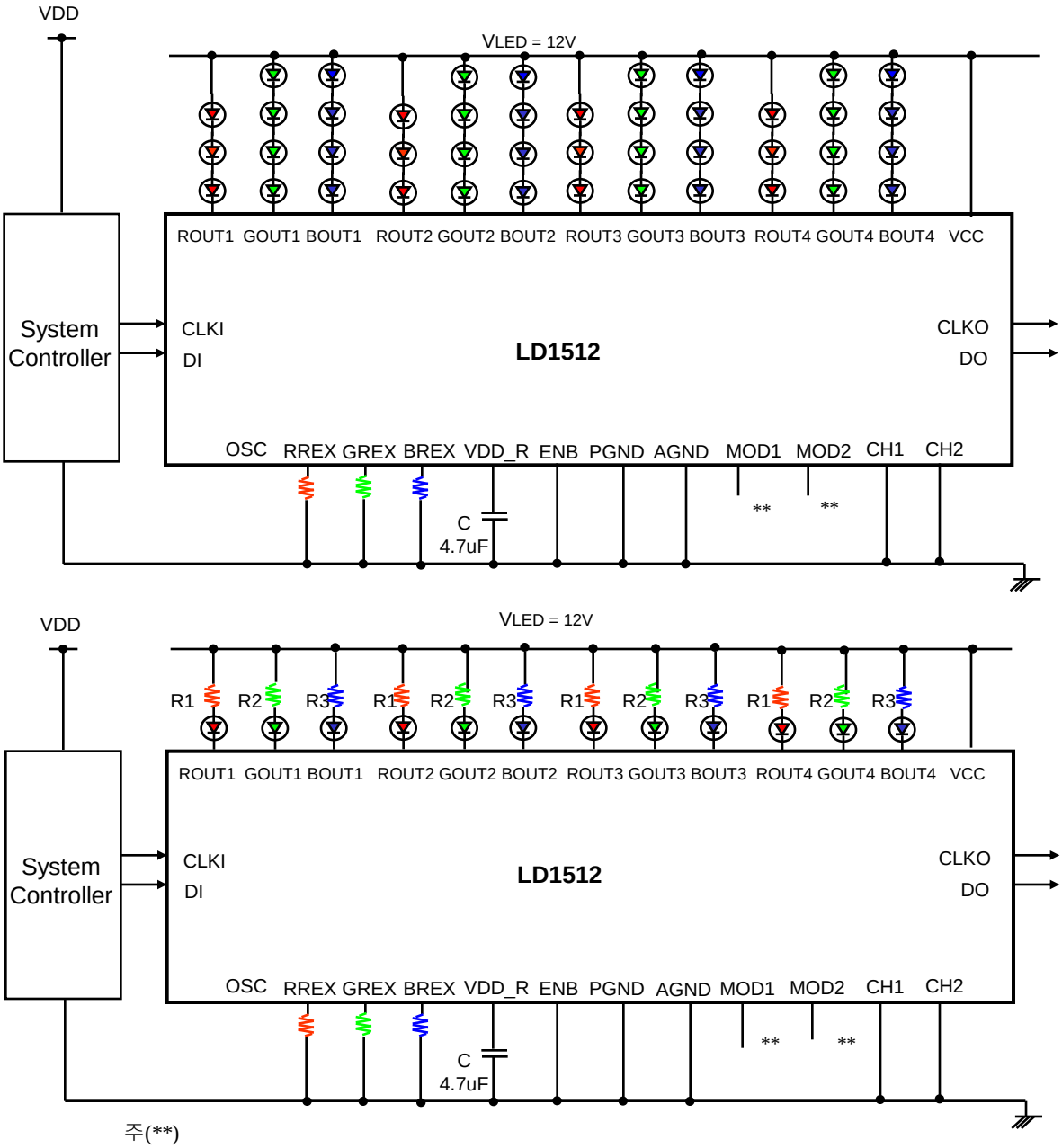
TYPICAL APPLICATION

3) VLED = 12V, 8bit PWM, 12 Channel (if RLED VF=3.4V, GLED VF=2.8V, BLED VF=2.6V)



주(**)

8bit PWM Mode

MOD2=GND, MOD1=GND

12 bit PWM Mode

MOD2=GND, MOD1=VDD_R

16 bit PWM Mode

MOD2=VDD_R, MOD1=VDD_R

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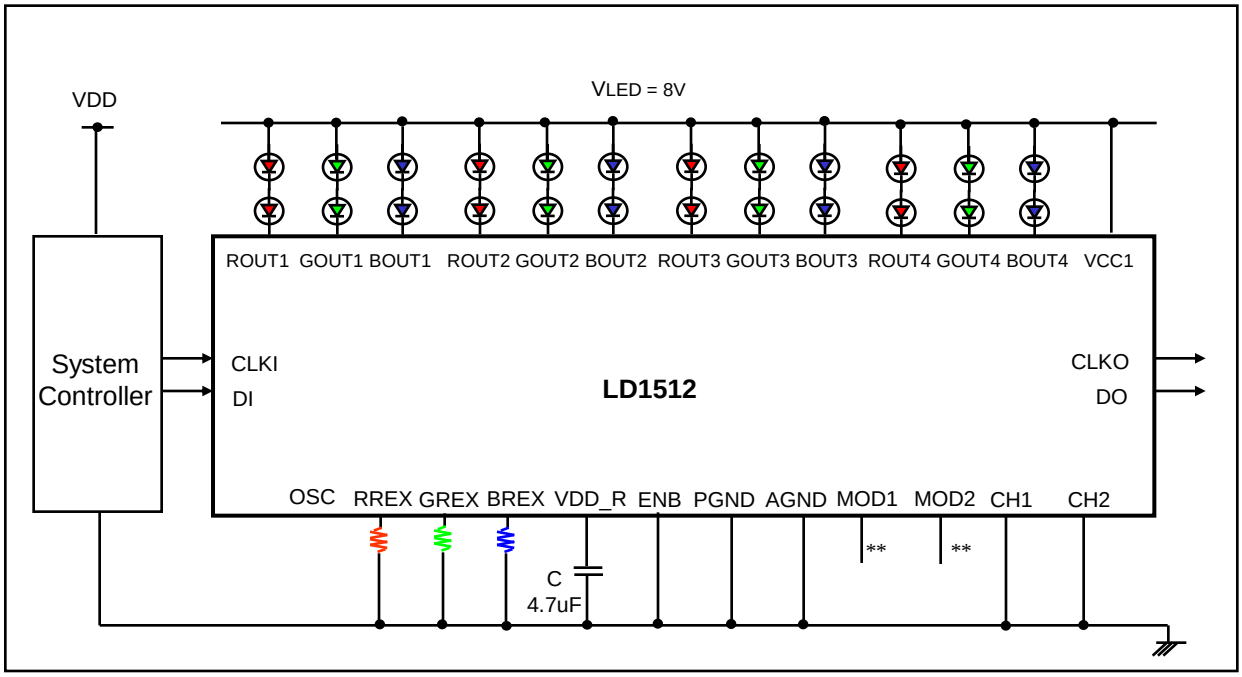
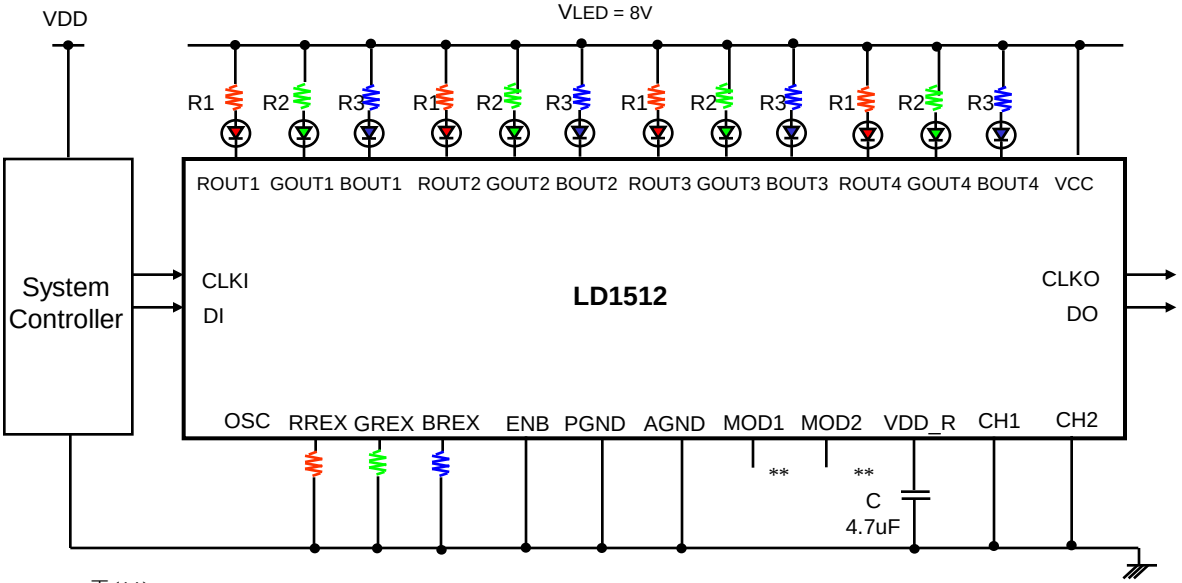
TYPICAL APPLICATION

4) VLED = 8V, 8bit/12bit/16bit PWM, 12 Channel (if RLED VF=3.4V, GLED VF=2.8V, BLED VF=2.6V)





주(**)

8bit PWM Mode

MOD2=GND, MOD1=GND

12 bit PWM Mode

MOD2=GND, MOD1=VDD_R

16 bit PWM Mode

MOD2=VDD_R, MOD1=VDD_R

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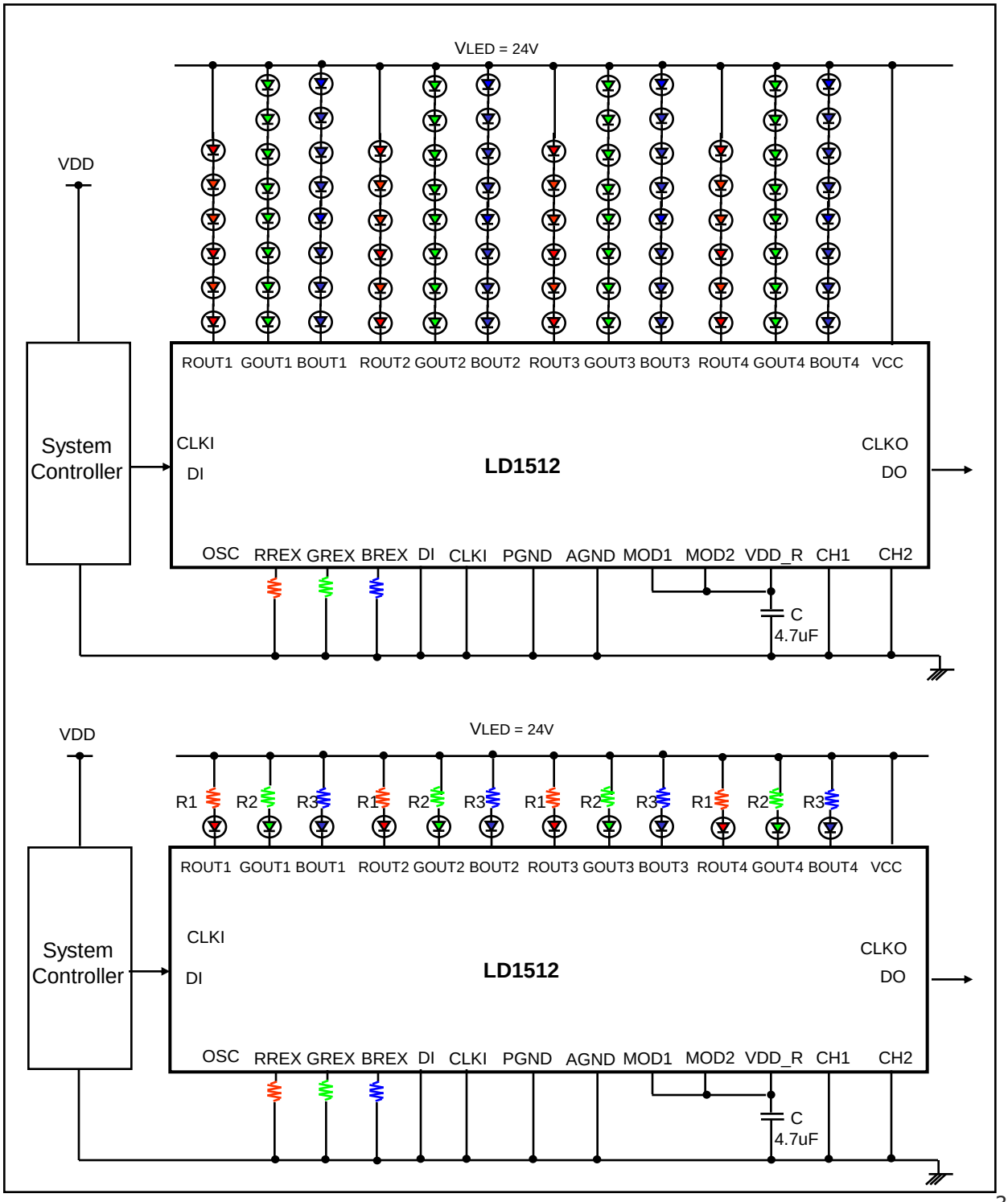
TYPICAL APPLICATION

5) VLED = 24V, All on by DI, 12 Channel (if RLED VF=3.4V, GLED VF=2.8V, BLED VF=2.6V)



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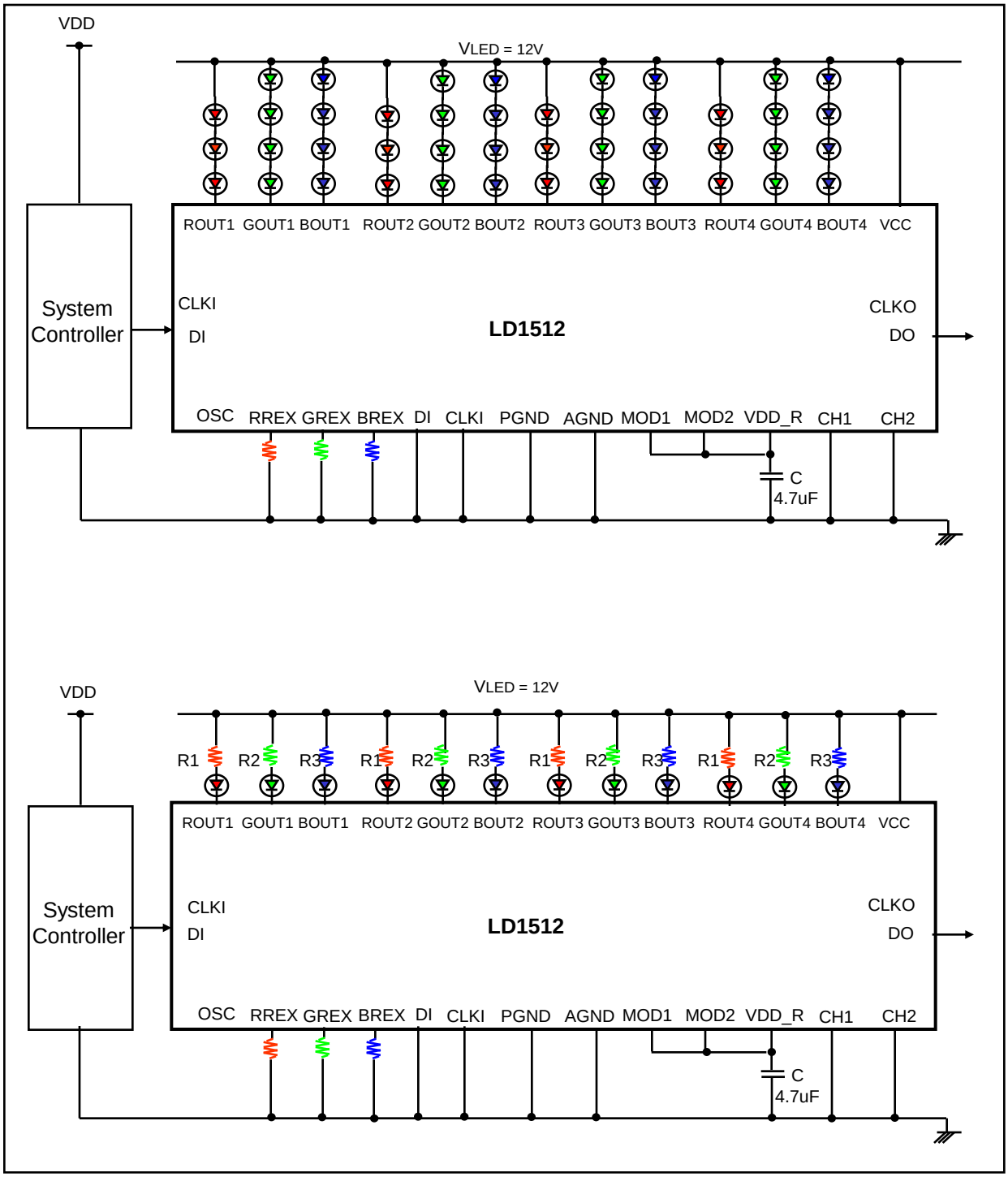
TYPICAL APPLICATION

6) VLED = 12V, All on by DI, 12 Channel (if RLED VF=3.4V, GLED VF=2.8V, BLED VF=2.6V)



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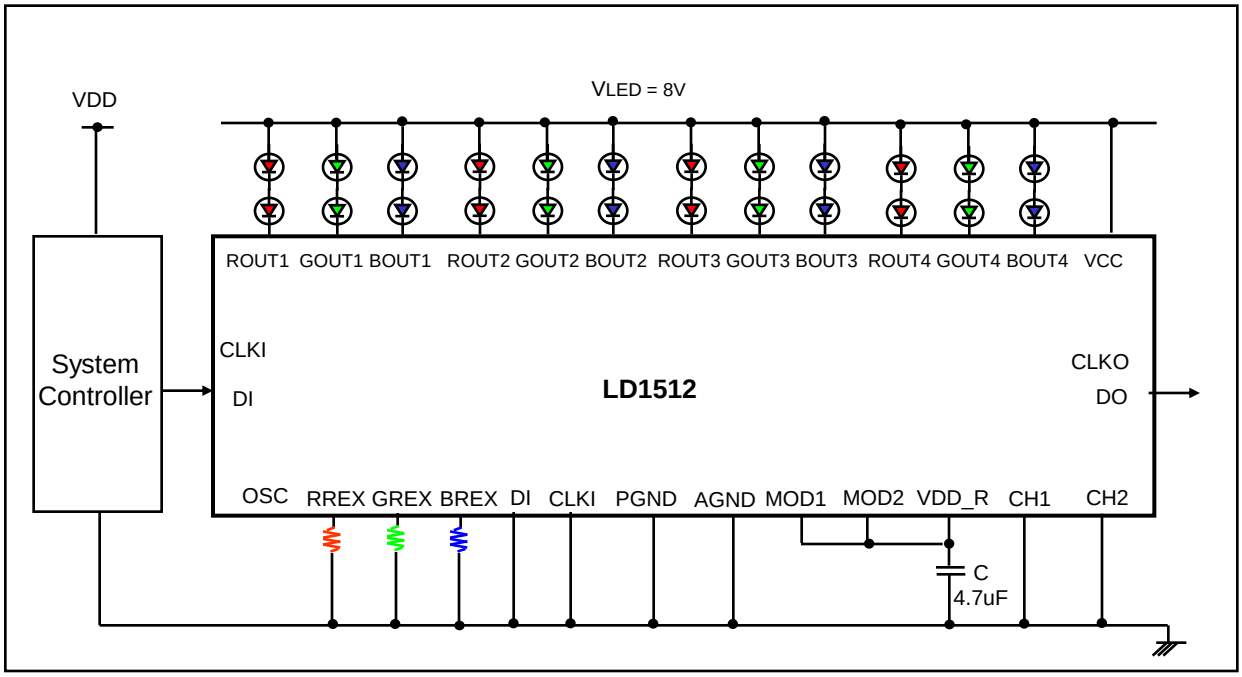
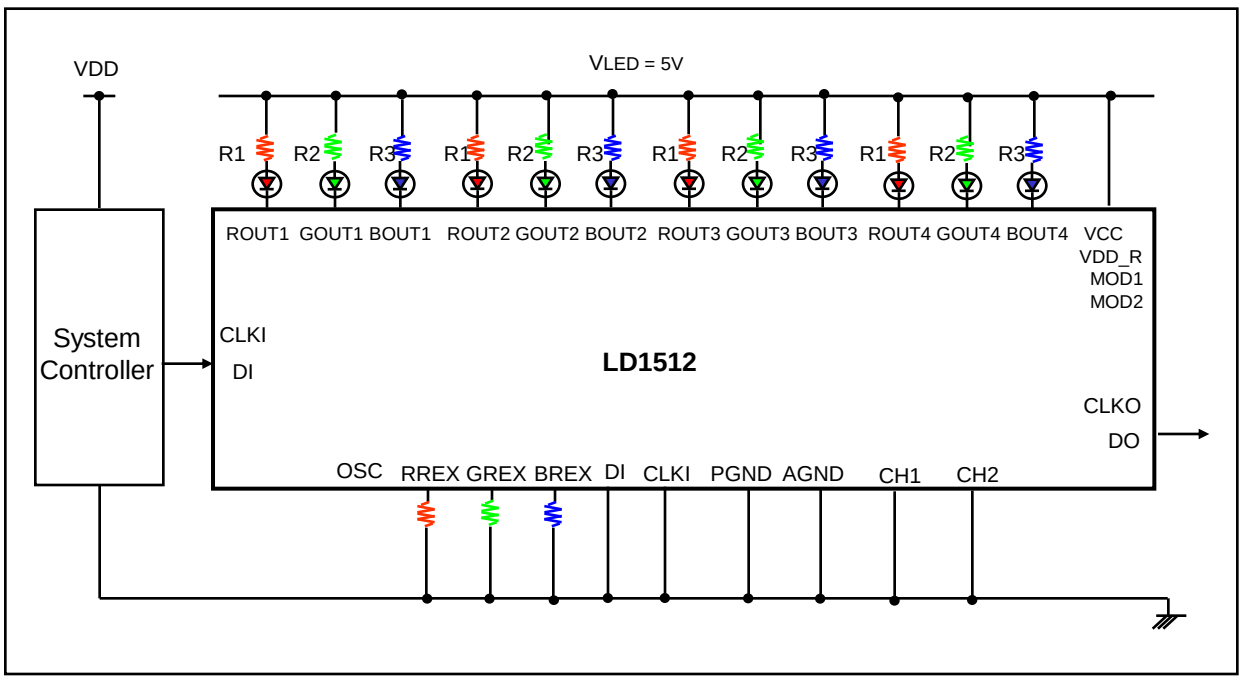
TYPICAL APPLICATION

7) VLED = 8V, All on by DI, 12 Channel (if RLED VF=3.4V, GLED VF=2.8V, BLED VF=2.6V)



16) VLED = 5V, All on by ENB, 12 Channel (if RLED VF=3.4V, GLED VF=2.8V, BLED VF=2.6V)



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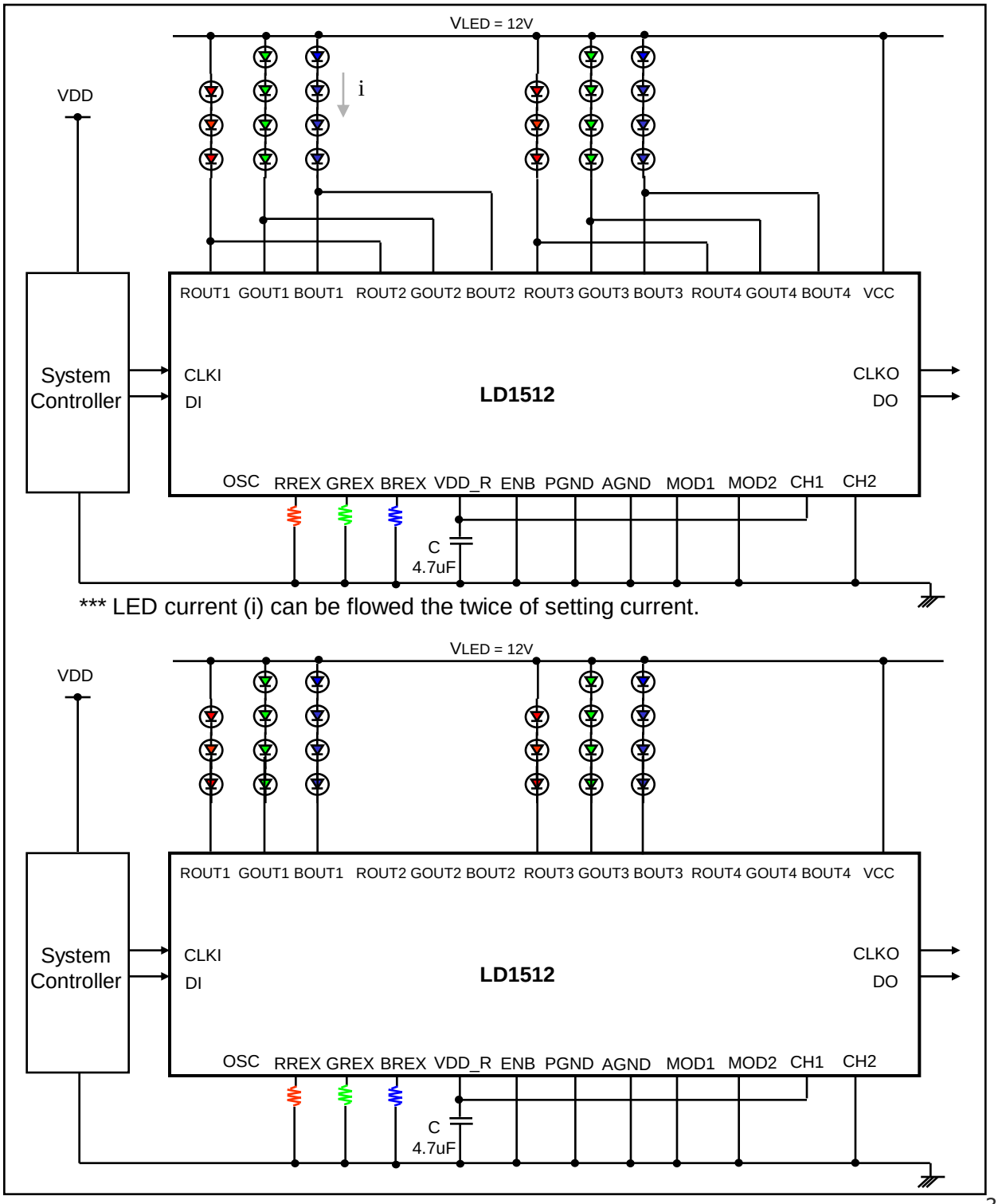
TYPICAL APPLICATION

8) VLED = 12V, 8bit PWM, 6 Channel (if RLED VF=3.4V, GLED VF=2.8V, BLED VF=2.6V)



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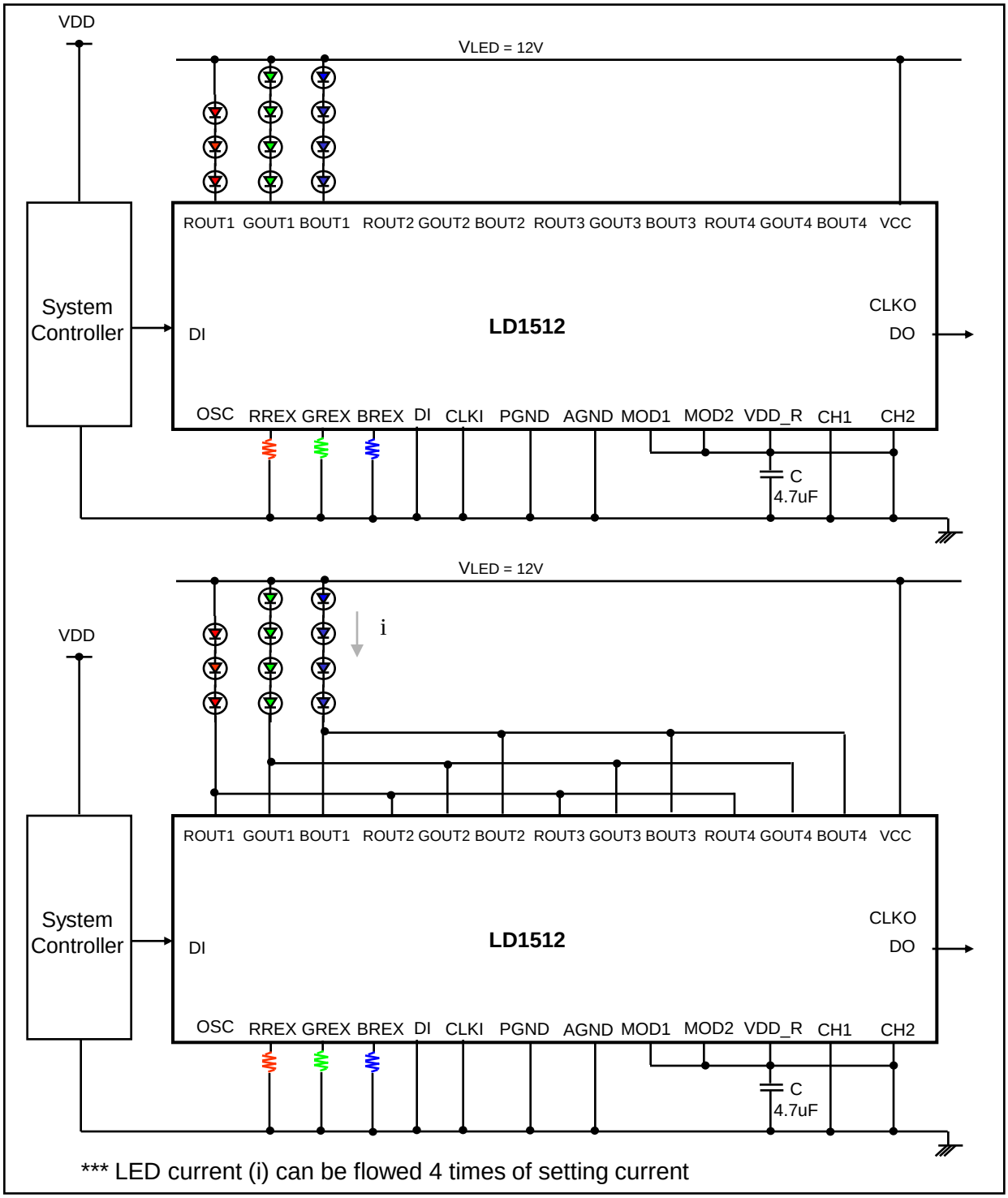
TYPICAL APPLICATION

9) VLED = 12V, All on by DI, 3 Channel (if RLED VF=3.4V, GLED VF=2.8V, BLED VF=2.6V)



*** LED current (i) can be flowed 4 times of setting current

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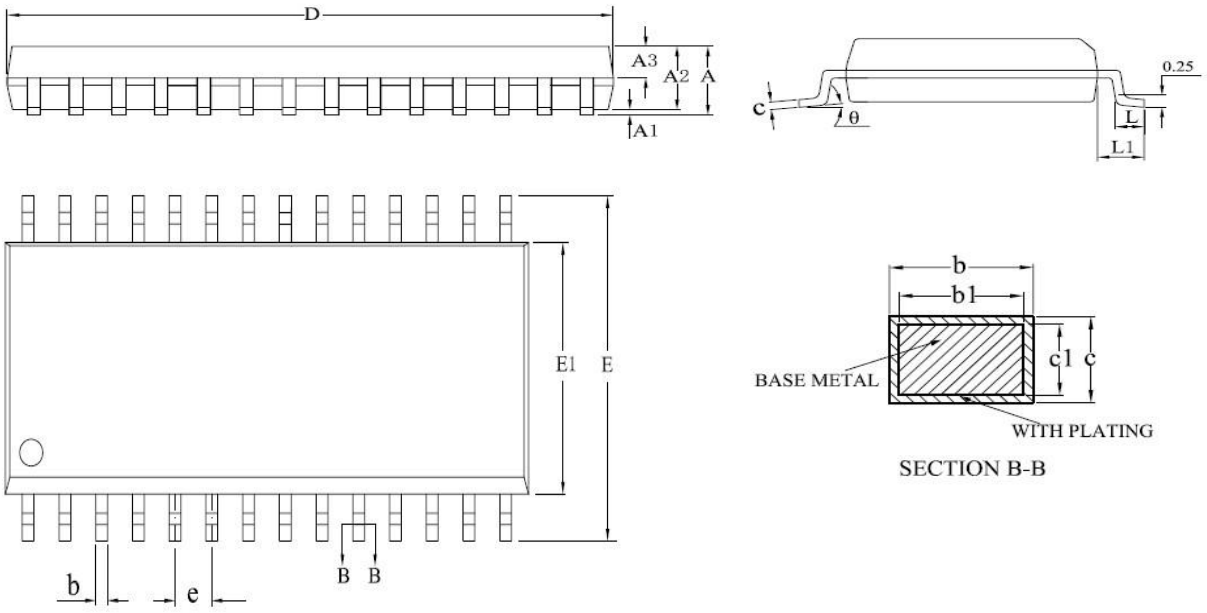
SOP28



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.70
A1	0.10	—	0.28
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	—	0.48
b1	0.38	0.41	0.43
c	0.25	—	0.31
c1	0.24	0.25	0.26
D	17.89	18.09	18.29
E	10.10	10.30	10.50
E1	7.30	7.50	7.70
e	1.27BSC		
L	0.70	—	1.00
L1	1.40BSC		
θ	0	—	8°

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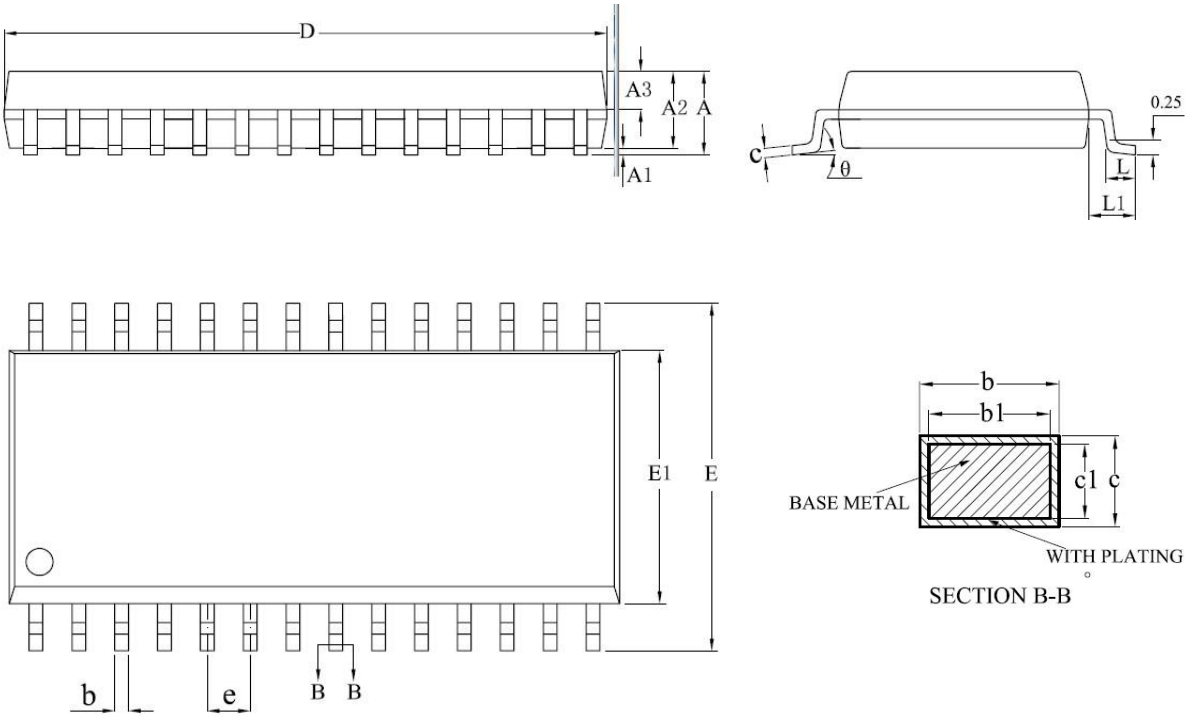
SSOP28



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.00
A1	0.05	—	0.25
A2	1.65	1.75	1.85
A3	0.75	0.80	0.85
b	0.29	—	0.37
b1	0.28	0.30	0.33
c	0.15	—	0.20
c1	0.14	0.15	0.16
D	10.00	10.20	10.40
E	7.60	7.80	8.00
E1	5.10	5.30	5.50
e	0.65BSC		
L	0.75	—	1.05
L1	1.25BSC		
θ	0	—	8°

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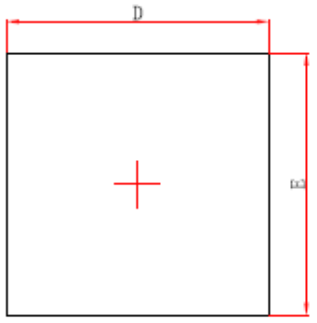
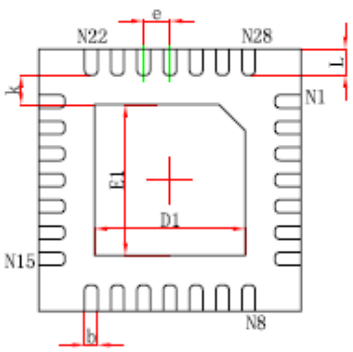
QFN 28

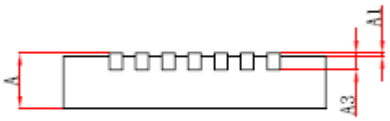
QFNWB4×4-28L(P0.40T0.75/0.85) PACKAGE OUTLINE DIMENSIONS



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.950	4.050	0.156	0.159
E	3.950	4.050	0.156	0.159
D1	2.200	2.400	0.087	0.094
E1	2.200	2.400	0.087	0.094
k	0.200MIN.		0.008MIN.	
b	0.150	0.250	0.006	0.010
e	0.400TYP.		0.016TYP.	
L	0.324	0.476	0.013	0.019

January 2010,Rev.A

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