LD1510

3Channel Output LED Driver with 12 bit PWM Controller

Ver. 3.0 / Feb. 2009

LDT Inc. Mplaza 3F, 538, Dujeong-dong, Seobuk-gu, Cheonan, Chungnam, 331-958, Korea
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Data Sheet

2009.02.17

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LD1510 Revision History

Version	Contents	Date
1.0	- First Version	2008.10.21
2.0	- Second Version Revised items ; (page 7) 'Twsh min= 100ns' is revised to '100 + N x 1ns' 'Twsl min= 100ns' is revised to '100 + N x 1 ns' (page 8) Strobe Transmit 'DI : 2 times toggle when CLKI=L' is revised to 'DI : 5 times toggle when CLKI=L' 'Strobe Diagram' is revised to new one (page 14, 15) 'COMMUNICATION MODE TIMING DIAGRAM' Is revised to new one '8Bit Mode & 12 Bit Mode' Is revised to new one Added items ; (page 7) Twss min= 10,000ns	2009.1.12
3.0	Deleted item ; (page 17) 'WRITING THE DISPLAY DATA' Revised items ; (page 16) '1 PWM Cycle(8bit PWM Display=16384 PWMCK clocks=256x4X4Clk)' Is revised to '1 PWM Cycle(8bit PWM Display=4096 PWMCK clocks=256x4X4Clk)' (page 17, 18) '1 PWM Cycle (= 14096 PWMCKs = 1024 x 4)' Is revised to '1 PWM Cycle (12 bit PWM Display = 4096 PWMCK clocks = 1024 x 4)'	2009.1.30
4.0	Revised items ; (page 3) 'Maximum serial input frequency : 20MHz ' Is revised to 'Maximum serial input frequency : 10MHz)' (page 5) 'CLKI Frequency 20MHZ ' Is revised to 'CLKI Frequency 10MHZ ' (page 22) Change 'TIMING DIAGRAM Data Transmission : Strobe Number ' (page 14) Change 'TIMING DIAGRAM : CLK Number '	2009.2.17

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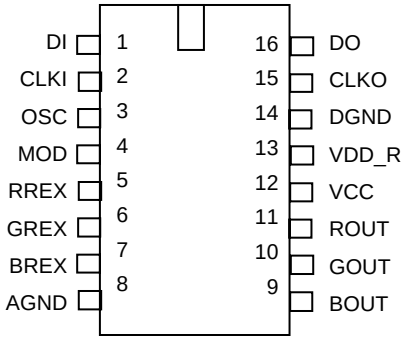
DESCRIPTION

The LD1510 is specifically designed for LED lighting or display applications. The 3-channel constant output current is controlled by 3 external resistors (IOUT = 5mA to 100mA). The device consists of 3 x 12 bit shift register, latches, built-in OSC, 3 constant current drivers and 8/12 bit PWM controller.
The main applications are decorative LED lighting, indoor/outdoor LED video or message display systems.

FEATURES

- **Output current : set-up at 5mA to 100mA**
- **8/12bit grayscale PWM control with three external resistors**
- **Maximum sinking output voltage : 17V**
- **5.0V CMOS compatible input**
- **Package : SOP16, SSOP16**
- **Maximum serial input frequency : 10MHz**
- **Built in internal RC oscillator**

PIN CONFIGURATION



ORDERING INFORMATION

PART NUMBER	PACKAGE	TA
LD1510-SS	16 SSOP	-40°C to 85 °C
LD1510-SP	16 SOP	-40°C to 85 °C

PIN DESCRIPTION

PIN NO	PIN NAME	DESCRIPTION
1	DI	Serial data input terminal
2	CLKI	Serial input clock terminal
3	OSC	Test only - Floating pin
4	MOD	Input data transfer mode selection. L : 8bit luminance data transfer. H : 12bit luminance data transfer
5-7	R/G/BREX	External resistors are connected between those pins and GND for driver current setting.
8	AGND	Analog GND terminal
9-11	B/G/ROUT	Constant current output terminals
12	VCC	LED driving voltage
13	VDD_R	Regulator output voltage
14	DGND	Digital GND terminal
15	CLKO	Serial clock output terminal
16	DO	Serial data output when CLKI is ‘H”, strobe transmit when CLKI is “L”.

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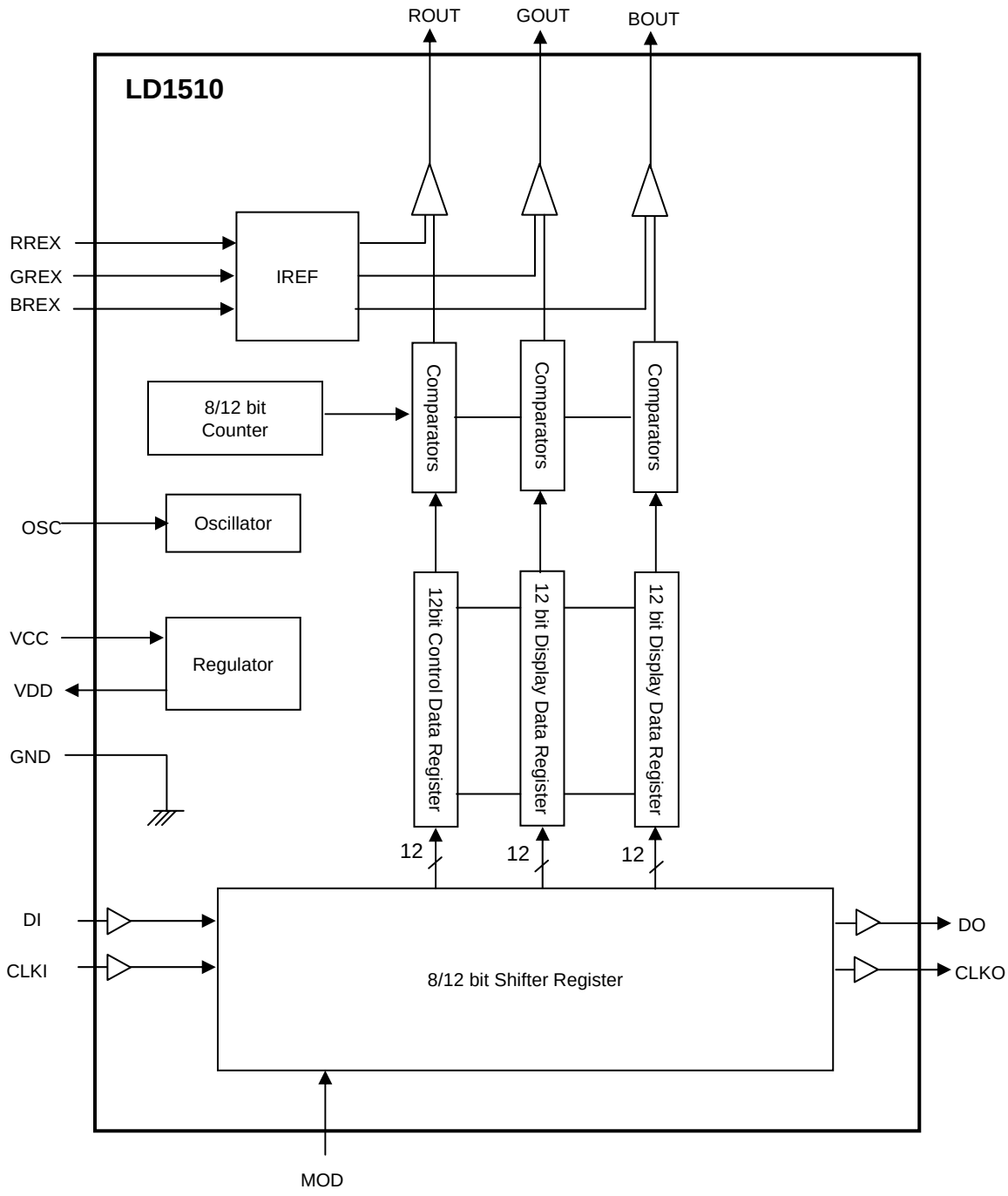
BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	0~20	V
Regulator Voltage	V_{DD}	0~6.5	V
Output Voltage	V_{OUT}	-0.5~20	V
Output Current	I_{OUT}	100	mA
Input Voltage	V_{IN}	-0.4~V_{DD}+0.4	V
GND Terminal Current	I_{GND}	400	mA
CLKI Frequency	f_{CK}	10	MHz
Internal PWM Clock Frequency	fPWMCK	12	MHz
Power Dissipation	P_D	0.35	W
Operating Temperature	T_{opr}	-40~85	ºC
Storage Temperature	T_{stg}	-55~150	ºC

(Note) Ambient temperature delated above 25ºC in the proportion of 14.2mW/ ºC

RECOMMENDED OPERATING CONDITIONS

Ta = 25ºC

DC CHARACTERISTICS		SYMBOL	MIN.	TYP.	MAX.	UNIT
VCC Supply Voltage		V_{cc}	4.5	15	18	V
LED Driver Output Voltage		V_{OUT}			18	V
VDD Regulator Voltage or External Supply Voltage		V_{DD}	4.5	5.0	5.5	V
Input Voltage	"H" Level	V_{IH}	0.8V_{DD}	-	V_{DD}	V
	"L" Level	V_{IL}	GND	-	0.2V_{DD}	
Output Voltage	DO,CLKO	V_{OL}	-	-	0.2V_{DD}	V
		V_{OH}	0.8V_{DD}	-	-	
High Level Output Current		I_{OH}	-1			mA
Low Level Output Current		I_{OL}			1	mA
LED Driver Output Current		I_{OUT}			100	mA
Operating Free-air Temperature Range			-40		85	ºC
AC CHARACTERISTICS		**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
CLKI Frequency		f_{CK}			10	MHz
Internal PWM Clock Frequency		f_{PWMCK}	8	10	12	MHz
Pulse Width	CLKI	t_{WH0} / t_{WL0}	20			ns
Setup Time		t_{setup}	15			ns
Hold Time		t_{hold}	15			ns

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ELECTRICAL CHARACTERISTICS

(VDD = 5V, Ta = 25ºC)

PARAMETER		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VCC Supply Voltage		VCC		4.5	15	18	V
VDD Regulator Voltage or External Supply Voltage		VDD		4.5	5.0	5.5	V
Input Voltage	H Level	VIH	-	0.8VDD		VDD	V
	L Level	VIL	-	GND		0.2VDD	
Output Leakage Current		IOZ	VOH=6.0V			1	uA
Output Voltage	DO,CLKO	VOL	IOL=1mA			0.2VDD	V
		VOH	IOH=1mA	0.8VDD			
Output Current1 Pin to Pin Deviation		IOLPP1	REXT=500Ω IOUT=100mA, VOUT=1.5V		±1.5	±3.0	%
Output Current2 Pin to Pin Deviation		IOLPP2	REXT=1000Ω IOUT=50mA, VOUT=1.5V		±1.5	±3.0	%
Output Current1 Chip to Chip Deviation		IOLCC1	REXT=500Ω IOUT=100mA, VOUT=1.5V		±3.0	±6.0	%
Output Current1 Chip to Chip Deviation		IOLCC2	REXT=1000Ω IOUT=50mA, VOUT=1.5V		±3.0	±6.0	%
Supply Voltage Regulation		%/VDD	REXT=1000Ω		±0.5	±1.0	%/V
Supply Current		I_{CC1}	REXT=Open, OUTn=OFF PWM=Gray0	-	1.0	2.0	mA
		I_{CC2}	REXT=500Ω, OUTn=OFF PWM=Gray0	-	5.0	7.0	
		I_{CC3}	REXT=1000Ω, OUTn=OFF PWM=Gray0	-	4.0	6.0	

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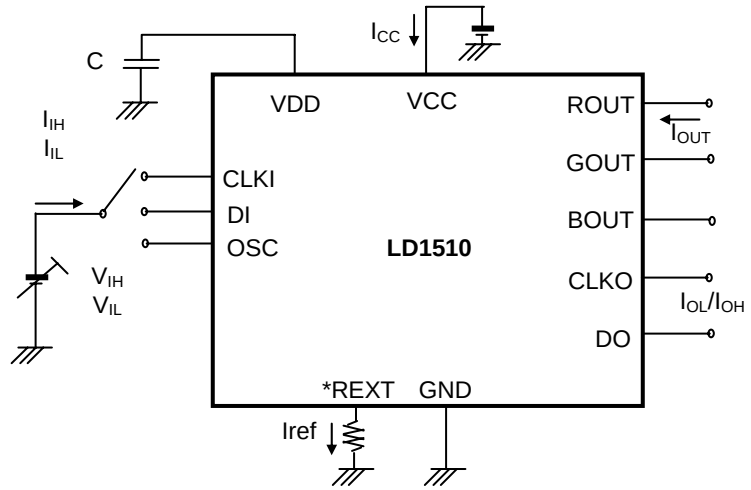
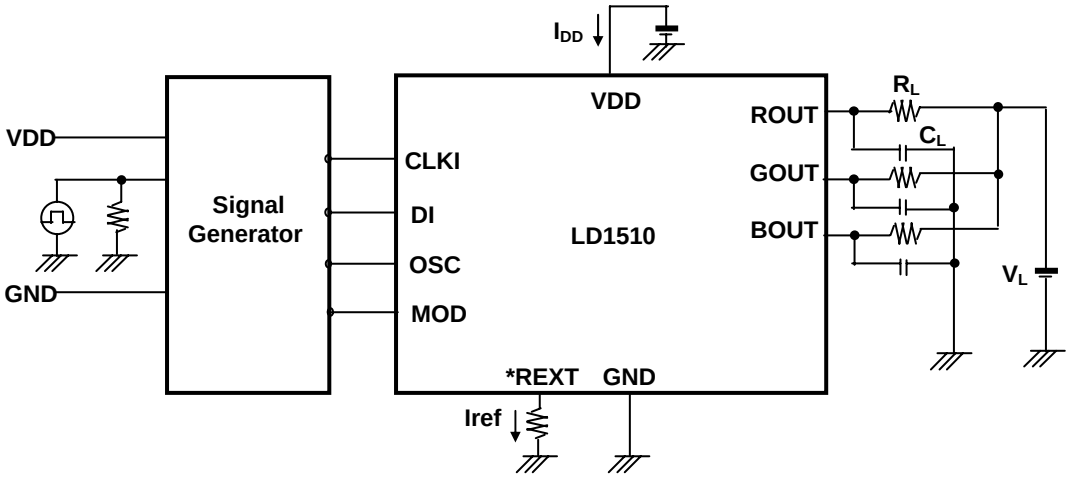
DC CHARACTERISTIC TEST CIRCUIT



NOTE *REXT = RREX,GREX,BREX

AC CHARACTERISTIC TEST CIRCUIT



NOTE *REXT = RREX,GREX,BREX

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AC CHARACTERISTICS

(Ta = 25°C unless otherwise noted)

PARAMETER		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	CLKI-DO	t_{PLH}	V_{DD} = 5.0V V_{IH} = VDD V_{IL} = GND f_{CK} = 10MHz R_{EXT} = 2.50kΩ I_{OUT} = 19.1㎃ C_L = 10.0pF R_L = 150Ω VL = 4.5V	-	13	20	ns
Propagation Delay Time ("H" to "L")	CLKI-DO	t_{PHL}		-	13	20	ns
Maximum CLKI Frequency		f_{CKMAX} (*1)		0.5	8	10	MHz
Pulse Width	CLKI	t_{WH0} / t_{WL0}		40	-	-	ns
		t_{WH1}		40	-	-	ns
Data Setup Time		t_{setup}		18	-	-	ns
Data Hold Time		t_{hold}		30	-	-	
DI Width		twsh		100 + 1 x N (*2)	-	-	ns
		twsl		100 + 1 x N (*2)	-	-	
		twss		10,000 (*3)	-	-	
Clock Delay	CLKO	t_{CKD}		-	13	-	ns
Clock Width	CLKO	t_W		-	45	-	ns
Clock Cycle	CLKO	t_{CY}		100	-	2000	ns
Maximum Clock Rise Time		t_r		-	-	10	ns
Maximum Clock Fall Time		t_f		-	-	10	
Minimum Output Rise Time		t_{or}		-	300		ns
Minimum Output Fall Time		t_{of}		-	150		

***1 : Cascade Operation**
***2 : N= Number of Chips in Serial**
***3 : N= 2000ea**

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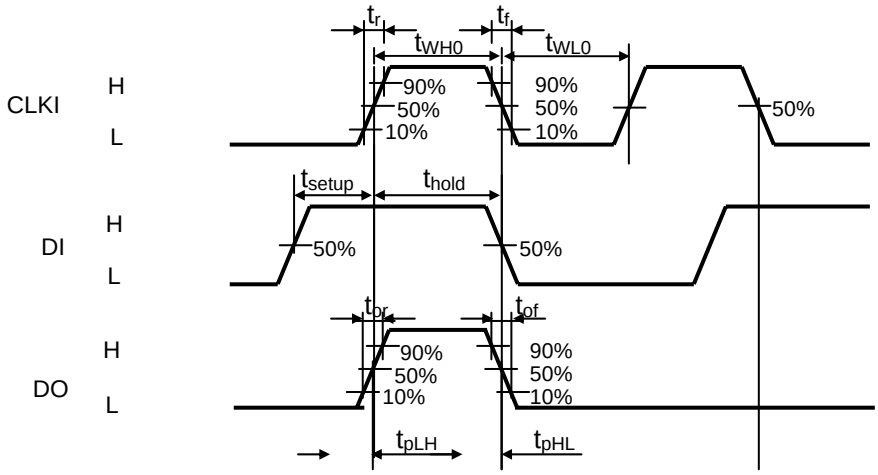
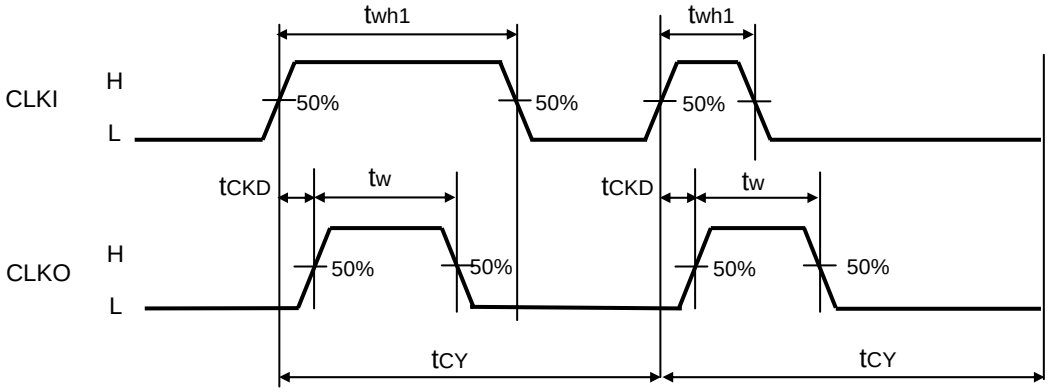
TIMING WAVEFORM

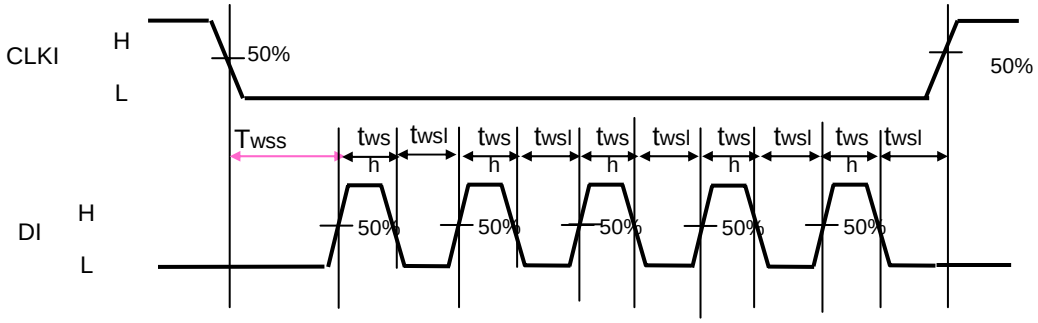
CLKI, DI, DO (Data Transmit)



CLKI, CLKO



CLKI, DI (Strobe Transmit)



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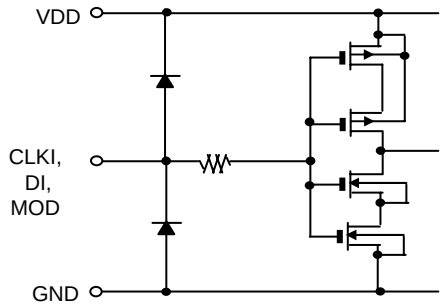
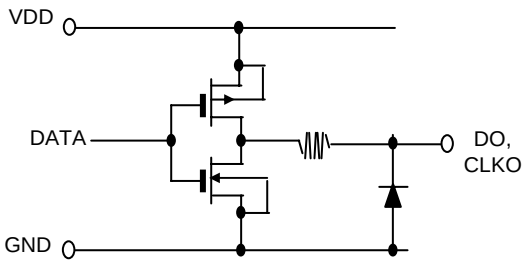
EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

CLKI, DI terminal



DO, CLKO terminal

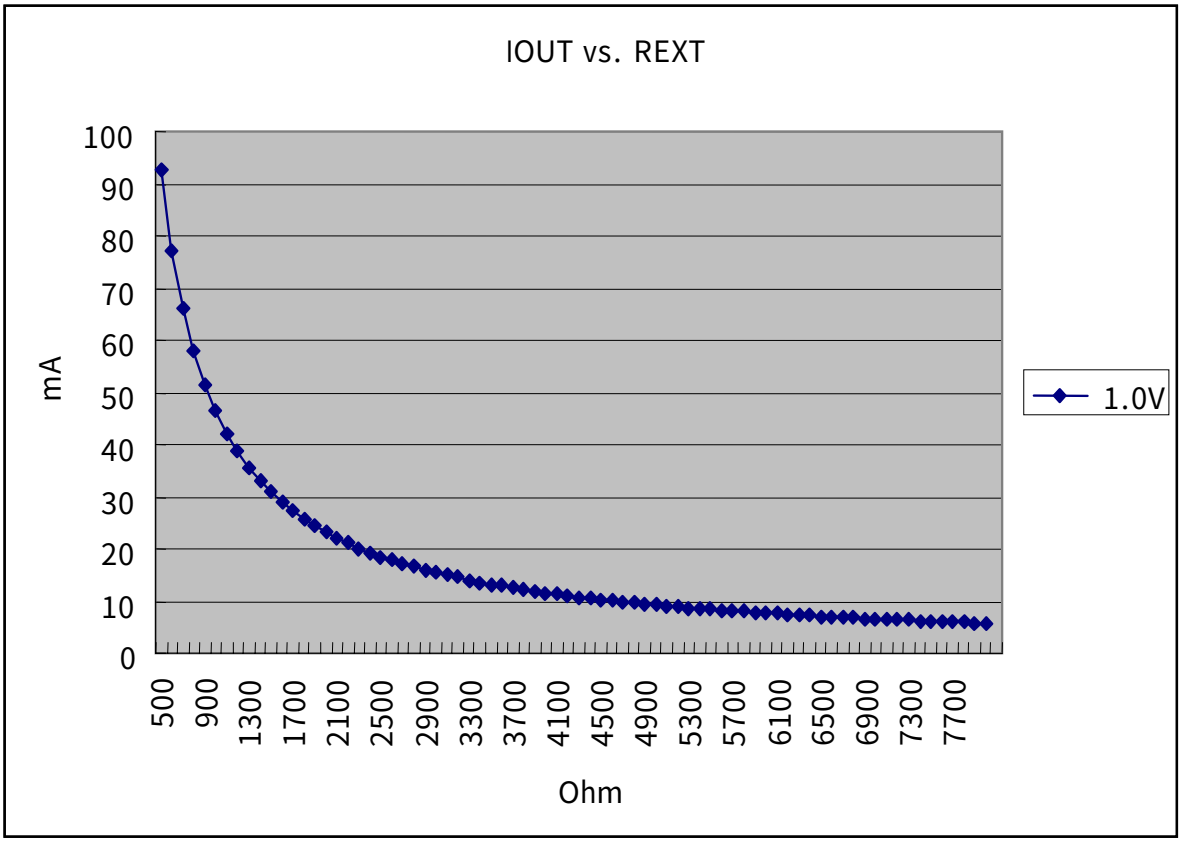


ADJUSTING OUTPUT CURRENT

The output current is determined by an external resistor. The relationship between I_{OUT} and R_{EXT} is as follows;

$$I_{OUT}[A] = \{1.16/(30+R_{EXT})\} * 50$$

OUTPUT CURRENT vs. REXT



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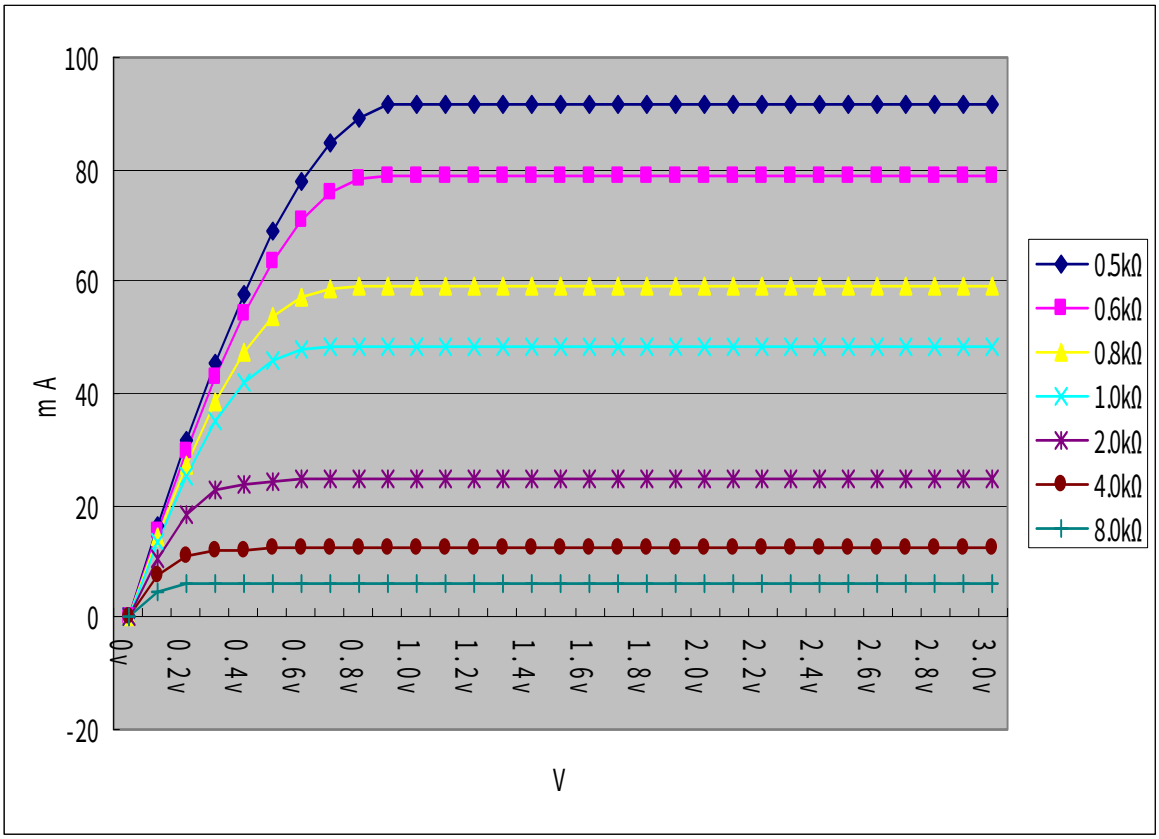
CONSTANT OUTPUT CURRENT

The LD1510 provides a constant current output characteristics for LED display application. ;



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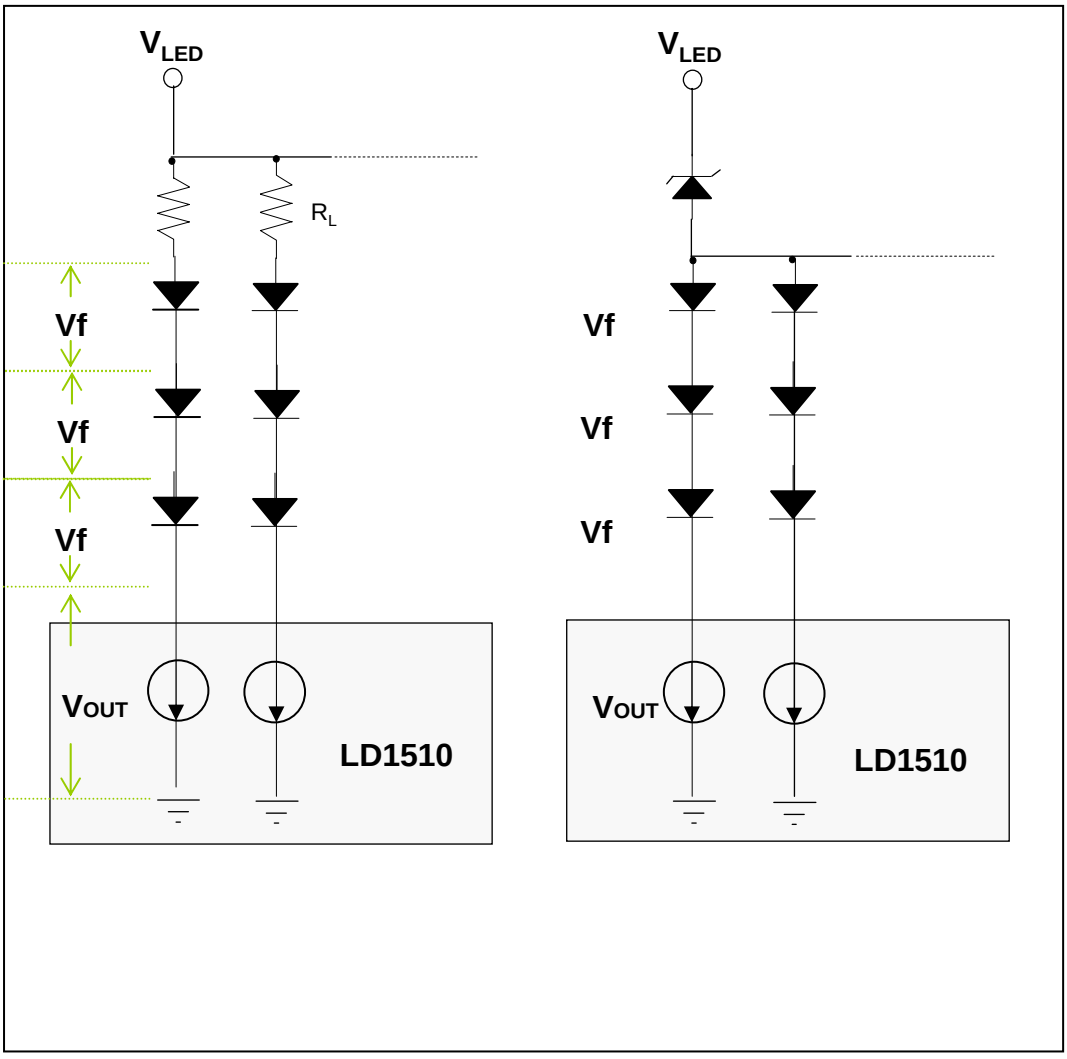
LED SUPPLY VOLTAGE(VLED)



It is very important to select the proper value of Load Resistor(RL). Because the optimal VOUT value guarantees the constant output current and long life time of LED driver IC without over power consumption.

For example, let's calculate the Load Resistor value at VLED=12V, Iout=50mA, LED Forward Voltage(Vf)=3V.

1) The full current of LD1510 = 50mA x 3 (channels) = 150mA
2) The power consumption is 150mA x VOUT voltage.
- when VOUT = 1V, the power consumption is 150mW.
- when VOUT= 2V, the power consumption is 300mW.

Therefore, the Load Resistor (RL) = (VLED – VOUT– Vf*3) / Iout
= (12V – VOUT – 9V) / 50mA
= 40Ω (When VOUT = 1V)

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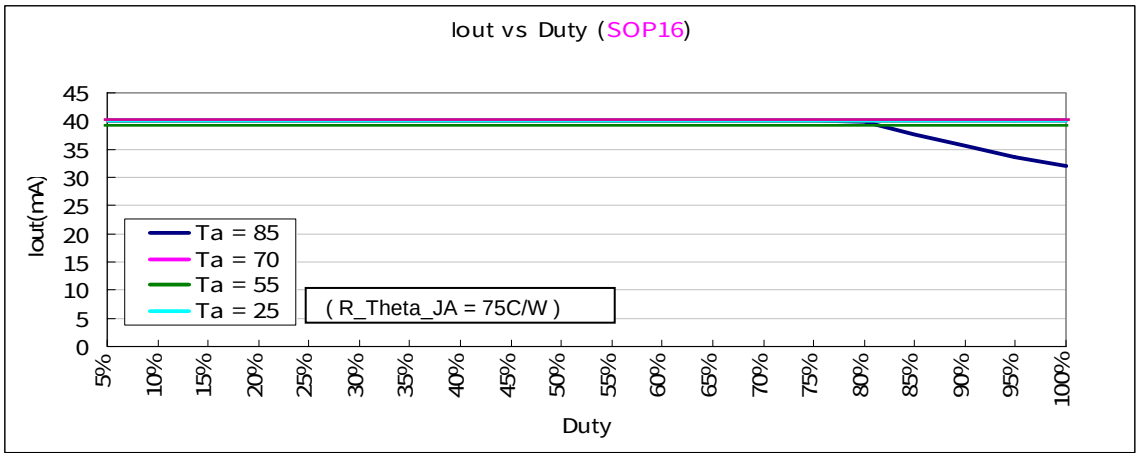
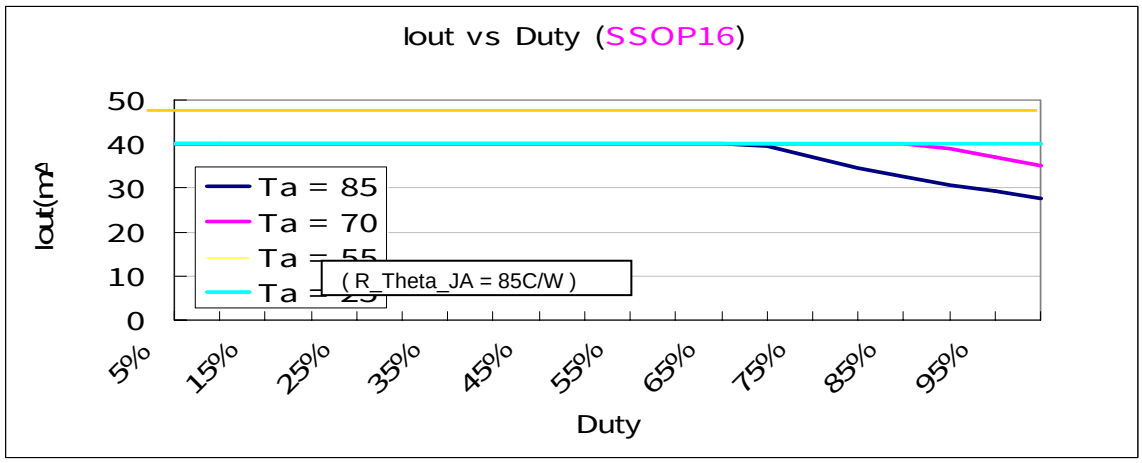
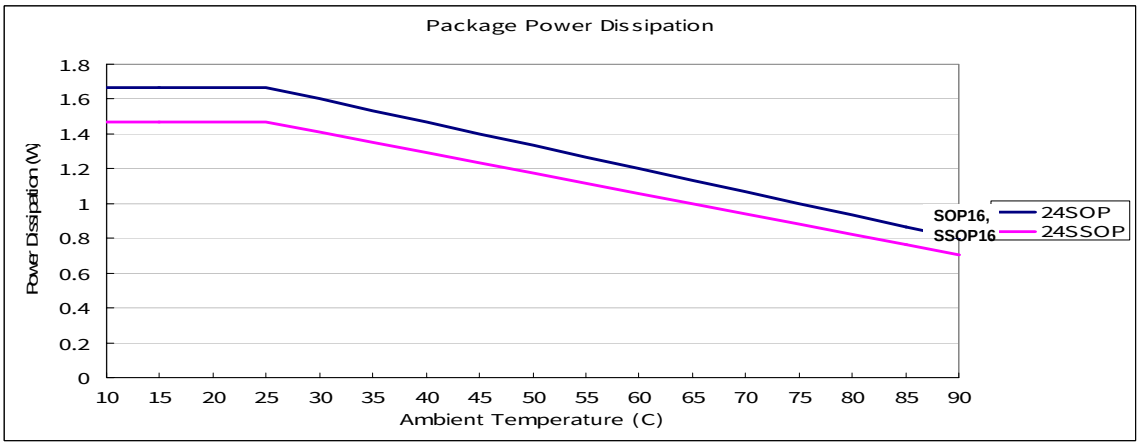
PACKAGE POWER DISSIPATION(PD)

The LD1510 provides many package options such as SOP16 package and SSOP16 package. The maximum allowable package power dissipation is determined as PD(max) = (Tj – Ta) / R_Theta_JA. When 3 output ports are turned on simultaneously, the actual power package dissipation is PD(act) = (IDD x VDD) + (IOUT x Duty x VOUT x 3). Therefore, to keep that PD(act) is less equal than PD(max). The maximum allowable output current as a function of duty cycle is:

IOUT = {[(Tj – Ta) / R_Theta_JA] – (IDD x VDD)} / VOUT / Duty / 3 where Tj = 150C







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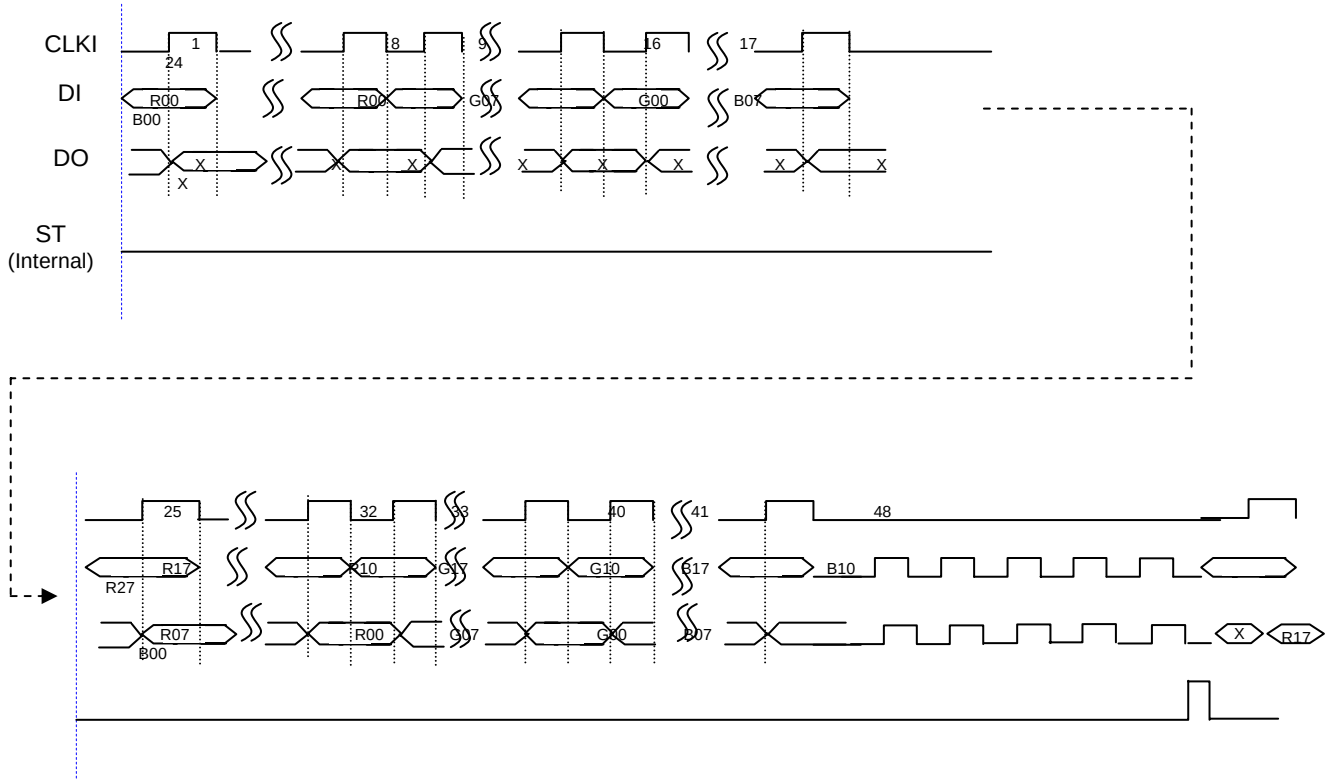
FUNCTIONAL DESCRIPTION

COMMUNICATION MODE TIMING DIAGRAM

8bit Mode (MOD = L)



When 2 chips are connected in series, strobe signal shall be applied after 48ea of clock input.

When more than 2 chips are connected in series, strobe signal shall be applied

after N x 24ea of clock input. ('N' is the number of chip.)

****Note) Apply the strobe signal after minimum 10us from the last clock (e.g. 48th clock in 2 chips)**

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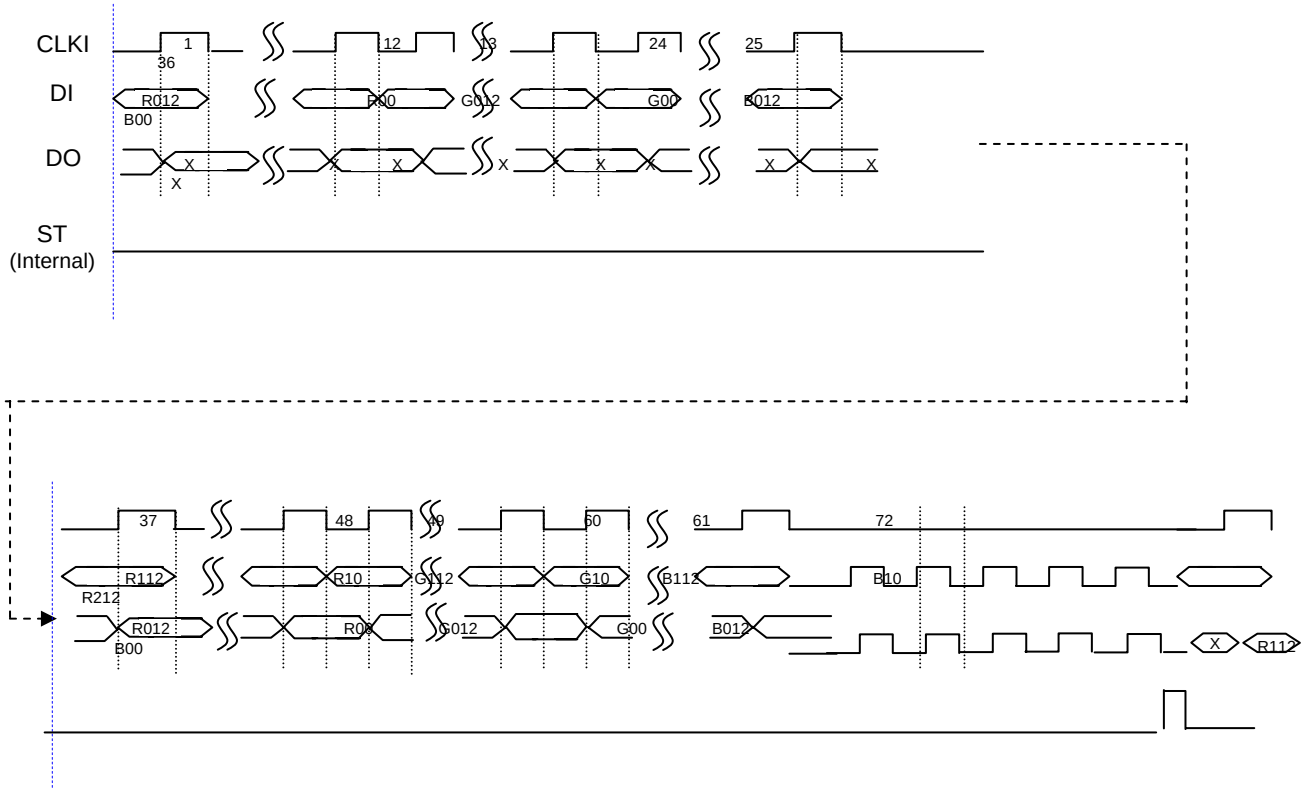
12bit Mode (MOD = H)



When 2 chips are connected in series, strobe signal shall be applied after 72ea of clock input.

When more than 2 chips are connected in series, strobe signal shall be applied

after N x 36ea of clock input. ('N' is the number of chip.)

****Note) Apply the strobe signal after minimum 10us from the last clock (e.g. 72th clock in 2 chips)**

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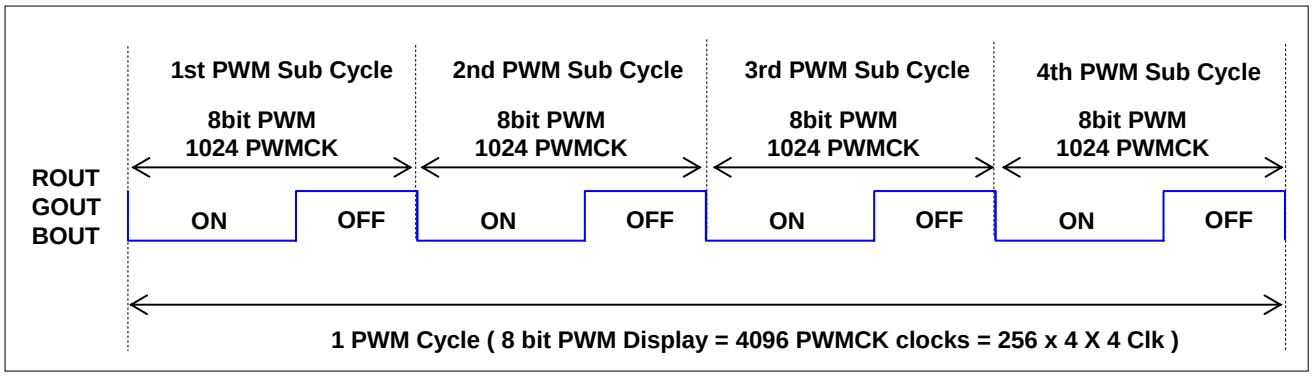
PWM DISPLAY CYCLE

The LD1510 implements the 8bit/12bit gray level of each output port using the 4 PWM sub cycles. Subcycle is consisted of 6 bit/10bit PWMCK clocks respectively. This enhancement provides a excellent energy distribution in lighting the LED and increases the visual refresh rate and reduces the flickers.

D[7:0] : Display Data(8 bit Gray Scale Data)



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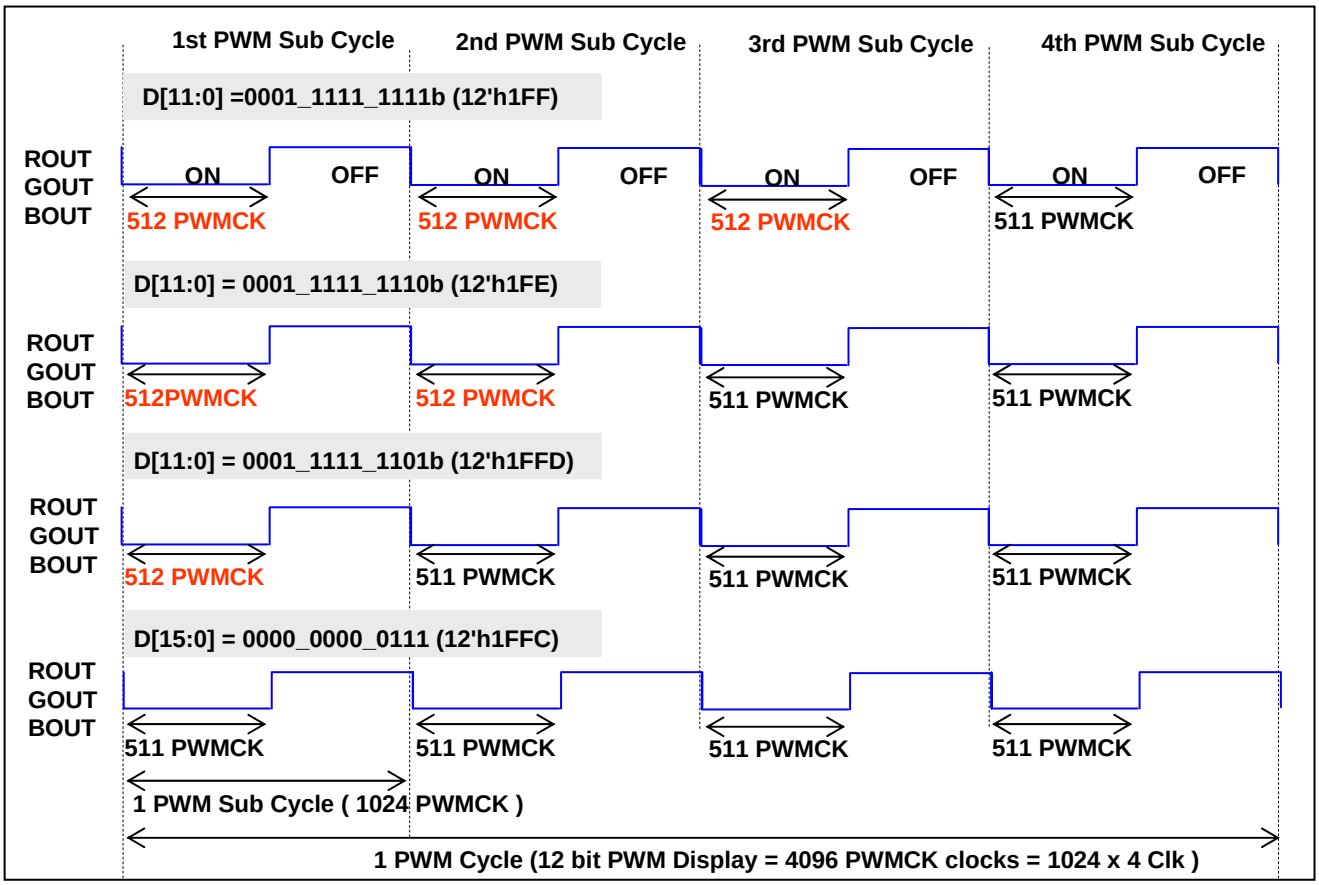
D[11:0] : **Display Data(12 bit Gray Scale Data)**

The following examples show the PWM timing diagram for different display data.

(Case 1)



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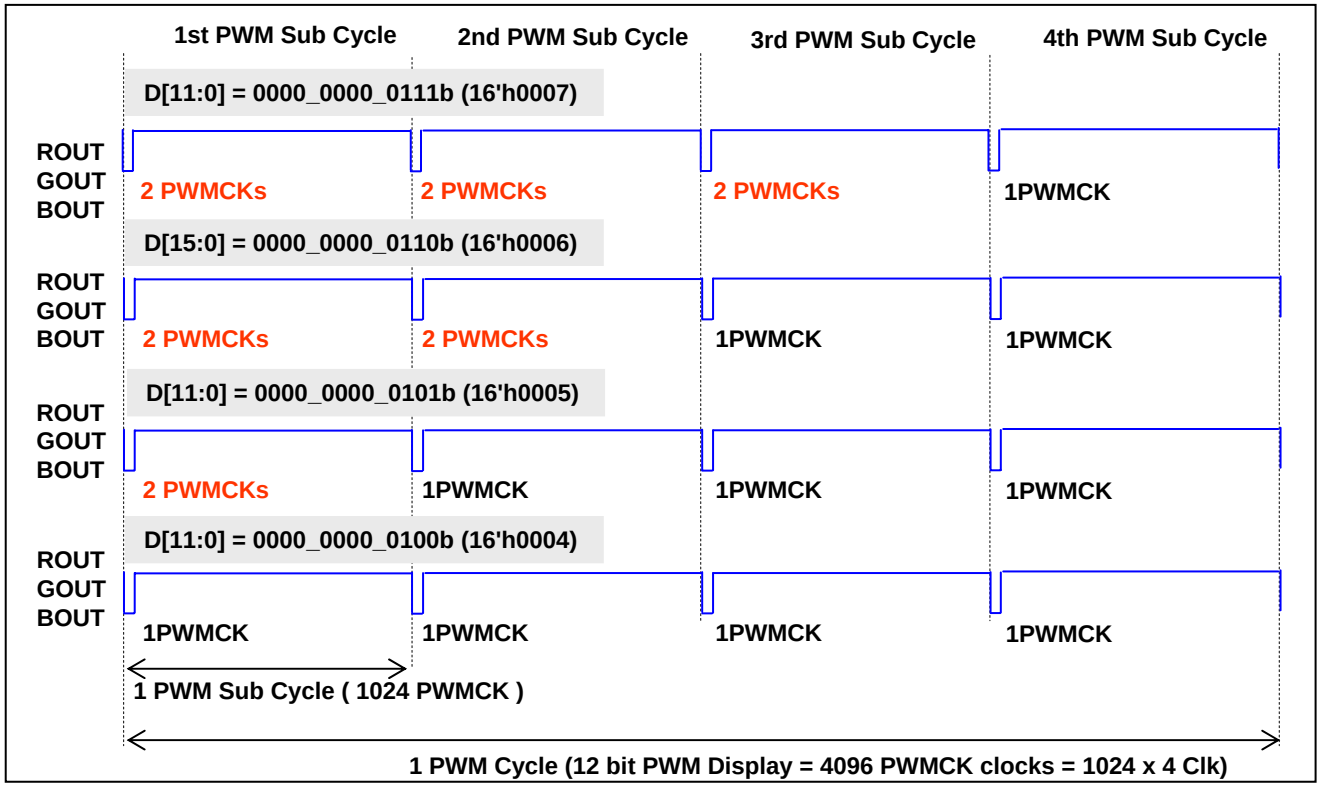
D[11:0] : Display Data(12 bit Gray Scale Data)

The following examples show the PWM timing diagram for different display data.

(Case 2)



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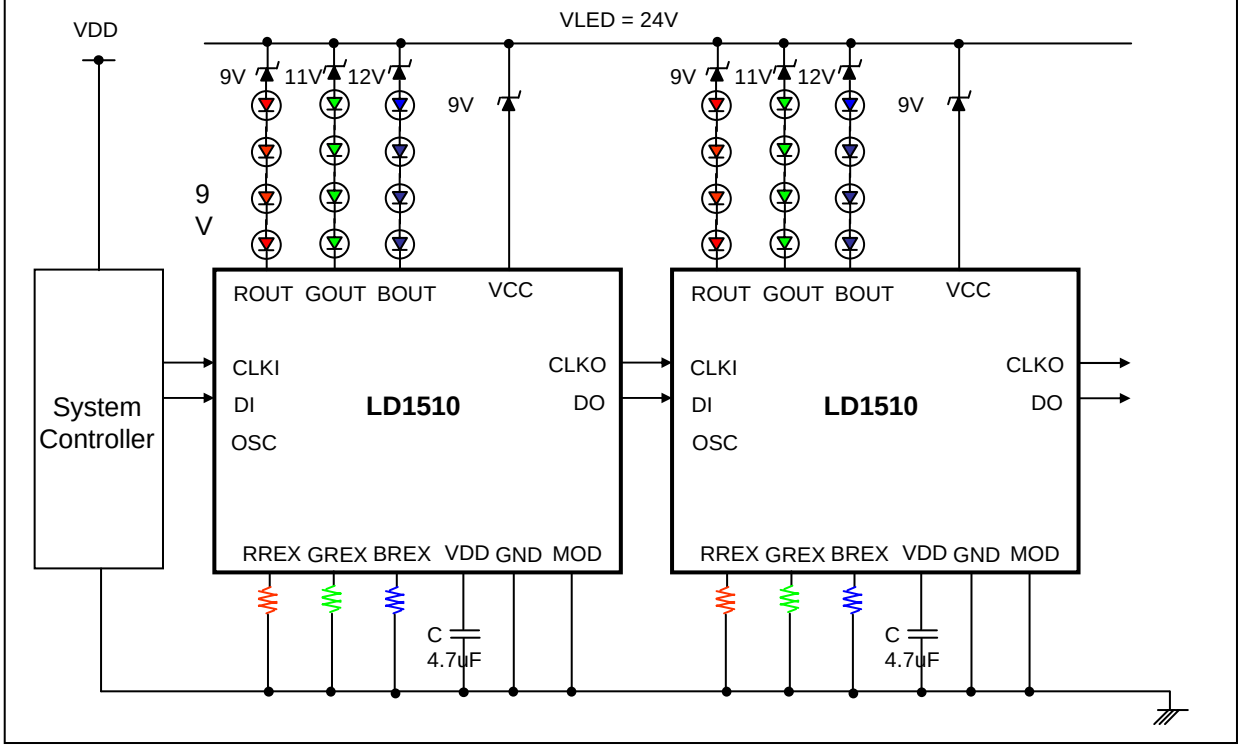
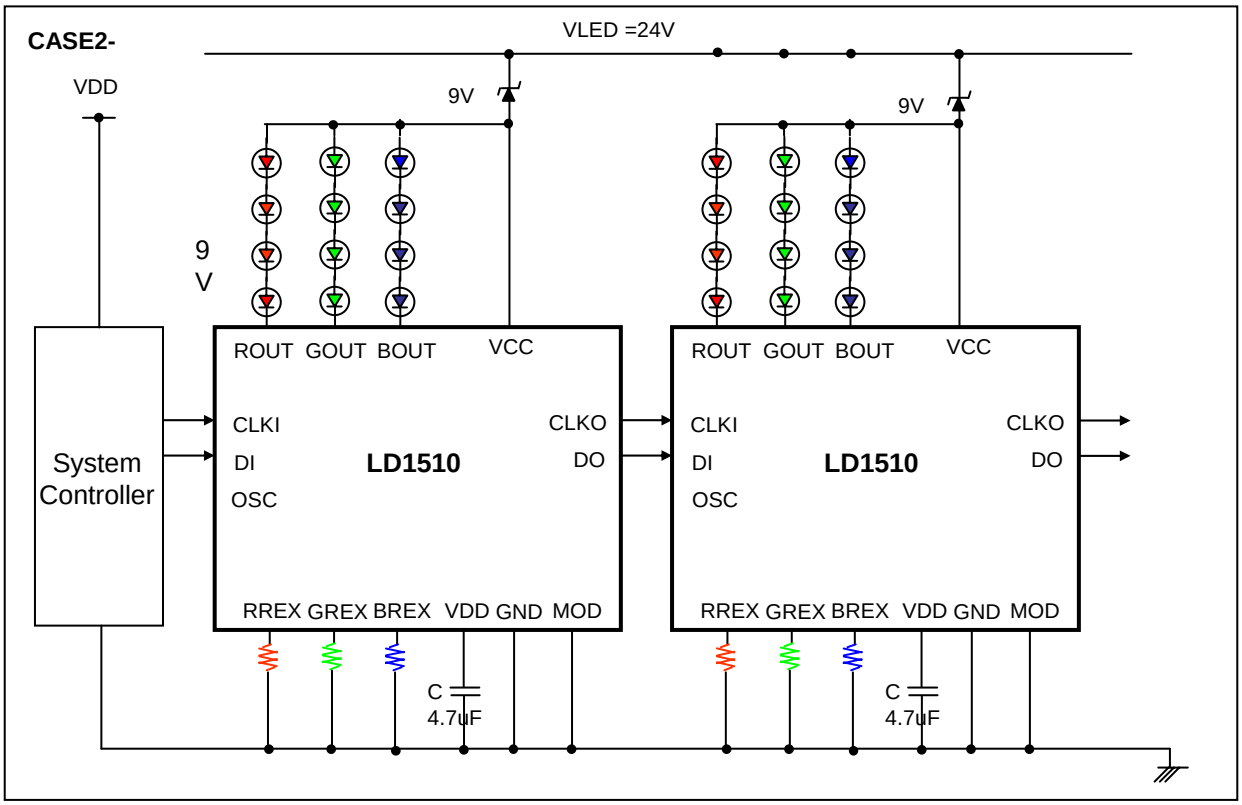
APPLICATION

CSSE1 - VLED = 24V (if RED VF=3.4V, GLED VF=2.8V, BLED VF=2.6V)



CASE2-



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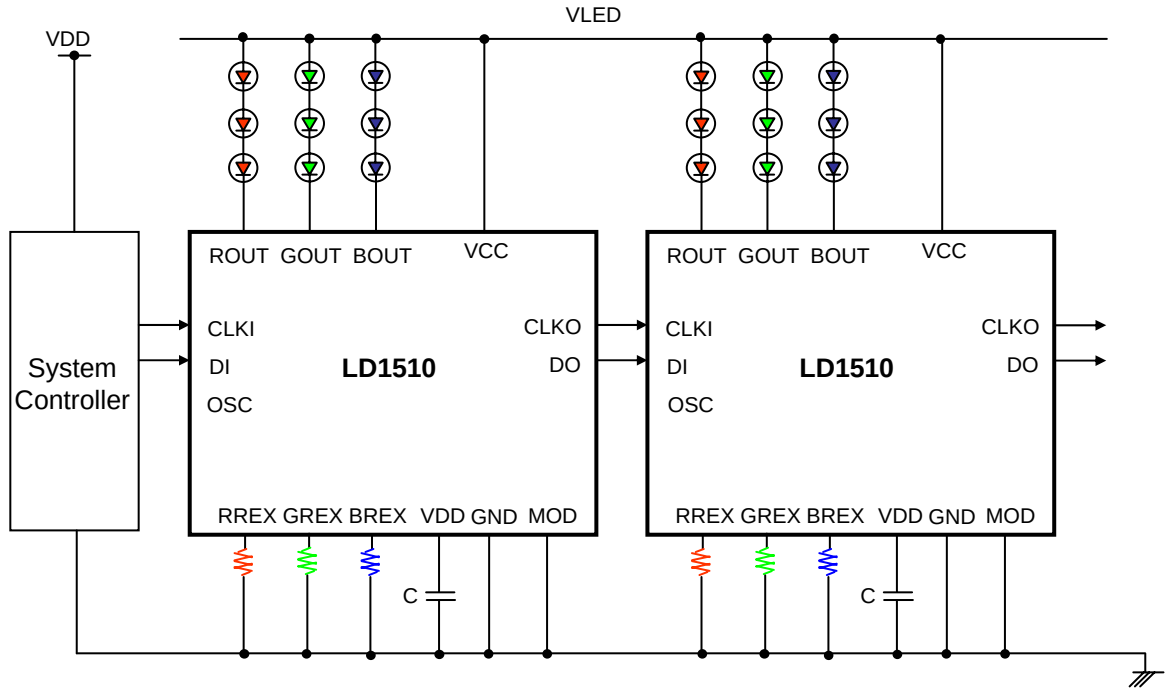
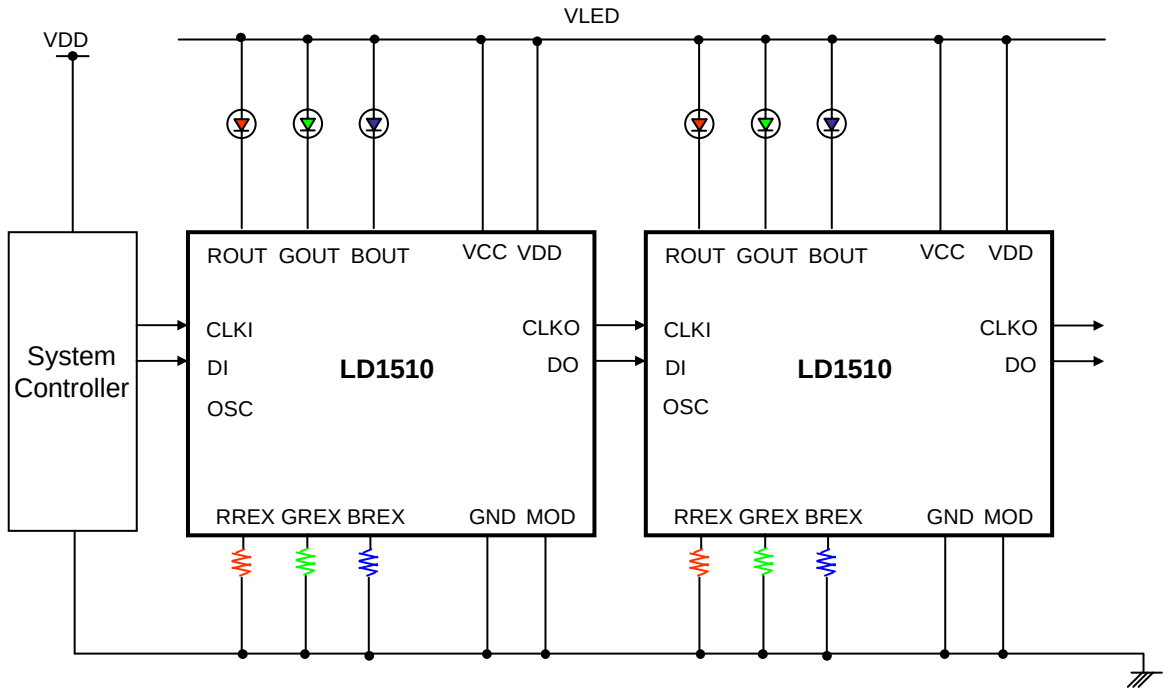
CASE3- 8bit Luminance Data and VLED = 7 ~ 18V



CASE4- 8bit Luminance Data and VLED = 4 ~ 6V



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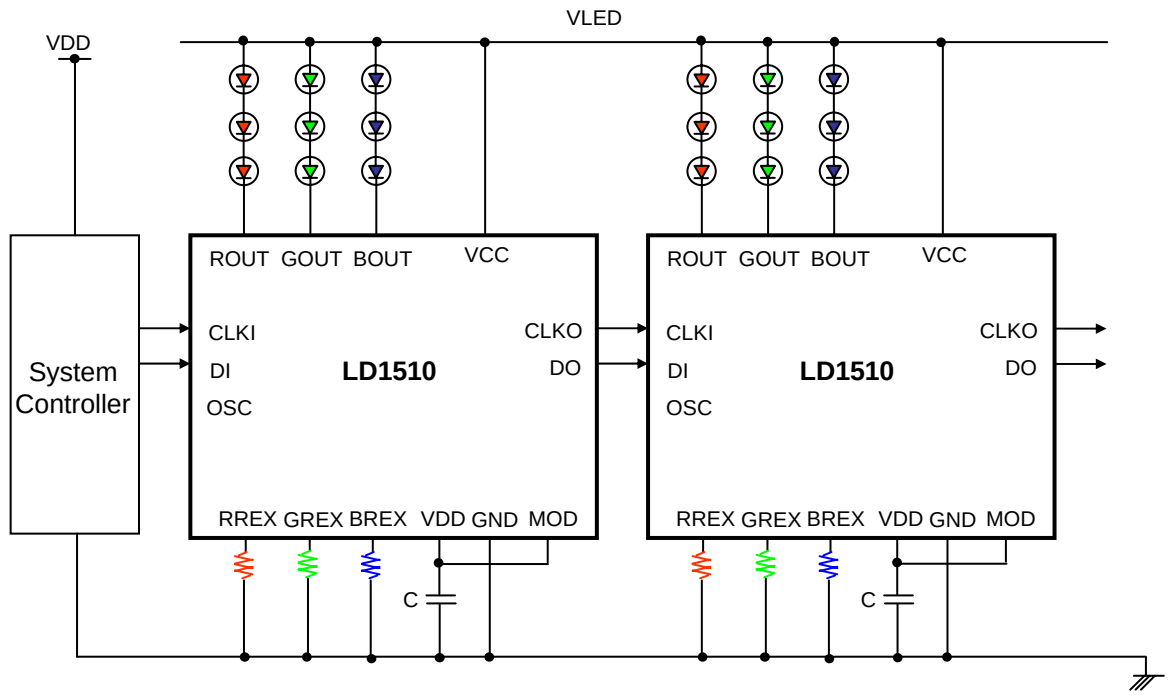
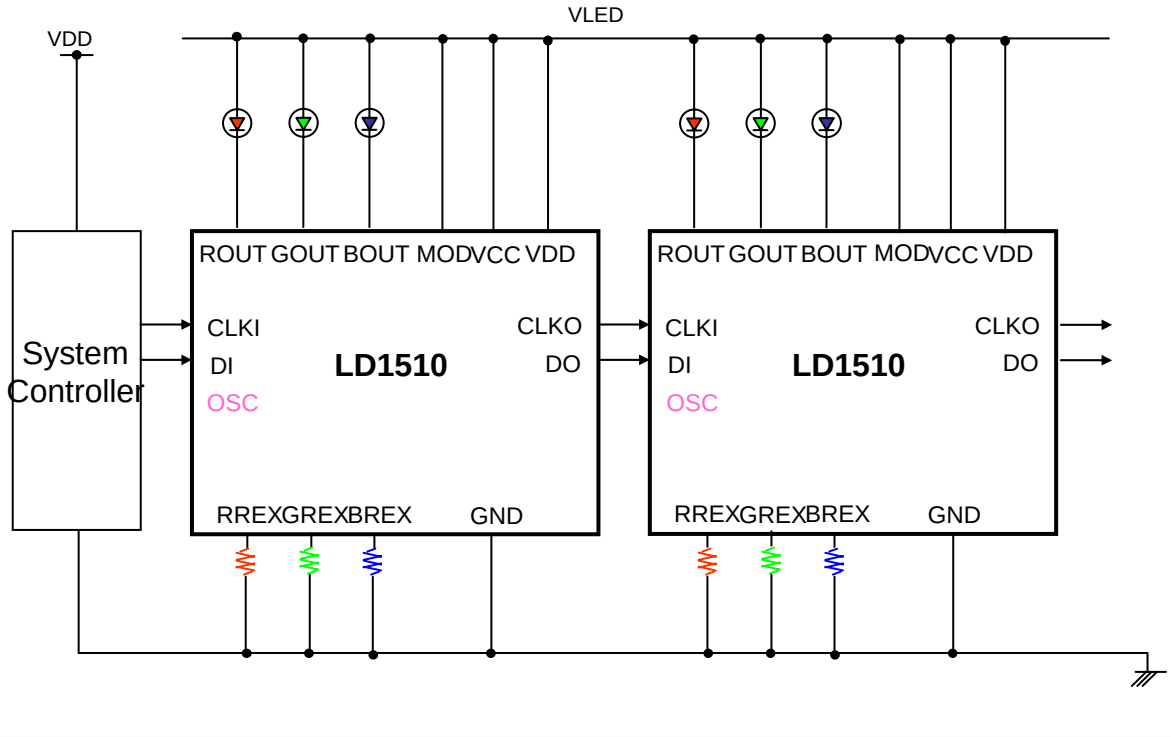
CASE5 - 12bit Luminance Data and VLED = 7 ~ 18V



CASE6 - 12bit Luminance Data and VLED = 4 ~ 6V



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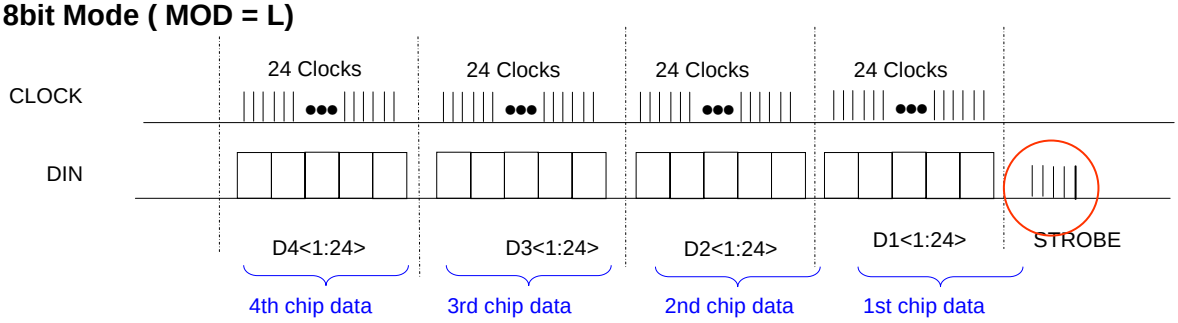
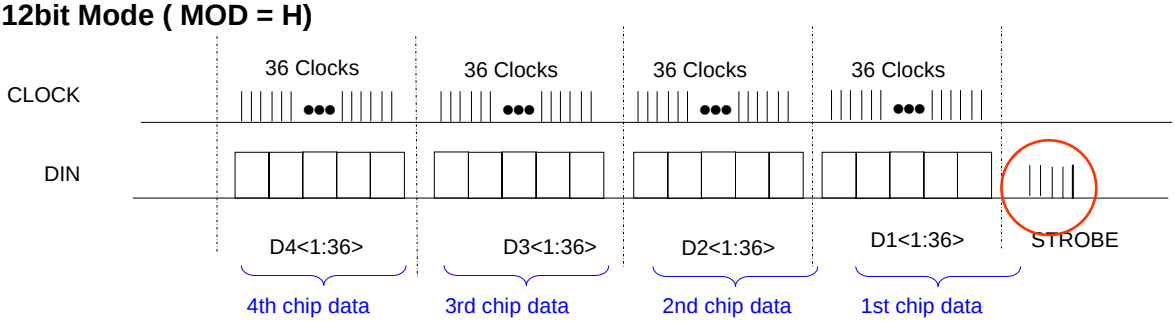
TIMING DIAGRAM FOR DATA TRANSMISION

For example - Using 4 CHIPS

8bit Mode (MOD = L)

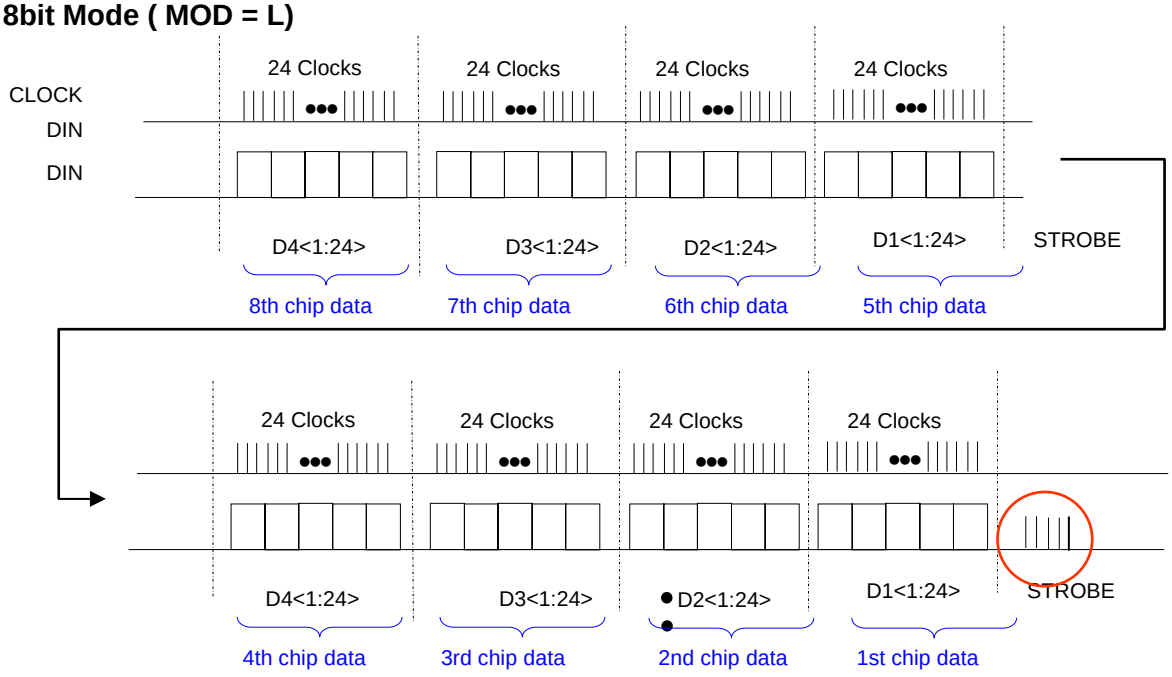


12bit Mode (MOD = H)



Case of 8 chips

8bit Mode (MOD = L)



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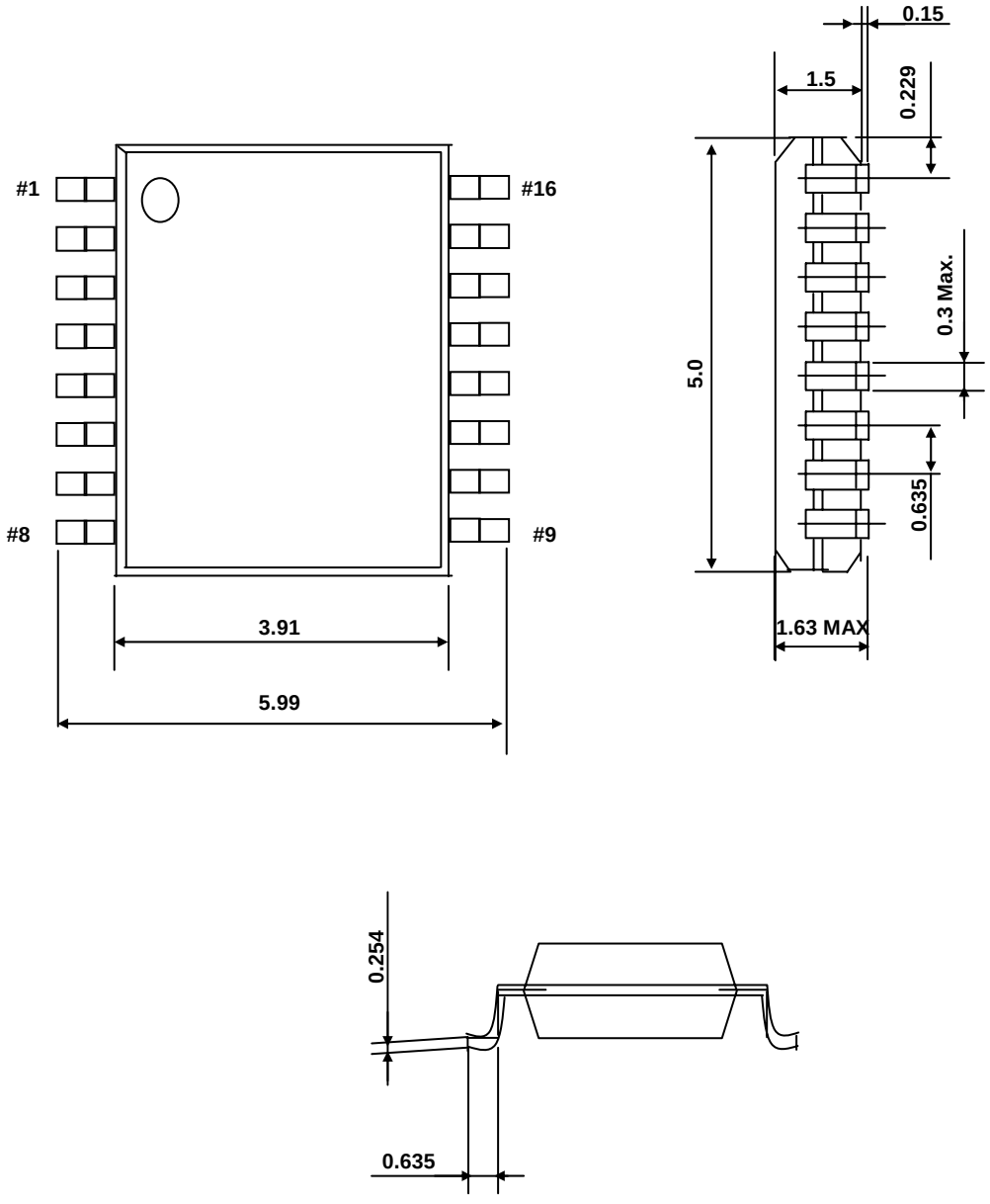
PACKAGE OUTLINE DIMENSION

SSOP1
6



Unit : mm

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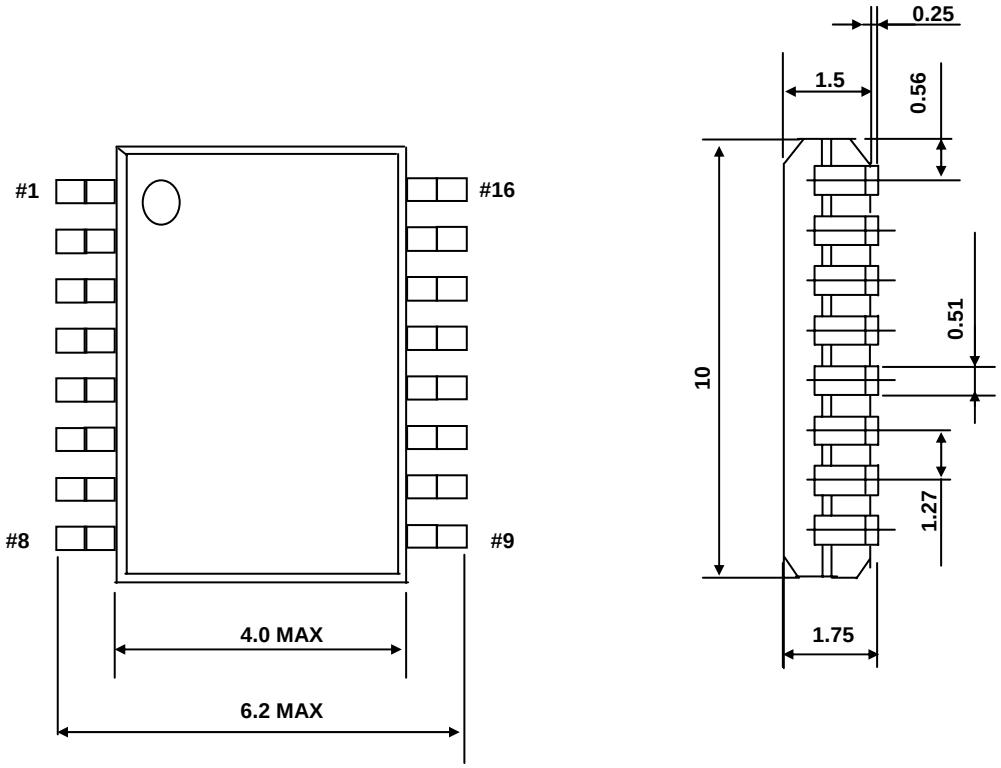
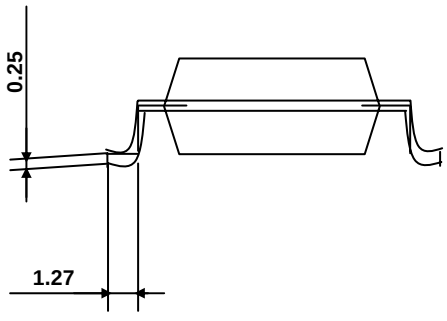
SOP16





Unit : mm

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