Ordering number : ENN*6724

CMOS IC

LC868116/12/08A

8-Bit Single Chip Microcontroller with 16/12/08K-Byte ROM and 640-Byte RAM On Chip

Preliminary

Overview

The LC868116A/12A/08A microcontrollers are 8-bit single chip microcontrollers with the following on-chip functional blocks :

- CPU : Operable at a minimum bus cycle time of 0.5μs (microseconds)
- On-chip ROM maximum capacity : 16K bytes
- On-chip RAM capacity : 640 bytes
- Dot-matrix liquid crystal display (LCD) automatic display controller / driver
- External memory
- 16-bit timer / counter (or two 8-bit timers)
- 16-bit timer / PWM (or two 8-bit timers)
- Two 8-bit synchronous serial-interface circuits
- 13-source 9-level vectored interrupt system

All of the above functions are fabricated on a single chip

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Features

(1) Read Only Memory (ROM) : LC868116A 16384 × 8 bits
: LC868112A 12288 × 8 bits
: LC868108A 8192 × 8 bits

(2) Random Access Memory (RAM) : 512 × 8 bits (calculation area)
128 × 8 bits (display area)

(3) Bus Cycle Time / Instruction Cycle Time

Bus cycle time	Instruction cycle time	System clock oscillation	Oscillation frequency	Voltage	Note	
0.5µs	1µs	Ceramic (CF)	12MHz	4.5-6.0V	OCR7=0	excluding external memory access function
			6MHz		OCR7=1	
1µs	2µs	Ceramic (CF)	6MHz	4.5-6.0V	OCR7=0	for external memory access
			3MHz		OCR7=1	
2µs	4µs	Ceramic (CF)	3MHz	2.5-6.0V	OCR7=0	
			1.5MHz		OCR7=1	
7.5µs	15µs	Internal RC	800kHz	2.5-6.0V	OCR7=0	
3.8µs	7.5µs				OCR7=1	
183µs	366µs	Crystal (XTAL)	32.768kHz	2.5-6.0V	OCR7=0	
91.5µs	183µs				OCR7=1	

* Bus cycle time means ROM-read period.
OCR7 : Bit-7 of the oscillation control register.

(4) Ports
- Input / output ports : 6 ports (47 terminals)
  - Input/output port programmable in a nibble : 1 port (8 terminals)
  - Input/output port programmable every function unit : 1 port (7 terminals)
  - Input/output port programmable in a bit : 4 ports (32 terminals)
- Input port : 1 port (4 terminals)
- Ports at external memory mode
  1. External Latch
     Port 0 : Address output of lower 8-bit, input/output of data
     Port 2 : Address output of upper 8-bit
     Port 5 : Bank address output
  2. No External Latch
     Port 0 : Input/output of data
     Port 3 : Address output of lower 8-bit
     Port 2 : Address output of upper 8-bit
     Port 5 : Bank address output

  (Set whether the external latch is used or not by program.)
- LCD segment driver output ports : 48 terminals
  (Function change available : segment/common)
- LCD common driver output ports : 16 terminals
  (1/32 duty maximum : at using segment output ports as common output by mask option)

(5) External memory access
- External program memory access function
  External program memory capacity : 64K bytes
  Programable switch internal program/external program
  (At initial : Internal program)
  Enable/disable control of external program → internal program memory switch

- Ports
  Port 2 : Address output of upper 8-bit
  Uses $\overline{\text{EROE}}$ terminal ($\overline{\text{OE}}$ signal of the external ROM)
  1. Using the external latch
     Port 0 : Address output of lower 8-bit, data input port
     Uses the ADLC terminal (latch clock of the lower 8-bit address signal)
  2. Not use the external latch
     Port 0 : Input port of data
     Port 3 : Address output of lower 8-bit
- External data memory access function
  Using the LDC instruction
  External memory capacity : 16M bytes
  1. Internal program memory
     Switch the reference of internal ROM data/external ROM data by program.
  2. External program memory
     Reference external ROM data only.
  Ports
  Port 2 : Address output of upper 8-bit
  Port 5 : Bank address output
  Uses $\overline{\text{EROE}}$ terminal ($\overline{\text{OE}}$ signal of the external ROM)
  1. Using external latch
     Port 0 : Address output of lower 8-bit, input port of data
     Uses the ADLC terminal (latch clock of the lower 8-bit address signal)
  2. Not use external latch
     Port 0 : Input port of data
     Port 3 : Address output of lower 8-bit
- External RAM memory access function
  Using the LDX, STX instruction
  External memory capacity : 16M bytes
  Ports
  Port 2 : Address output of upper 8-bit
  Port 5 : Bank address output
  Uses the P46 terminal ($\overline{\text{OE}}$ signal of external RAM) : the LDX instruction execution
  Uses the P47 terminal ($\overline{\text{WE}}$ signal of external RAM) : the STX instruction execution
  1. Using the external latch circuit
     Port 0 : Address output of lower 8-bit, input/output port of data
     Uses the ADLC terminal (latch clock of the lower 8-bit address signal)
  2. Not use the external latch circuit
     Port 0 : Input/output port of data
     Port 3 : Address output of lower 8-bit

(6) LCD automatic display controller
- Display duty : 1/4 - 1/32 duty
  * Up to 1/32 display duty can be specified by program. VDD allows up to 6V. Select the preferable LCD panel within this range.
- Display bias : 1/4, 1/5, 1/7 bias
- Programmable character display / graphic display
- Character display
  1. On-chip character generator ROM
     ROM capacity : 8960 bits
     Character font : 5 × 7 dots
     Number of Characters : 256

2. LCD instruction
   - Display : ON/OFF
   - Cursor : ON/OFF/BLINK
   - Character blink : ON/OFF
   - Character scroll : Control by specified starting address

- Graphic display
  - LC868100 series : 1024 dots Maximum
  - External segment driver : Enable to extend of LCD drive
- LCD contrast
  - LCD display contrast programmable
- LCD display power supply
  - Doubler circuit available within VDD≤3V.
  - * Doubler generates up to 6V.
- LCD driver
  - Following two kinds of combination can be selected by mask option

No.	Segment output port	Common output port
1	48	16
2	32	32

  - * Up to 32 commons can be specified by mask option. As maximum LCD display voltage is 6V, please select the preferable LCD panel and the display condition with this range.
  - * In general, the LCD driver cannot be expanded.

(7) Serial-interface
- Two 8-bit serial-interface circuits
  LSB first / MSB first function available
- Internal 8-bit baud-rate generator in common with two serial-interface circuits

(8) Timers
- Timer0 (T0L, T0H)
  16-bit timer / counter
  2-bit prescaler + 8-bit programmable prescaler
  - Mode 0 : Two 8-bit timers with programmable prescaler
  - Mode 1 : 8-bit timer with a programmable prescaler + 8-bit counter
  - Mode 2 : 16-bit timer with a programmable prescaler
  - Mode 3 : 16-bit counter
- Timer1 (T1L, T1H)
  16-bit timer / PWM
  - Mode 0 : Two 8-bit timers
  - Mode 1 : 8-bit timer + 8-bit PWM
  - Mode 2 : 16-bit timer
  - Mode 3 : Variable-bit PWM (9-16 bits)
- Base timer
  Every 500ms overflow system for a clock application (using 32.768kHz crystal oscillation for Base timer clock)
  The Base timer clock selectable ; 32.768kHz crystal oscillation, System clock, and programmable prescaler output of Timer 0

(9) Buzzer output
- The Buzzer sound frequency selectable ; 4KHz, 2KHz

(10) Remote control receiver circuit (using P73/INT3/T0IN terminal)
- Noise rejection available
- The interrupt polarity selectable

(11) Watchdog timer
- The watchdog timer is taken on RC outside. (using P70/INT0 terminal)
- Watchdog timer operation selectable : interrupt system, system reset

(12) Interrupts system
- 13-source 9-level vectored interrupts :
  1. External interrupt INT0 (includes watchdog timer)
  2. External interrupt INT1
  3. External interrupt INT2, timer / counter T0L (timer 0 lower 8 bits)
  4. External interrupt INT3, base timer
  5. Timer / counter T0H (timer 0 upper 8-bit)
  6. Timer T1L (timer 1 lower 8-bit), Timer T1H (timer 1 upper 8-bit)
  7. Serial interface SIO0
  8. Serial interface SIO1
  9. Port 0 or Port 3
- Interrupt priority control available

  Microcomputer allows 3 levels of interrupt; low level, high level and highest level of multiplex interrupt. It can specify a low level or a high level interrupt priority from INT2/T0L through port 0 or port 3 (the above interrupt number from three through nine). It can also specify a low level or the highest level interrupt priority to INT0 and INT1.

(13) Sub-routine stack levels
- 128 levels (Max.) : stack area included in RAM area

(14) Multiplication and division
- 16 bits × 8-bit (7 instruction cycle times)
- 16 bits / 8-bit (7 instruction cycle times)

(15) Three oscillation circuits
- On-chip RC oscillation circuit using for the system clock, for the LCD display and for the step-up circuit.
- On-chip CF oscillation circuit using for the system clock, for the LCD display and for the step-up circuit.
- On-chip crystal oscillation circuit using for the system clock, for time-base clock and for the LCD display.

(16) Standby function
- HALT mode function

  The HALT mode is used to reduce the power dissipation. In this operation mode, the program execution is stopped. This operation mode can be released by the interrupt request signals or setting to low level for the reset terminal ($\overline{\text{RES}}$).
- HOLD mode function

  The HOLD mode is used to freeze all the oscillations ;
  RC (internal), CF and Crystal oscillations. This mode can be released by the following operations:
  - Reset terminal ($\overline{\text{RES}}$) set to low level.
  - Set to assigned level to INT0/1 terminals.
  - Set to assigned level to Port 0/3.

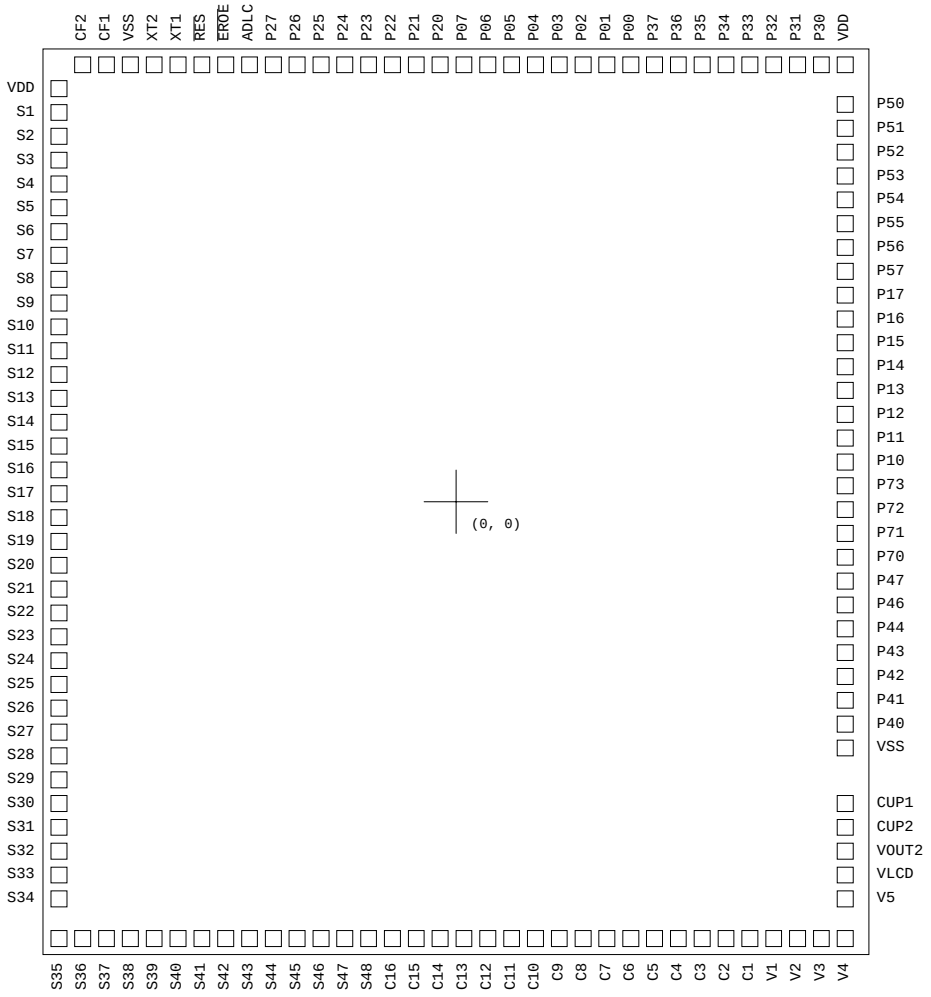
(17) Factory shipment
- Chip

  QIC160 package shipping available for sample evaluation.

(18) Development support tools
- Evaluation (EVA) chip : LC868099
- Emulator : EVA86000 + ECB868000 (Evaluation chip board)

Pin Assignment

Chip size : 4.98mm × 6.26mm
Pad size : 106μm × 106μm
Bonding area size : 90μm × 90μm
Chip thickness : 480μm±20μm

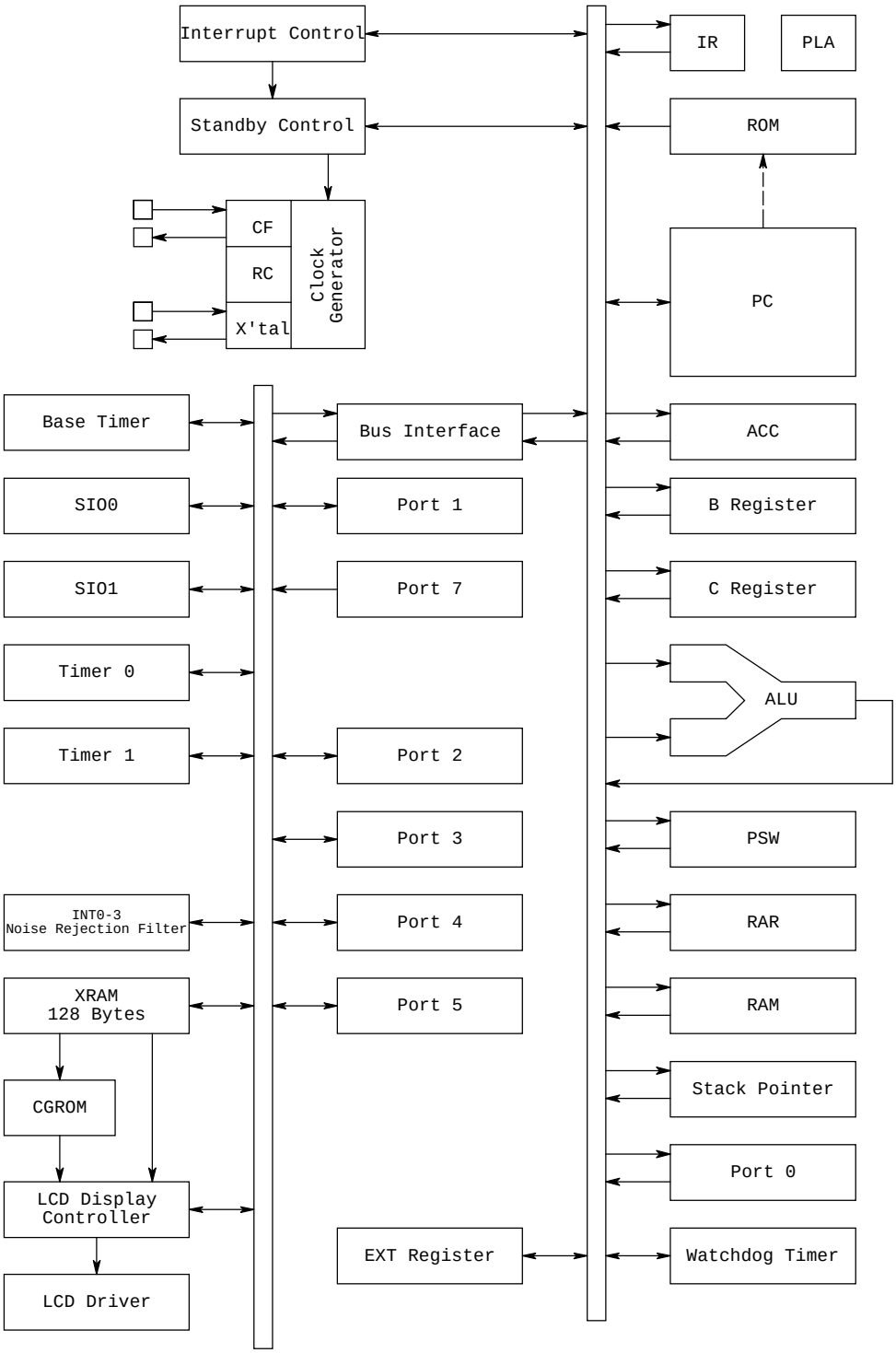


Pad Name and coordinates table

Pad No.	Name	Coordinates	
		Xμm	Yμm
1	VDD	-2240	2236
2	S1	-2240	2100
3	S2	-2240	1965
4	S3	-2240	1829
5	S4	-2240	1694
6	S5	-2240	1558
7	S6	-2240	1422
8	S7	-2240	1287
9	S8	-2240	1151
10	S9	-2240	1016
11	S10	-2240	880
12	S11	-2240	744
13	S12	-2240	609
14	S13	-2240	473
15	S14	-2240	338
16	S15	-2240	202
17	S16	-2240	66
18	S17	-2240	-69
19	S18	-2240	-205
20	S19	-2240	-340
21	S20	-2240	-476
22	S21	-2240	-612
23	S22	-2240	-747
24	S23	-2240	-883
25	S24	-2240	-1018
26	S25	-2240	-1154
27	S26	-2240	-1290
28	S27	-2240	-1425
29	S28	-2240	-1561
30	S29	-2240	-1696
31	S30	-2240	-1832
32	S31	-2240	-1968
33	S32	-2240	-2103
34	S33	-2240	-2239
35	S34	-2240	-2374
36	S35	-2192	-2875
37	S36	-2056	-2875
38	S37	-1921	-2875
39	S38	-1785	-2875
40	S39	-1649	-2875
41	S40	-1514	-2875
42	S41	-1378	-2875
43	S42	-1243	-2875
44	S43	-1107	-2875
45	S44	-971	-2875
46	S45	-836	-2875
47	S46	-700	-2875
48	S47	-565	-2875
49	S48	-429	-2875
50	C16	-293	-2875
51	C15	-158	-2875
52	C14	-22	-2875
53	C13	113	-2875
54	C12	249	-2875
55	C11	385	-2875
56	C10	520	-2875
57	C9	656	-2875
58	C8	791	-2875
59	C7	927	-2875
60	C6	1063	-2875
61	C5	1198	-2875
62	C4	1334	-2875
63	C3	1469	-2875
64	C2	1605	-2875
65	C1	1741	-2875
66	V1	1876	-2875
67	V2	2012	-2875
68	V3	2147	-2875
69	V4	2283	-2875
70	V5	2240	-2479
71	VLCD	2240	-2344
72	VOUT2	2240	-2208
73	CUP2	2240	-2072
74	CUP1	2240	-1937
75	VSS	2240	-1481
76	P40	2240	-1345
77	P41	2240	-1210
78	P42	2240	-1074
79	P43	2240	-938
80	P44	2240	-803
81	P46	2240	-667
82	P47	2240	-532
83	P70	2240	-396
84	P71	2240	-260
85	P72	2240	-125
86	P73	2240	11
87	P10	2240	146
88	P11	2240	282
89	P12	2240	418
90	P13	2240	553
91	P14	2240	689
92	P15	2240	824
93	P16	2240	960
94	P17	2240	1096
95	P57	2240	1231
96	P56	2240	1367
97	P55	2240	1502
98	P54	2240	1638
99	P53	2240	1774
100	P52	2240	1909
101	P51	2240	2045
102	P50	2240	2180
103	VDD	2123	2875
104	P30	1987	2875
105	P31	1852	2875
106	P32	1716	2875
107	P33	1581	2875
108	P34	1445	2875
109	P35	1309	2875
110	P36	1174	2875
111	P37	1038	2875
112	P00	903	2875
113	P01	767	2875
114	P02	631	2875
115	P03	496	2875
116	P04	360	2875
117	P05	225	2875
118	P06	89	2875
119	P07	-47	2875
120	P20	-182	2875
121	P21	-318	2875
122	P22	-453	2875
123	P23	-589	2875
124	P24	-725	2875
125	P25	-860	2875
126	P26	-996	2875
127	P27	-1131	2875
128	ADLC	-1267	2875
129	$\overline{\text{ER0E}}$	-1403	2875
130	$\overline{\text{RES}}$	-1538	2875
131	XT1	-1674	2875
132	XT2	-1809	2875
133	VSS	-1945	2875
134	CF1	-2081	2875
135	CF2	-2216	2875

The values (X, Y) indicate the coordinates of each pad center with the center of the chip as the origin.
Connect the substrate of chip to VSS or open.

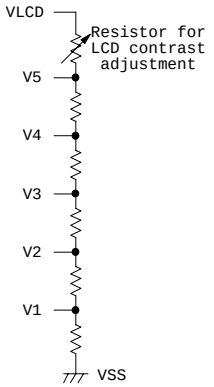
System Block Diagram



Pin Description

Name	No.	I/O	Function description	Option
VSS	75,133	-	Power terminal (-)	-
VDD	1,103	-	Power terminal (+)	-
VLCD	71	-	Power terminal (+) for LCD driver *2	-
V1 to V5	66-70	-	Voltage supply terminals to LCD drivers *2	-
VOUT2	72	-	Output terminals for doubler VOUT2 ≅ 2X(VDD-VSS)	-
CUP1,2	74,73	-	Capacitor connecting terminals for doubler, tripler	-
Port0 P00 to P07	112-119	I/O	•8-bit input/output port •Input/output can be specified in 4-bit •External memory mode 1. EXT resistor bit 2=0 Address output of lower 8-bit, input/output of data 2. EXT resistor bit 2=1 •Input/output of data •Input for key interrupt (P30INT=0) *1	•Pull-up resistor : Provided/Not provided •Output form : CMOS/N-ch open drain
Port1 P10 to P17	87-94	I/O	•8-bit input/output port •Input/output can be specified in a bit •Another functions P10 SIO0 data output P11 SIO0 data input, bus input/output P12 SIO0 clock input/output P13 SIO1 data output P14 SIO1 data input, bus input/output P15 SIO1 clock input/output P16 Buzzer output P17 Timer 1 output (PWM output)	•Output form : CMOS/N-ch open drain
Port2 P20 to P27	120-127	I/O	•8-bit input/output port •Input/output can be specified in a bit •External memory mode Address output of upper 8-bit	•Output form : CMOS/N-ch open drain
Port3 P30 to P37	104-111	I/O	•8-bit input/output port •Input/output in a bit •External memory mode 1. EXT resistor bit 2=0 : input/output port 2. EXT resistor bit 2=1 : address output of lower 8-bit for external memory •Input for key interrupt (P30INT=L) *1	•Pull-up resistor : Provided/Not provided •Output form : CMOS/N-ch open drain

*1 P30INT : Bit 0 of Port 3 interrupt control register.
*2 The structure of the LCD power supply is shown below.



Note : If the microcontroller is operated at 3V, the voltage doubler output (VOUT2) should be connected to the LCD power terminal (VLCD).
(or the output of an external voltage doubler should be connected to VLCD)

<table>
<tr><th>Name</th><th>No.</th><th>I/O</th><th>Function description</th><th>Option</th></tr>
<tr><td>Port4
P40 to P44
P46, P47</td><td>
76-80
81,82</td><td>I/O</td><td>•7-bit input/output port
•Input/output can be specified each upper 2 bits and lower 5 bits
•Another functions
P40 CL1 Latch clock
P41 CL2 Shift clock
P42 DO Output data
P43 M Alternate signal
P44 FRM Frame signal
P46 $\overline{RD}$ Read signal
P47 $\overline{WR}$ Write signal
(P40-P44 : LCD display extend signal, P46, P47 : External RAM access signal)</td><td>•Pull-up resistor : Provided/Not provided
•Output form : CMOS/N-ch open drain</td></tr>
<tr><td>Port5
P50 to P57</td><td>
102-95</td><td>I/O</td><td>•8-bit input/output port
•Input/output in bit unit
•External memory mode
1. EXT resistor bit 3=0 : input/output
2. EXT resistor bit 3=1 : bank address output for external memory</td><td>•Pull-up resistor : Provided/Not provided
•Output form : CMOS/N-ch open drain</td></tr>
<tr><td>Port7

P70 to P73</td><td>

83-86</td><td>I</td><td>•4-bit input port
•Another functions
P70 INT0 input/HOLD release/N-ch Tr. output for watchdog timer
P71 INT1 input/HOLD release
P72 INT2 input/timer 0 event input
P73 INT3 input with noise filter/timer 0 event input
•Interrupt received form, vector address
<table>
<tr><th></th><th>leading</th><th>trailing</th><th>leading & trailing</th><th>high level</th><th>low level</th><th>vector</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr>
</table></td><td>•Pull-up resistor : Provided/Not provided</td></tr>
</table>

Name	No.	I/O	Function description	Option
C1 to C16	65-50	O	LCD output terminals for common	-
S1 to S48	2-49	O	LCD output terminals for segment	LCD output terminals : segment/common
$\overline{RES}$	130	I	Reset	-
ADLC	128	O	Address control signal for external memory	-
$\overline{EROE}$	129	O	Enable signal of external ROM output	-
XT1	131	I	Input for 32.768kHz crystal oscillation In case of non use, connect to VDD	-
XT2	132	O	Output for 32.768kHz crystal oscillation In case of non use, should be left unconnected	-
CF1	134	I	Input for ceramic resonator oscillation In case of non use, connect to VDD	-
CF2	135	O	Output for ceramic resonator oscillation In case of non use, should be left unconnected	-

* Port options can be specified in a bit.

* A state of port at initial

Pin name	Input/output mode	A state of pull-up resistor specified at pull-up option
Port 0, 7	Input	Fixed pull-up resistor exist
Ports 1, 2 Ports 3, 5	Input	Programmable pull-up resistor OFF
Port 4	Input	Programmable pull-up resistor ON

Name	Output level
C1 to C16	VSS (Display OFF)
S1 to S48	VSS (Display OFF)

1. Absolute Maximum Ratings at VSS=0V and Ta=25°C

Parameter		Symbol	Pins	Conditions		Ratings			unit
					VDD[V]	min.	typ.	max.	
Supply voltage		VDDMAX	VDD			-0.3		+7.0	V
Input voltage		VI(1)	•Ports 71,72,73 • $\overline{\text{RES}}$			-0.3		VDD+0.3	
		VI(2)	VLCD			-0.3		+7.0	
Output voltage		VO(1)	•C1 to C16 •S1 to S48			-0.3		VLCD+0.3	
		VO(2)	•VOUT2 •CUP1,CUP2			-0.3		VDD+0.3	
		VO(3)	ADLC, $\overline{\text{EROE}}$			-0.3		VDD+0.3	
Input/output voltage		VIO(1)	•Ports 0,1,2,3,4,5 •Port 70			-0.3		VDD+0.3	
High level output current	Peak output current	IOPH(1)	•Ports 0,1,2,3,4,5 •ADLC, $\overline{\text{EROE}}$	•CMOS output •At each pin		-4			mA
	Total output current	ΣIOAH(1)	•Ports 0,2,3 •C1-C16,S1-S48 •ADLC, $\overline{\text{EROE}}$	Total all pins		-25			
		ΣIOAH(2)	Ports 1, 4, 5	Total all pins		-25			
Low level output current	Peak output current	IOPL(1)	•Ports 0,1,2,3,4,5 •ADLC, $\overline{\text{EROE}}$	At each pin				20	
		IOPL(2)	Port 70	At each pin				15	
	Total output current	ΣIOAL(1)	Port 0	Total all pins				40	
		ΣIOAL(2)	•Port 2 •ADLC, $\overline{\text{EROE}}$	Total all pins				40	
		ΣIOAL(3)	Port 3	Total all pins				40	
		ΣIOAL(4)	Ports 1, 5	Total all pins				40	
		ΣIOAL(5)	Port 4	Total all pins				40	
		ΣIOAL(6)	Port 70	Total all pins				15	
		ΣIOAL(7)	C1-C16,S1-S48	Total all pins				30	
Operating temperature range		Topr				-30		+70	°C
Storage temperature range		Tstg				-65		+150	

Notes :
The specifications above are for a die mounted in a QIC160 type package.
However, we ship this product as a die only, not a package chip.
Therefore, the operational characteristics may vary depending on the user's packaging techniques.

2. Recommended Operating Range at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
Operating supply voltage range	VDD(1)	VDD	0.98μs ≤ tCYC ≤ 400μs		4.5		6.0	V
	VDD(2)		1.9μs ≤ tCYC ≤ 400μs		4.5		6.0	
	VDD(3)		3.9μs ≤ tCYC ≤ 400μs		2.5		6.0	
Hold voltage	VHD	VDD	RAMs and the registers hold voltage at HOLD mode.		2.0		6.0	
LCD display voltage	VLCD	VLCD		2.5-3.0	VDD		6.0	
				3.0-6.0	VDD		6.0	
Input high voltage	VIH(1)	Port 0 (Schmitt)	Output disable	2.5-6.0	0.4VDD +0.9		VDD	
	VIH(2)	•Ports 1,2,3,4,5 •Ports 72,73 (Schmitt)	Output disable	2.5-6.0	0.75VDD		VDD	
	VIH(3)	•Port 70 for Port input/interrupt •Port 71 • $\overline{\text{RES}}$ (Schmitt)	Output N-channel Tr. OFF	2.5-6.0	0.75VDD		VDD	
	VIH(4)	Port 70 for watchdog timer	Output N-channel Tr. OFF	2.5-6.0	0.9VDD		VDD	
Input low voltage	VIL(1)	Port 0 (Schmitt)	Output disable	2.5-6.0	VSS		0.2VDD	
	VIL(2)	•Ports 1,2,4,5 •Ports 72,73 (Schmitt)	Output disable	2.5-6.0	VSS		0.25VDD	
	VIL(3)	•Port 70 Port input/interrupt •Port 71 • $\overline{\text{RES}}$	Output N-channel Tr. OFF	2.5-6.0	VSS		0.25VDD	
	VIL(4)	Port 70 for watchdog timer	Output N-channel Tr. OFF	2.5-6.0	VSS		0.8VDD -1.0	
Operation cycle time	tCYC		excluding external memory access function	4.5-6.0	0.98		400	μs
				2.5-6.0	3.9		400	
			for external memory access	4.5-6.0	1.9		400	
				2.5-6.0	3.9		400	
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	•12MHz (ceramic resonator oscillation) •Refer to figure 1	4.5-6.0	11.76	12	12.24	MHz
	FmCF(2)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 1	4.5-6.0	5.88	6	6.12	
	FmCF(3)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 1	2.5-6.0	2.94	3	3.06	
	FmRC		RC oscillation	2.5-6.0	0.4	0.8	2.0	
	FsXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 2	2.5-6.0		32.768		kHz

Continue.

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
Oscillation stabilizing time period (Note 1)	tmsCF(1)	CF1, CF2	•12MHz (ceramic resonator oscillation) •Refer to figure 3	4.5-6.0		0.02	0.3	ms
	tmsCF(2)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 3	4.5-6.0		0.02	0.3	
	tmsCF(3)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 3	4.5-6.0		0.1	1	
				2.5-6.0		0.1	3	
	tssXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 3	4.5-6.0		1	1.5	s
				2.5-6.0		1	3	

(Note 1) The oscillation constant is shown on table 1 and table 2.

3. Electrical Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Input high current	IIH(1)	•Ports 1,2,3,4,5 •Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr. OFF •VIN=VDD (including the off-leak current of the output Tr.)	2.5-6.0			1	μA
	IIH(2)	Port 7 without pull-up MOS Tr.	•Output Nch Tr. OFF •VIN=VDD (including the off-leak current of the output Tr.)	2.5-6.0			1	
	IIH(3)	$\overline{RES}$	VIN=VDD	2.5-6.0			1	
Input low current	IIL(1)	•Ports 1,2,3,4,5 •Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr. OFF •VIN=VSS (including the off-leak current of the output Tr.)	2.5-6.0	-1			
	IIL(2)	Port 7 without pull-up MOS Tr.	•Output Nch Tr. OFF •VIN=VSS (including the off-leak current of the output Tr.)	2.5-6.0	-1			
	IIL(3)	$\overline{RES}$	VIN=VSS	2.5-6.0	-1			
Output high voltage	VOH(1)	Port 0 of CMOS output	IOH=-10mA	4.5-6.0	VDD-2.2			V
	VOH(2)		IOH=-1mA	2.5-6.0	VDD-0.4			
	VOH(3)	•Ports 1,2,3,4,5 of CMOS output •ADLC, $\overline{EROE}$	IOH=-1.0mA	4.5-6.0	VDD-1			
	VOH(4)		IOH=-0.1mA	2.5-6.0	VDD-0.5			
Output low voltage	VOL(1)	•Ports 0,1,2,3,4,5 •ADLC, $\overline{EROE}$	IOL=10mA	4.5-6.0			1.5	
	VOL(2)		IOL=1.6mA	4.5-6.0			0.4	
	VOL(3)		•IOL=1.0mA •The current of any measurement pin is not over 1mA.	2.5-6.0			0.4	
	VOL(4)	Port 70	IOL=1mA	4.5-6.0			0.4	
	VOL(5)		IOL=0.5mA	2.5-6.0			0.4	
Pull-up MOS Tr. resistor	Rpu	•Ports 0,1,2,3,4,5 •Port 7	VOH=0.9VDD	4.5-6.0	15	40	70	kΩ
				2.5-4.5	25	60	120	
Hysteresis voltage	VHIS	•Ports 0,1,2,3,4,5 •Port 7 • $\overline{RES}$	Output disable	2.5-6.0		0.1VDD		V
Pin capacitance	CP	All pins	•f=1MHz •Unmeasurement terminals for the input are set to VSS level. •Ta=25°C	2.5-6.0		10		pF

4. Serial Input/Output Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter			Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0, SCK1	Refer to figure 5.	2.5-6.0	2			tCYC
		Low Level pulse width	tCKL(1)				1			
		High Level pulse width	tCKH(1)				1			
	Output clock	Cycle	tCKCY(2)	SCK0, SCK1	•Use pull-up resistor (1kΩ) when Nch open-drain output. •Refer to figure 5.	2.5-6.0	2			
		Low Level pulse width	tCKL(2)					1/2 tCKCY		
		High Level pulse width	tCKH(2)					1/2 tCKCY		
Serial input	Data set up time		tICK	•SI0,SI1 •SB0,SB1	•Data set-up to SCK0,1 •Data hold from SCK0,1 •Refer to figure 5.	4.5-6.0	0.1			µs
						2.5-6.0	0.4			
						4.5-6.0	0.1			
	Data hold time		tCKI			2.5-6.0	0.4			
Serial output	Output delay time (Serial clock is external clock)		tCKO(1)	•SO0,SO1 •SB0,SB1	•Data set-up to SCK0,1 •Use pull-up resistor (1kΩ) when Nch open-drain output. •Refer to figure 5.	4.5-6.0			7/12 tCYC +0.2	
						2.5-6.0			7/12 tCYC +1	
	Output delay time (Serial clock is internal clock)		tCKO(2)	•SO0,SO1 •SB0,SB1	•Data hold from SCK0,1 •Use pull-up resistor (1kΩ) when Nch open-drain output. •Refer to figure 5.	4.5-6.0			1/3 tCYC +0.2	
						2.5-6.0			1/3 tCYC +1	

5. Pulse Input Conditions at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Ratings				unit
				VDD[V]	min.	typ.	max.	
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN •Refer to figure 6	•Interrupt acceptable •Timer0-countable	2.5-6.0	1			tCYC
	tPIH(2) tPIL(2)	•INT3/T0IN (The noise rejection clock is selected to 1/1.) •Refer to figure 6	•Interrupt acceptable •Timer0-countable	2.5-6.0	2			
	tPIH(3) tPIL(3)	•INT3/T0IN (The noise rejection clock is selected to 1/16.) •Refer to figure 6	•Interrupt acceptable •Timer0-countable	2.5-6.0	32			
	tPIH(4) tPIL(4)	•INT3/T0IN (The noise rejection clock is selected to 1/64.) •Refer to figure 6	•Interrupt acceptable •Timer0-countable	2.5-6.0	128			
	tPIL(5)	• $\overline{\text{RES}}$ •Refer to figure 6	Reset acceptable	2.5-6.0	200			μs

6. Current Dissipation Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	OCR7	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Current drain during basic operation (Note 2)	IDDOP(1)	VDD	•FmCF=12MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : 12MHz •Internal RC oscillation stops	0	4.5-6.0		10	25	mA
	IDDOP(2)		•FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : 6MHz •Internal RC oscillation stops	1	4.5-6.0		10	25	
	IDDOP(3)		•FmCF=3MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : 3MHz •Internal RC oscillation stops	0	4.5-6.0		3	9	
	IDDOP(4)			1			6	15	
	IDDOP(5)			0	2.5-4.5		1.5	5	
	IDDOP(6)		•FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation	0	4.5-6.0		0.7	3.4	
	IDDOP(7)			1			1.2	4.5	
	IDDOP(8)			0	2.5-4.5		0.4	2.8	
	IDDOP(9)			1			0.8	3.6	
	IDDOP(10)		•FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : 32.768kHz •Internal RC oscillation stops	0	4.5-6.0		38	150	μA
	IDDOP(11)			1			60	300	
	IDDOP(12)			0	2.5-4.5		15	70	
	IDDOP(13)			1			25	120	

*OSCR : Bit 7 of the oscillation control register.

Continue.

Parameter	Symbol	Pins	Conditions	OCR7	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Current drain in HALT mode (Note 2)	IDDHALT(1)	VDD	•HALT mode •FmCF=12MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : 12MHz •Internal RC oscillation stops	0	4.5-6.0		5.0	14	mA
	IDDHALT(2)		•HALT mode •FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : 6MHz •Internal RC oscillation stops	1	4.5-6.0		5.0	14	
	IDDHALT(3)		•HALT mode •FmCF=3MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : 3MHz •Internal RC oscillation stops	0	4.5-6.0		2.3	7	
	IDDHALT(4)			1			4.5	15	
	IDDHALT(5)			0	2.5-4.5		0.8	4	
	IDDHALT(6)		•HALT mode •FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation	0	4.5-6.0		400	1600	
	IDDHALT(7)			1			600	2400	
	IDDHALT(8)			0	2.5-4.5		200	1300	
	IDDHALT(9)			1			350	1500	
	IDDHALT(10)		•HALT mode •FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : 32.768kHz •Internal RC oscillation stops	0	4.5-6.0		25	100	μA
	IDDHALT(11)			1			36	140	
	IDDHALT(12)			0	2.5-4.5		8	55	
	IDDHALT(13)			1			12	85	
Current drain in HOLD mode (Note 2)	IDDHOLD(1)	VDD	HOLD mode		4.5-6.0		0.05	30	
	IDDHOLD(2)				2.5-4.5		0.02	20	

(Note 2) The currents of the output transistors, pull-up transistors and the LCD bleeder resistors are ignored. Refer to figure 7.

7. LCD Voltage and LCD Driver Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins, Conditions		VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
VX-Ci drop voltage (X : 1 to 5) (i : 1 to 16)	|VD1|	•Only a Ci terminal for –15µA •LCD display ON •1/5 bias •V5=VDD		2.9			120	mV
				5.0			200	
VX-Ci drop voltage (X : 1 to 5) (i : 1 to 16)	|VD2|	•Only a Ci terminal for +15µA •LCD display ON •1/5 bias •V5=VDD		2.9	-120			
				5.0	-200			
VX-Si drop voltage (X : 1 to 5) (i : 1 to 48)	|VD3|	•Only a Si terminal for -15µA •LCD display ON •1/5 bias •V5=VDD		2.9			120	
				5.0			200	
VX-Si drop voltage (i : 1 to 5) (i : 1 to 48)	|VD4|	•Only a Si terminal for +15µA •LCD display ON •1/5 bias •V5=VDD		2.9	-120			
				5.0	-200			
V4 output voltage	VV4	•LCD clock frequency=0Hz •LCD display ON •1/5 bias •V5=VDD •Refer to figure 9		2.9	0.75VDD	0.80VDD	0.85VDD	V
				5.0				
V3 output voltage	VV3			2.9	0.55VDD	0.60VDD	0.65VDD	
				5.0				
V2 output voltage	VV2			2.9	0.35VDD	0.40VDD	0.45VDD	
				5.0				
V1 output voltage	VV1			2.9	0.15VDD	0.20VDD	0.25VDD	
				5.0				
LCD display current	ILCD1	•LCD display ON •1/5 bias •VLCD=VDD •V1-V5 are opened •Refer to figure 8	20kΩ mode	5	25	50	100	µA
				2.9	15	29	60	
	ILCD2		4KΩ mode	5	125	250	500	
				2.9	75	150	300	
Step-up output voltage	VOUT2	•V1-V5 resistor=20kΩ •LCD display ON •LVCR0=1 (doubler) •VOUT2 •VDD=2.5 to 3.0V •C5=C6=0.1µF •Refer to figure 10	•IL=100µA •step-up clock : RC oscillation	2.7	4.4	4.6	5.4	V
				3	5.6	5.8	6.0	
			•IL=500µA •step-up clock : RC oscillation	2.7	4.2	4.5	5.4	
				3	5.2	5.6	6.0	
			•IL=100µA •step-up clock : crystal oscillation	2.7	4.3	4.5	5.4	
				3	5.4	5.7	6.0	
			•IL=500µA •step-up clock : crystal oscillation	2.7	4.0	4.3	5.4	
				3	5.0	5.4	6.0	
Contrast current (VLCD terminal)	ILC1	•LCD display ON •V5=VDD-0.5V •VLCD=VDD •Refer to figure 11	VCCR=1	5	0.8	1.6	3.2	mA
	ILC2		VCCR=2	5	0.4	0.8	1.6	
	ILC3		VCCR=4	5	0.2	0.4	0.8	
	ILC4		VCCR=8	5	0.1	0.2	0.4	µA
	ILC5		VCCR=10H	5	0.05	0.1	0.2	

VCCR : The LCD contrast control register
LVCR0 : Bit 0 of the LCD bias control register

Table 1. Ceramic resonator oscillation recommended constant (main clock)

Oscillation type	Maker	Oscillator	C1	C2
12MHz ceramic resonator oscillation	Murata	CSA12.0MT	33pF	33pF
		CST12.00MTW	on chip	
	Kyocera	KBR-12.0M	33pF	33pF
6MHz ceramic resonator oscillation	Murata			
			on chip	
	Kyocera			
			on chip	
3MHz ceramic resonator oscillation	Murata	CSA3.0MG	33pF	33pF
		CST3.0MGW	on chip	
	Kyocera	KBR-3.0MS	47pF	47pF

* Both C1 and C2 must use K rank (±10%) and SL characteristics.

Table 2. Crystal oscillation guaranteed constant (sub clock)

Oscillation type	Maker	Oscillator	C3	C4
32.768kHz crystal oscillation	CITIZEN	CFS-308	18pF	18pF
	SII	DT-VT-200	18pF	18pF

* Both C3 and C4 must use J rank (±5%) and CH characteristics.
(It is about the application which is not in need of high precision. Use K rank (±10%) and SL characteristics.)

(Notes) •Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
•If you use other oscillators herein, we provide no guarantee for the characteristics.

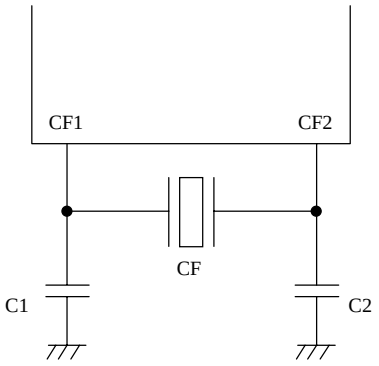


Figure 1 Ceramic oscillation circuit

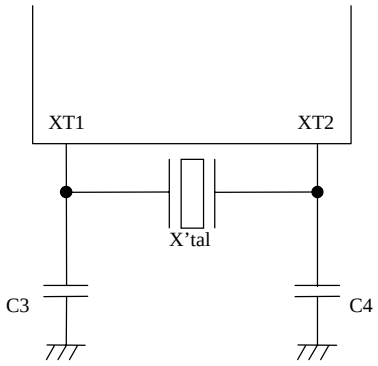


Figure 2 Crystal oscillation circuit

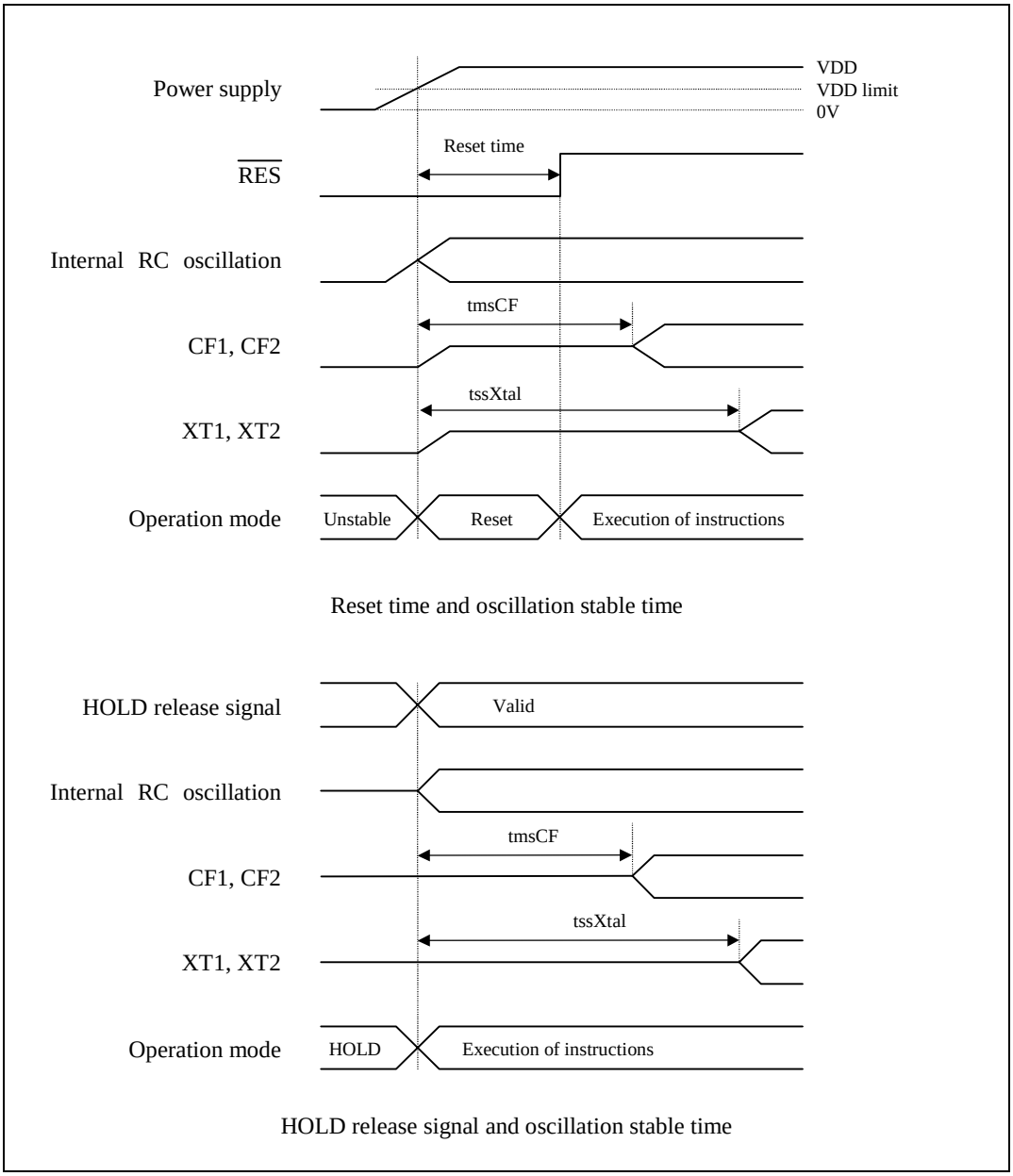
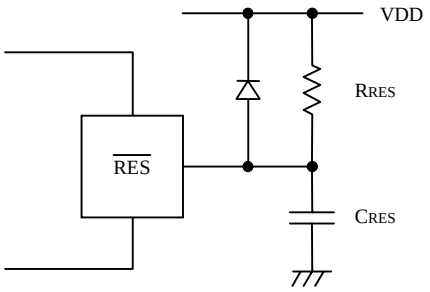


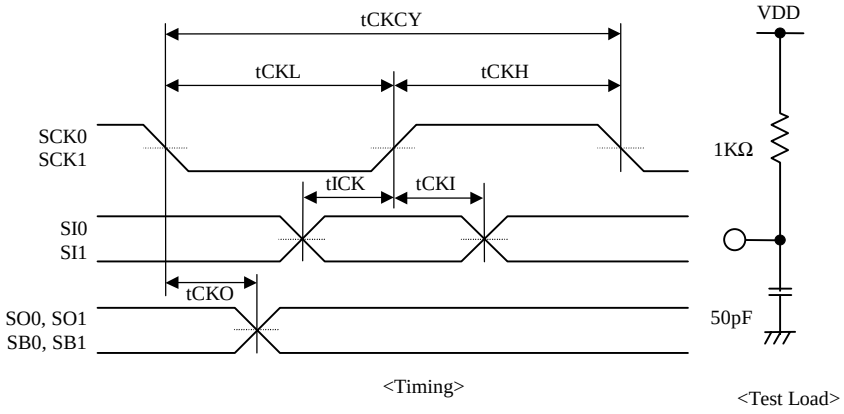
Figure 3 Oscillation stable time



(Note) Fix the value of CRES, RRES that is sure to reset until 200μs, after Power supply has been over inferior limit of supply voltage.

Figure 4 Reset circuit

<AC Timing Point>



<Timing> <Test Load>

Figure 5 Serial input / output test condition

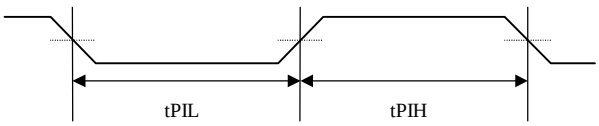


Figure 6 Pulse input timing condition

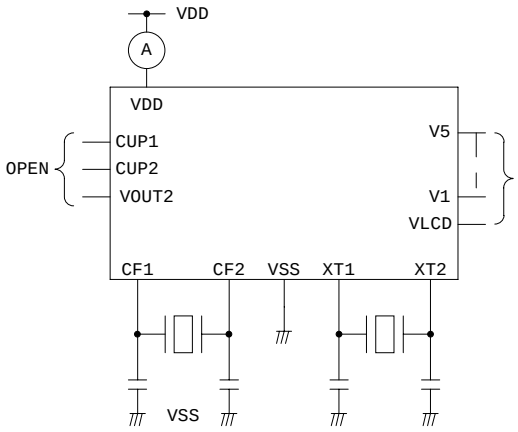


Figure 7 Current dissipation measurement

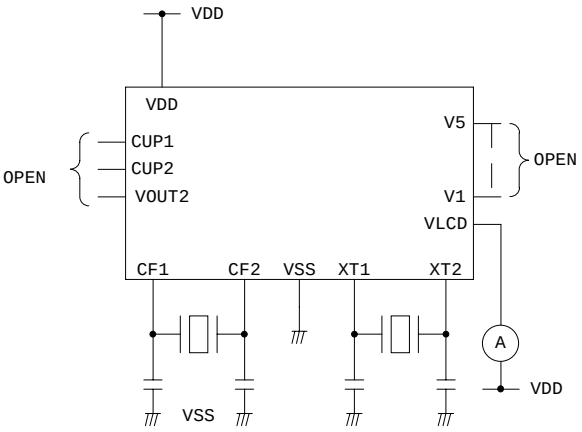


Figure 8 LCD display current measurement

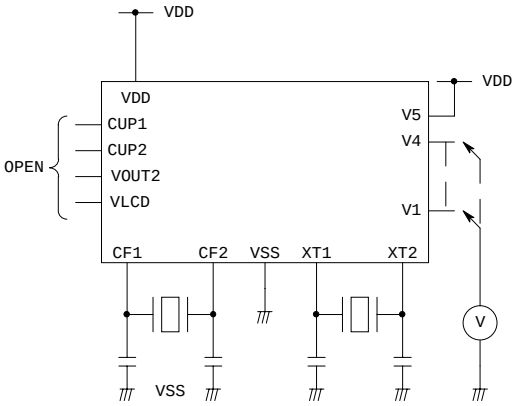


Figure 9 Output voltage of V1-V4 measurement

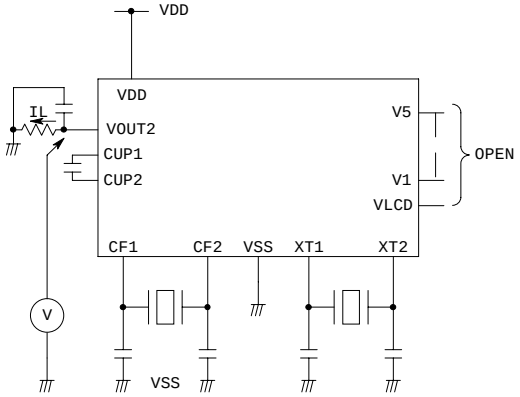


Figure 10 Step up output voltage measurement

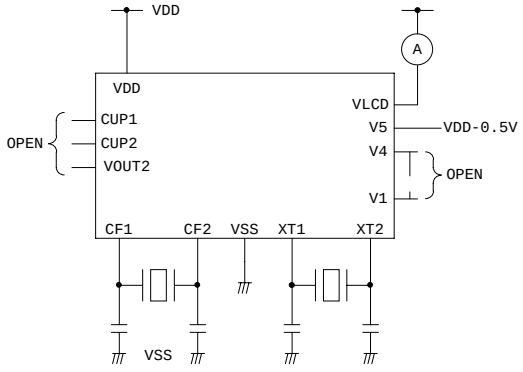


Figure 11 Contrast current measurement

8. AC Characteristics at Ta=-30°C to +70°C, VSS=0V

Load capacity : 100pF (Port 0, ADLC, $\overline{\text{EROE}}$)
Load capacity : 80pF (Output terminals except above)
*tCLCL=1/12 tCYC

External program memory timing

Parameter	Symbol	Pads and Conditions		Ratings		unit
			VDD[V]	min.	max.	
ADLC pulse width	tLHLL		4.5 - 6.0	2tCLCL-40		ns
			2.5 - 6.0	2tCLCL-160		
Address settling time	tAVLL	For ADLC	4.5 - 6.0	tCLCL-40		
			2.5 - 6.0	tCLCL-160		
Address hold time	tLLAX	For ADLC	4.5 - 6.0	tCLCL-35		
			2.5 - 6.0	tCLCL-140		
ADLC → control signal	tLLEL	For $\overline{\text{EROE}}$	4.5 - 6.0	tCLCL-25		
			2.5 - 6.0	tCLCL-100		
$\overline{\text{EROE}}$ pulse width	tELEH		4.5 - 6.0	3tCLCL-35		
			2.5 - 6.0	3tCLCL-140		
Data delay time	tELIV	From $\overline{\text{EROE}}$	4.5 - 6.0		3tCLCL-125	
			2.5 - 6.0		3tCLCL-400	
Data hold time	tEHIX	For $\overline{\text{EROE}}$	4.5 - 6.0	0		
			2.5 - 6.0	0		
$\overline{\text{EROE}}$ → address in	tEHAV		4.5 - 6.0	tCLCL-8		
			2.5 - 6.0	tCLCL-32		

Refer to figure 12.

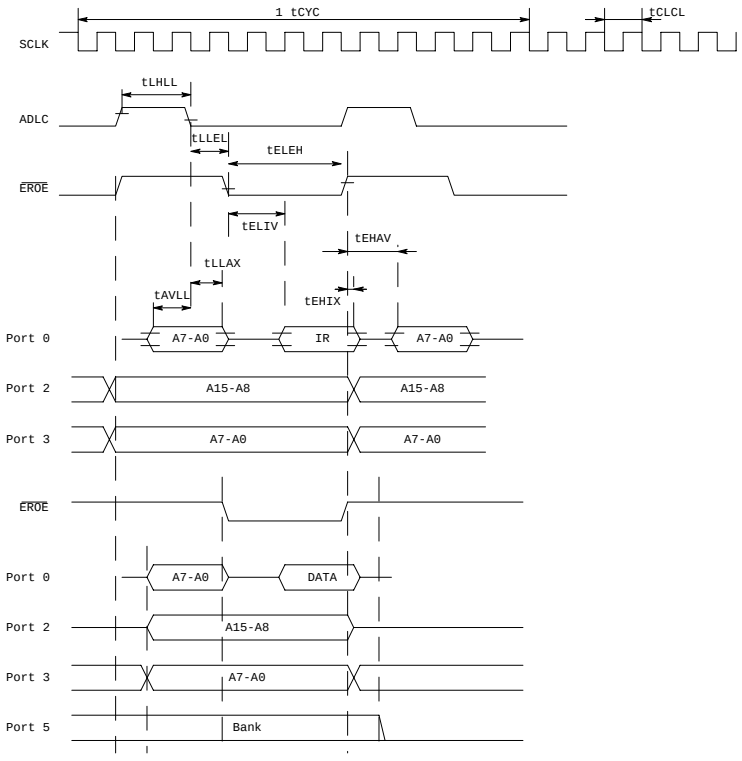


Figure 12 Timing of the external Program Memory/Data Memory

External data memory timing

Parameter	Symbol	Pads and Conditions	VDD[V]	Ratings min.	Ratings max.	unit
$\overline{RD}$ pulse width	tRLRH		4.5 - 6.0	6tCLCL-80		ns
			2.5 - 6.0	6tCLCL-320		
$\overline{WR}$ pulse width	tWLWH		4.5 - 6.0	6tCLCL-80		
			2.5 - 6.0	6tCLCL-320		
Data address hold time	tLLAX	For ADLC (at LDX)	4.5 - 6.0	2tCLCL-35		
			2.5 - 6.0	2tCLCL-140		
		For ADLC (at STX)	4.5 - 6.0	2tCLCL-35		
			2.5 - 6.0	2tCLCL-140		
Data delay time	tRLDV	From $\overline{RD}$	4.5 - 6.0		5tCLCL-125	
			2.5 - 6.0		5tCLCL-400	
Data hold time	tRHDX	From $\overline{RD}$	4.5 - 6.0	0		
			2.5 - 6.0	0		
Data floating time	tRHDZ	From $\overline{RD}$	4.5 - 6.0	2tCLCL-70	2tCLCL+70	
			2.5 - 6.0	2tCLCL-280	2tCLCL+280	
Data address setting time	tAVLL	For ADLC	4.5 - 6.0	tCLCL-40		
			2.5 - 6.0	tCLCL-160		
ADLC → control signal	tLLRL	For $\overline{RD}$	4.5 - 6.0	3tCLCL-50	3tCLCL+50	
			2.5 - 6.0	3tCLCL-200	3tCLCL+200	
	tLLWL	For $\overline{WR}$	4.5 - 6.0	3tCLCL-50	3tCLCL+50	
			2.5 - 6.0	3tCLCL-200	3tCLCL+200	
Data settling time	tQVWL	For $\overline{WR}$	4.5 - 6.0	tCLCL-60		
			2.5 - 6.0	tCLCL-240		
Data in $\overline{WR}$ =1	tQVWH		4.5 - 6.0	7tCLCL-140		
			2.5 - 6.0	7tCLCL-560		
Data hold time	tWHQX	From $\overline{WR}$	4.5 - 6.0	tCLCL-50		
			2.5 - 6.0	tCLCL-200		
Control signal → ADLC	tRHLH	For $\overline{RD}$	4.5 - 6.0	tCLCL-50	tCLCL+50	
			2.5 - 6.0	tCLCL-200	tCLCL+200	
	tWHLH	For $\overline{WR}$	4.5 - 6.0	tCLCL-50	tCLCL+50	
			2.5 - 6.0	tCLCL-200	tCLCL+200	

Refer to figure 13.

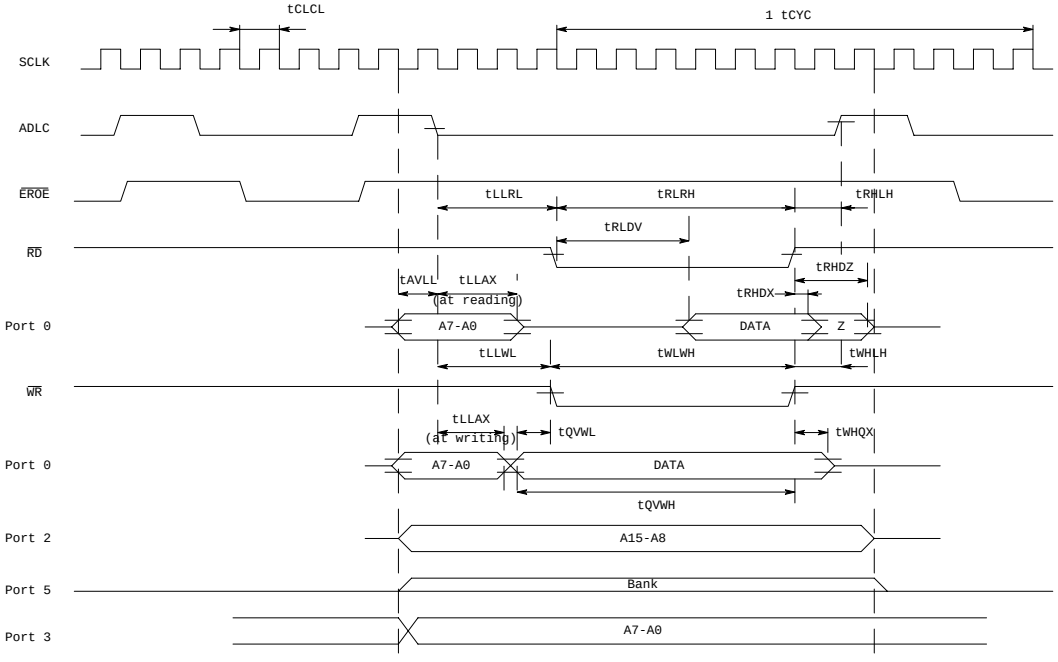
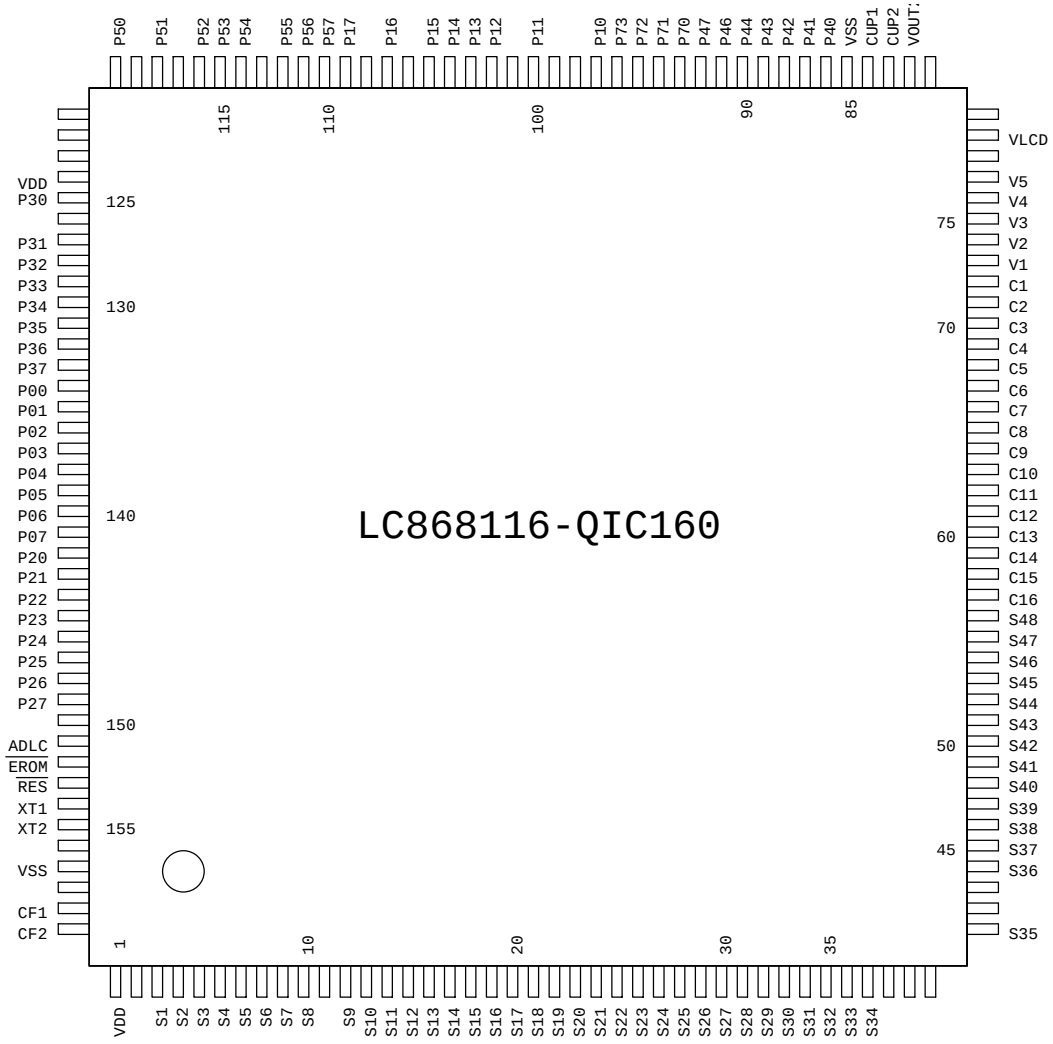


Figure 13 Timing of the external RAM

• Evaluation Sample (ES)

The factory shipment of this microcomputer is chip.
But there are two types of shipment of evaluation sample.
One type is chip and the other is package (QIC160).
If you selected package type, please refer to the following pin assignment and layout, and make the user target board.

• Pin Assignment of evaluation sample (Package type)



• Layout of evaluation sample (Package type) : QIC160