Ordering number : ENN*6697

CMOS IC

LC865520A/16A/12A/08A/04A

8-Bit Single Chip Microcontroller with On-Chip 20/16/12/08/04K-Byte ROM and 512-Byte RAM

Preliminary

Overview

The LC865520A/16A/12A/08A/04A microcontrollers are 8-bit single chip microcontrollers with the following one-chip functional blocks:

- CPU : Operable at a minimum bus cycle time of 0.5µs (microsecond)
- On-chip ROM Maximum Capacity : 20K bytes
- On-chip RAM Capacity : 512 bytes (LC865520A/16A/12A/08A/04A)
- 16-bit timer /counter (or two 8-bit timers)
- 16-bit timer /PWM (or two 8-bit timers)
- 8-channel × 8-bit AD converter
- Two 8-bit synchronous serial-interface circuits
- 13-source 10-vectored interrupt system80

All of the above functions are fabricated on a single chip.

Features

(1) Read-Only Memory (ROM)
: LC865520A 20480 × 8 bits
: LC865516A 16384 × 8 bits
: LC865512A 12288 × 8 bits
: LC865508A 8192 × 8 bits
: LC865504A 4096 × 8 bits

(2) Random Access Memory (RAM) : LC865520A/16A/12A/08A/04A 512 × 8 bits

(3) Bus Cycle Time/Instruction Cycle Time

The LC865520A/16A/12A/08A/04A are constructed to read ROM twice within one instruction cycle. It has 1.7 times more performance capability within the same instruction cycle compared to our 4-bit microcomputers (LC66000 series).

Bus cycle time indicates the speed to read ROM.

Bus cycle time	Cycle time	Clock divider	System clock oscillation	Oscillation Frequency	Voltage
0.5µs	1µs	1/1	Ceramic resonator oscillation	6MHz	4.5V to 6.0V
2µs	4µs	1/2	Ceramic resonator oscillation	3MHz	2.5V to 6.0V
7.5µs	15µs	1/2	RC resonator oscillation	800kHz	2.5V to 6.0V
183µs	366µs	1/2	Crystal oscillation	32.768kHz	2.5V to 6.0V

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

(4) Ports
- Input/output ports : 3 ports (16 terminals : port 1,7,8)
  Input/output programmable in a bit
- Maximum 15V withstand input/output port : 2 ports (15 terminals)
  Input/output port programmable in nibble units : 1 port (8 terminals : port 0)
  (When the N-channel open drain output is selected, the data in a bit can be inputted.)
  Input/output port programmable in a bit : 1 port (7 terminals : port 3)
- Input ports : 2 ports (6 terminals : port 7,8)

(5) AD converter
- 8-channel × 8-bit AD converter

(6) Serial-interface
- 1 channel × 16-bit serial-interface (8-bit transmission available by program)
- 1 channel × 8-bit serial-interface
  LSB first/MSB first function available
- Internal 8-bit baud-rate generator in common with two serial-interface circuits

(7) Timer
- Timer 0
  16-bit timer/counter
  2-bit prescaler + 8-bit programmable prescaler
  Mode 0 : Two 8-bit timers with programmable prescaler
  Mode 1 : 8-bit timer with programmable prescaler + 8-bit counter
  Mode 2 : 16-bit timer with programmable prescaler
  Mode 3 : 16-bit counter
  The resolution of Timer is tCYC. (tCYC: cycle time)
- Timer 1
  16-bit timer/PWM
  Mode 0 : Two 8-bit timers
  Mode 1 : 8-bit timer + 8-bit PWM
  Mode 2 : 16-bit timer
  Mode 3 : Variable-bit PWM (9-16bits)
  In Mode 0 and Mode 1,the resolution of Timer and PWM is tCYC.
  In Mode 2 and Mode 3,the resolution of Timer and PWM selectable: tCYC or 1/2 tCYC by program.

- Base timer
  Every 500ms overflow system for a clock application (using 32.768kHz crystal oscillation for Base timer clock)
  Every 976μs, 3.9ms, 15.6ms, 62.5ms overflow system (using 32.768kHz crystal oscillation for Base timer clock)
  The Base timer clock selectable; 32.768kHz crystal oscillation, System clock, and programmable prescaler output of Timer 0

(8) Buzzer output
- The Buzzer sound frequency selectable; 4KHz, 2KHz (using 32.768kHz crystal oscillation for Base timer clock)

(9) Remote-control receiver circuit (Shares with P73/INT3/T0IN terminal)
- Noise Rejection function (the time constant of noize rejection filter: 1tCYC/16tCYC/64tCYC)
  (tCYC: instruction cycle time)
- Switch Polarity function

(10) Watchdog timer
- The watchdog timer is taken on RC outside
- Watchdog timer operation selectable: interrupt system, system reset

(11) Interrupt system
- 13-source 10-vectored interrupts :
  1. External interrupt INT0 (include watchdog timer)
  2. External interrupt INT1
  3. External interrupt INT2, Timer/counter T0L (Lower 8-bit)
  4. External interrupt INT3, Base timer
  5. Timer/counter T0H (Upper 8-bit)
  6. Timer T1L, Timer T1H
  7. Serial-interface SIO0
  8. Serial-interface SIO1
  9. AD converter
  10. Port 0
- Built-in Interrupt Priority control register
  Microcomputer allows 3 levels of interrupt; low level, high level, and highest level of multiplex interrupt. It can specify a low level or a high level interrupt priority from INT2/T0L through port 0
  (i.e. the above interrupt number from three through ten). It can also specify a low level or the highest level interrupt priority to INT0 and INT1.

(12) Subroutine stack levels
- 128 levels (Max.): Stack area included in RAM area

(13) Multiplication and division
16-bit × 8-bit (7 instruction cycle times)
16-bit / 8-bit (7 instruction cycle times)

(14) 3 oscillation circuits
- On-chip RC oscillation circuit using for the system clock.
- On-chip CR oscillation circuit using for the system clock.
- On-chip crystal oscillation circuit using for the system clock and for time-base clock.

(15) Standby function
- HALT mode function
  The HALT mode is used to reduce power dissipation. In this operation mode, program execution is stopped. This operation mode can be released by interrupt request signals or the initial system reset request signal.
- HOLD mode function
  The HOLD mode is used to freeze all the oscillations;
  RC (internal), CR and Crystal oscillations. This mode can be released by the following operations.
  - Reset terminal ($\overline{\text{RES}}$) set to Low level
  - P70/INT0/T0IN, P71/INT1/T0IN terminals set to assigned level (programmable)
  - Port 0 terminal/terminals set to Low level (programmable)

(16) Factory shipment
- DIP42S, QFP48E delivery form

(17) Development support tools

Evaluation (EVA) chip	:	LC866096
EPROM version	:	LC86E5420
One time version	:	LC86P5420
Emulator	:	EVA-86000 + ECB867100 (Evaluation chip board) + POD865400 (POD)

Notice for use

1. Follow the under table.

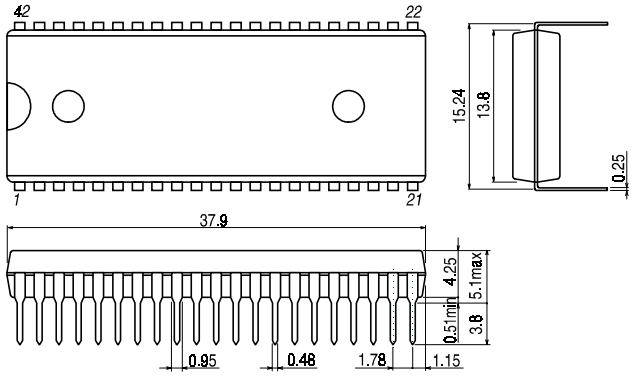
Frequency range of the system clock	Voltage range	Clock Divider	Note
15kHz to 30kHz	4.5V to 6.0V	1/1	Can not use 1/2 divider
30kHz to 6MHz		1/1,1/2	
15kHz to 30kHz	2.5V to 6.0V	1/1	Can not use 1/2 divider
30kHz to 1.5MHz		1/1,1/2	
1.5MHz to 3MHz		1/2	Can not use 1/1 divider
Internal RC oscillation	4.5V to 6.0V	1/1,1/2	
	2.5V to 6.0V	1/2	Can not use 1/1 divider

Pin Assignment

Package Dimension

(unit : mm)

3025B

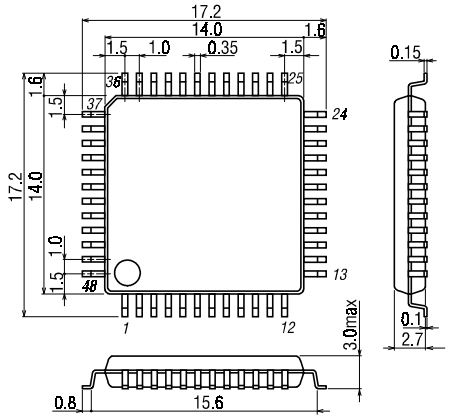


SANYO : DIP-42S(600mil)

Package Dimension

(unit : mm)

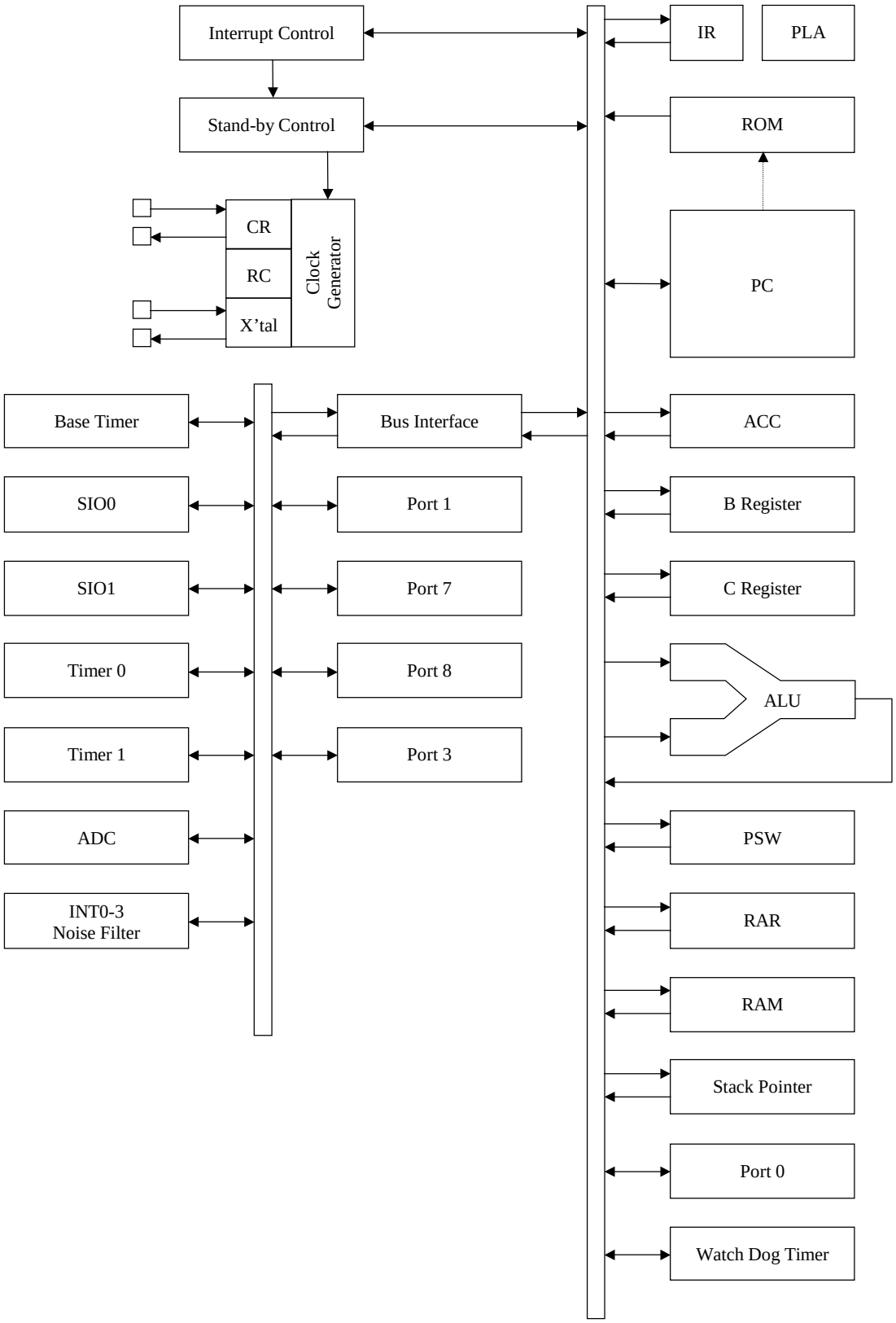
3156



SANYO : QIP-48E

*NC pin must not connect to anything.

System Block Diagram



Pin description

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function description</th><th>Option</th></tr>
<tr><td>VSS</td><td>-</td><td>Power pin (-)</td><td>-</td></tr>
<tr><td>VDD</td><td>-</td><td>Power pin (+)</td><td>-</td></tr>
<tr><td>PORT0
P00 to P07</td><td>I/O</td><td>•8-bit input/output port
•Input for port 0 interrupt
•Input/output in nibble units
•Input for HOLD release
•15V withstand at N-channel open drain output</td><td>•Pull-up resistor :
Provided/Not provided (each nibble)
•Output form :
CMOS/N-channel open drain (each bit)</td></tr>
<tr><td>PORT1
P10 to P17</td><td>I/O</td><td>•8-bit input/output port
•Input/output can be specified in a bit unit
•Other pin functions
P10 SIO0 data output
P11 SIO0 data input/bus input/output
P12 SIO0 clock input/output
P13 SIO1 data output
P14 SIO1 data input/bus input/output
P15 SIO1 clock input/output
P16 Buzzer output
P17 Timer 1 output (PWM0 output)</td><td>•Output form :
CMOS/N-channel open drain (each bit)</td></tr>
<tr><td>PORT3
P30 to P36</td><td>I/O</td><td>•7-bit input/output port
•Input/output in bit unit
•15V withstand at N-channel open drain output</td><td>•Pull-up resistor :
Provided/Not provided (each bit)
•Output form :
CMOS/N-channel open drain (each bit)</td></tr>
<tr><td>PORT7

P70 to P73

$\overline{P74}$, P75</td><td>

I/O

I</td><td>•4-bit input/output port
•Input/output in bit unit
•2-bit input port
•Other pin functions
P70 : INT0 input/HOLD release/N-channel Tr. output for watchdog timer
P71 : INT1 input/HOLD release input
P72 : INT2 input/timer 0 event input
P73 : INT3 input with noise filter/timer 0 event input
$\overline{P74}$: 32.768kHz crystal oscillation terminal XT1
P75 : 32.768kHz crystal oscillation terminal XT2
•Interrupt received forms, the vector addresses
<table>
<tr><th></th><th>rising</th><th>falling</th><th>rising & falling</th><th>high level</th><th>low level</th><th>vector</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr>
</table></td><td></td></tr>
</table>

Continue.

Pin name	I/O	Function description	Option
PORT8 P80 to 83 P84 to 87	 I I/O	•4-bit input port •Input/output in bit unit •4-bit input/output port •Other function AD input port (8Port pins)	-
$\overline{RES}$	I	Reset pin	-
XT1/$\overline{P74}$	I	•Input pin for 32.768kHz crystal oscillation •Other function XT1 : Input port $\overline{P74}$ •In case of non use, connect to VDD.	-
XT2/P75	O	•Output pin for 32.768kHz crystal oscillation •Other function XT2 : Input port P75 •In case of non use, connect to VDD at using as port or unconnect at using as oscillation.	-
CF1	I	Input pin for the ceramic resonator oscillation	-
CF2	O	Output pin for the ceramic resonator oscillation	-

* All of port options (except pull-up resistor of port 0) can be specified in bit unit.

*A state of pins at reset

Pin name	Input/output mode	A state of pull-up resistor specified at pull-up option
Port 0	Input	Fixed pull-up resistor OFF
Ports 1,3	Input	Programmable pull-up resistor OFF

1. Absolute Maximum Ratings at VSS=0V and Ta=25°C

Parameter		Symbol	Pins	Conditions	VDD[V]	Ratings min.	typ.	max.	unit
Supply voltage		VDDMAX	VDD	VDD		-0.3		+7.0	V
Input voltage		VI(1)	•Ports $\overline{74}$,75 •Ports 80,81,82,83 • $\overline{RES}$			-0.3		VDD+0.3	
Input/Output voltage		VIO(1)	•Port 1 •Ports 70,71,72,73 •Ports 84,85,86,87 •Ports 0, 3 at CMOS output option			-0.3		VDD+0.3	
		VIO(2)	Ports 0, 3 at N-ch open drain output option			-0.3		15	
High level output current	Peak output current	IOPH	•Ports 0, 1, 3 •Ports 71,72,73 •Ports 84,85,86,87	•CMOS output •At each pins		-10			mA
	Total output current	ΣIOAH(1)	Ports 0, 1	The total of all pins		-30			
		ΣIOAH(2)	Port 3	The total of all pins		-15			
		ΣIOAH(3)	•Ports 71,72,73 •Ports 84,85,86,87	The total of all pins		-10			
Low level output current	Peak output current	IOPL(1)	Ports 0, 1, 3	At each pins				20	
		IOPL(2)	•Ports 70,71,72,73 •Ports 84,85,86,87	At each pins				15	
	Total output current	ΣIOAL(1)	Ports 0,1,70	The total of all pins				60	
		ΣIOAL(2)	Port 3	The total of all pins				40	
		ΣIOAL(3)	•Ports 71,72,73 •Ports 84,85,86,87	The total of all pins				20	
Maximum power dissipation		Pdmax(1)	DIP42S	Ta=-30 to+70°C				630	mW
		Pdmax(2)	QFP48E	Ta=-30 to+70°C				390	
Operating temperature range		Topr				-30		70	°C
Storage temperature range		Tstg				-55		125	

2. Recommended Operating Range at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
Operating Supply voltage	VDD(1)	VDD	0.98μs ≤ tCYC tCYC ≤ 400μs		4.5		6.0	V
	VDD(2)		3.9μs ≤ tCYC tCYC ≤ 400μs		2.5		6.0	
Hold voltage	VHD	VDD	RAMs and the registers hold voltage at HOLD mode.		2.0		6.0	
Input high voltage	VIH(1)	Port 0 at CMOS output	Output disable	2.5 to 6.0	0.33VDD +1.0		VDD	
	VIH(2)	Port 0 at N-ch open drain output	Output disable	4.0 to 6.0	0.75VDD		13.5	
				2.5 to 4.0	0.8VDD		13.5	
	VIH(3)	•Port 1 •Ports 72,73 •Port 3 at CMOS output	Output disable	2.5 to 6.0	0.75VDD		VDD	
	VIH(4)	Port 3 at N-ch open drain output	Output disable	4.5 to 6.0	0.75VDD		13.5	
				2.5 to 4.0	0.8VDD		13.5	
	VIH(5)	•Port 70 Port input/interrupt •Port 71 • $\overline{RES}$	Output disable	2.5 to 6.0	0.75VDD		VDD	
	VIH(6)	Port 70 Watchdog timer	Output disable	2.5 to 6.0	0.9VDD		VDD	
	VIH(7)	•Port 8 •Ports $\overline{74}$,75	•Output disable •Using as port	2.5 to 6.0	0.75VDD		VDD	
Input low voltage	VIL(1)	Port 0 at CMOS output option	Output disable	2.5 to 6.0	VSS		0.2VDD	
	VIL(2)	Port 0 at N-ch open drain output	Output disable	2.5 to 6.0	VSS		0.25VDD	
	VIL(3)	•Ports 1,3 •Ports 72,73	Output disable	2.5 to 6.0	VSS		0.25VDD	
	VIL(4)	•Port 70 Port input/interrupt •Port 71 • $\overline{RES}$	Output disable	2.5 to 6.0	VSS		0.25VDD	
	VIL(5)	Port 70 Watchdog timer	Output disable	2.5 to 6.0	VSS		0.8VDD -1.0	
	VIL(6)	•Port 8 •Ports $\overline{74}$,75	•Output disable •Using as port	2.5 to 6.0	VSS		0.25VDD	
Operation cycle time	tCYC			4.5 to 6.0	0.98		400	μs
				2.5 to 6.0	3.9		400	
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 1	4.5 to 6.0	5.88	6	6.12	MHz
	FmCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 1	2.5 to 6.0	2.94	3	3.06	
	FmRC		RC oscillation	2.5 to 6.0	0.3	0.8	3.0	
	FsXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 2	2.5 to 6.0		32.768		kHz

Continue.

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Oscillation stabilizing time period (Note 1)	tmsCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 to 6.0				ms
	tmsCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 to 6.0				
				2.5 to 6.0				
	tssXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 3	4.5 to 6.0				s
				2.5 to 6.0				

(Note 1) The oscillation constant is shown on table 1 and table 2.

3. Electrical Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Ratings				unit
				VDD[V]	min.	typ.	max.	
Input high current	IIH(1)	Ports 0,3 at open drain output	•Output disable •VIN=13.5V (including off-leakage current of the output Tr.)	2.5 to 6.0			5	μA
	IIH(2)	•Port 0 without pull-up MOS Tr. •Ports 1,3 •Ports 70,71,72,73 •Port 8	•Output disable •Pull-up MOS Tr. OFF. •VIN=VDD (including off-leakage current of the output Tr.)	2.5 to 6.0			1	
	IIH(3)	$\overline{RES}$	VIN=VDD	2.5 to 6.0			1	
	IIH(4)	Ports $\overline{74}$,75	•VIN=VDD •Using as port	2.5 to 6.0			1	
Input low current	IIL(1)	•Ports 1,3 •Port 0 without pull-up MOS Tr. •Ports 70,71,72,73 •Port 8	•Output disable •Pull-up MOS Tr. OFF. •VIN=VSS (including off-leakage current of the output Tr.)	2.5 to 6.0	-1			
	IIL(2)	$\overline{RES}$	VIN=VSS	2.5 to 6.0	-1			
	IIL(3)	Ports $\overline{74}$,75	•VIN=VSS •Using as port	2.5 to 6.0	-1			
Output high voltage	VOH(1)	•Ports 0,1,3 of CMOS output	IOH=-1.0mA	4.5 to 6.0	VDD-1			V
	VOH(2)	•Ports 71,72,73 •Ports 84,85,86,87	IOH=-0.1mA	2.5 to 6.0	VDD-0.5			
Output low voltage	VOL(1)	Ports 0,1,3	IOL=10mA	4.5 to 6.0			1.5	
	VOL(2)		IOL=1.6mA	4.5 to 6.0			0.4	
	VOL(3)		•IOL=1.0mA •The current of any unmeasurement pin is not over 1mA.	2.5 to 6.0			0.4	
	VOL(4)	•Ports 71,72,73 •Ports 84,85,86,87	IOL=1.6mA	4.5 to 6.0			0.4	
	VOL(5)		•IOL=0.5mA •The current of any unmeasurement pin is not over 1mA.	2.5 to 6.0			0.4	
	VOL(6)	Port 70	IOL=1mA	4.5 to 6.0			0.4	
	VOL(7)		•IOL=0.5mA •The current of any unmeasurement pin is not over 1mA.	2.5 to 6.0			0.4	
Pull-up MOS Tr. resistor	Rpu	•Ports 0,1,3 •Ports 70,71,72,73 •Ports 84,85,86,87	VOH=0.9VDD	4.5 to 6.0	15	40	70	KΩ
				2.5 to 4.5	25	70	150	
Hysteresis voltage	VHIS	•Port 1 •Ports 70,71,72,73 • $\overline{RES}$	Output disable	2.5 to 6.0		0.1VDD		V
Pin capacitance	CP	All pins	•f=1MHz •VIN=VSS for all unmeasured terminals. •Ta=25°C	2.5 to 6.0		10		pF

4. Serial Input/Output Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter			Symbol	Pins	Conditions	Ratings				unit
						VDD[V]	min.	typ.	max.	
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0,SCK1	Refer to figure 5	2.5 to 6.0	2			tCYC
		Low Level pulse width	tCKL(1)				1			
		High Level pulse width	tCKH(1)				1			
	Output clock	Cycle	tCKCY(2)	SCK0,SCK1	•Use pull-up resistor (1kΩ) in the open drain output. •Refer to figure 5	2.5 to 6.0	2			
		Low Level pulse width	tCKL(2)					1/2tCKCY		
		High Level pulse width	tCKH(2)					1/2tCKCY		
Serial input	Data set-up time		tICK	•SI0,SI1 •SB0,SB1	•Data set-up to SCK0,1 •Data hold from SCK0,1 •Refer to figure 5	4.5 to 6.0	0.1			µs
						2.5 to 6.0	0.4			
	Data hold time		tCKI			4.5 to 6.0	0.1			
						2.5 to 6.0	0.4			
Serial output	Output delay time (External clock using for serial transfer clock)		tCKO(1)	•SO0,SO1 •SB0,SB1	•Use pull-up resistor (1kΩ) in the open drain output. •Data hold from SCK0,1 •Refer to figure 5	4.5 to 6.0			7/12 tCYC +0.2	
						2.5 to 6.0			7/12 tCYC +1	
	Output delay time (Internal clock using for serial transfer clock)		tCKO(2)			4.5 to 6.0			1/3 tCYC +0.2	
						2.5 to 6.0			1/3 tCYC +1	

5. Pulse Input Conditions at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				VDD[V]	min.	typ.	max.	
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN	•Interrupt acceptable •Timer0-countable	2.5 to 6.0	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock selected to 1/1.)	•Interrupt acceptable •Timer0-countable	2.5 to 6.0	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock selected to 1/16.)	•Interrupt acceptable •Timer0-countable	2.5 to 6.0	32			
	tPIH(4) tPIL(4)	INT3/T0IN (The noise rejection clock selected to 1/64.)	•Interrupt acceptable •Timer0-countable	2.5 to 6.0	128			
	tPIL(5)	$\overline{\text{RES}}$	Reset acceptable	2.5 to 6.0	200			µs

6. AD Converter Characteristics at Ta=-30°C to + 70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				VDD[V]	min.	typ.	max.	
Resolution	N			4.5 to 6.0		8		bit
Absolute precision (Note 2)	ET			4.5 to 6.0			±1.5	LSB
Conversion time	tCAD		AD conversion time = 16 × tCYC (ADCR2=0) (Note 3)	4.5 to 6.0	15.68 (tCYC= 0.98µs)		65.28 (tCYC= 4.08µs)	µs
			AD conversion time = 32 × tCYC (ADCR2=1) (Note 3)		31.36 (tCYC= 0.98µs)		130.56 (tCYC= 4.08µs)	
Analog input voltage range	VAIN	AN0 to AN7		4.5 to 6.0	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5 to 6.0			1	µA
	IAINL		VAIN=VSS	4.5 to 6.0	-1			

(Note 2) Absolute precision excepts the quantizing error (±1/2 LSB).

(Note 3) The conversion time means the time from executing the AD conversion instruction to setting the complete digital conversion value to the register.

7. Current Dissipation Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Ratings				unit
				VDD[V]	min.	typ.	max.	
Current dissipation during basic operation (Note 4)	IDDOP(1)	VDD	•FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/1 divided	4.5 to 6.0		7	18	mA
	IDDOP(2)		•FmCF=3MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/2 divided	4.5 to 6.0		3	7	
	IDDOP(3)			2.5 to 4.5		1.5	5	
	IDDOP(4)		•FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation •1/2 divided	4.5 to 6.0		0.7	3	
	IDDOP(5)			2.5 to 4.5		0.4	2.5	
	IDDOP(6)		•FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : 32.768kHz •Internal RC oscillation stops •1/2 divided	4.5 to 6.0		35	130	
	IDDOP(7)			2.5 to 4.5		15	70	

Continue.

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Current dissipation in HALT mode (Note 4)	IDDHALT(1)	VDD	•HALT mode •FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/1 divided	4.5 to 6.0		4	9	mA
	IDDHALT(2)		•HALT mode •FmCF=3MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/2 divided	4.5 to 6.0		2.2	5	
	IDDHALT(3)			2.5 to 4.5		0.8	3	
	IDDHALT(4)		•HALT mode FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation •1/2 divided	4.5 to 6.0		400	1600	μA
	IDDHALT(5)			2.5 to 4.5		200	1300	
	IDDHALT(6)		•HALT mode FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : crystal oscillation •Internal RC oscillation stops •1/2 divided	4.5 to 6.0		25	100	
	IDDHALT(7)			2.5 to 4.5		8	55	
Current dissipation in HOLD mode (Note 4)	IDDHOLD(1)	VDD	HOLD mode	4.5 to 6.0		0.05	30	
	IDDHOLD(2)			2.5 to 4.5		0.02	20	

(Note 4) The currents of the output transistors and the pull-up MOS transistors are ignored.

Table 1. Ceramic resonator oscillation recommended constant (main-clock)

Oscillation type	Maker	Oscillator	C1	C2
6MHz ceramic resonator oscillation	Murata	CSA6.00MG		
		CST6.00MGW		
	Kyocera	KBR-6.0MSA		
		PBRC6.00A (chip type)		
		KBR-6.0MKS		
		PBRC6.00B (chip type)		
3MHz ceramic resonator oscillation	Murata	CSA3.00MG		
		CST3.00MGW		
	Kyocera	KBR-3.0MS		

* Both C1 and C2 must be use K rank (±10%) and SL characteristics.

Table 2. Crystal oscillation guaranteed constant (sub-clock)

Oscillation type	Maker	Oscillator	C3	C4	Rd
32.768kHz crystal oscillation					

* Both C3 and C4 must be use J rank (±5%) and CH characteristics.
(Not in need of high precision, use K rank (±10%) and SL characteristics.)

(Notes) • Please place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length since the circuit pattern affects the oscillation frequency.
• If you use other oscillators herein, we provide no guarantee for the characteristics.

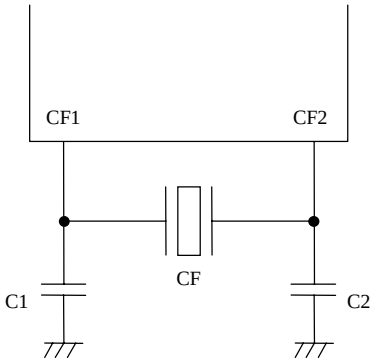


Figure 1 Main-clock circuit
Ceramic resonator oscillation

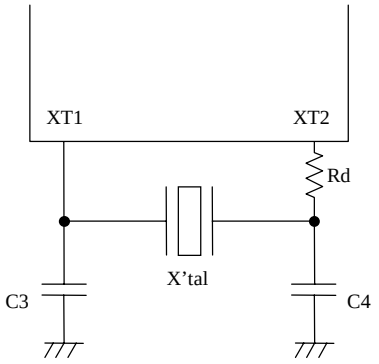


Figure 2 Sub-clock circuit
Crystal oscillation

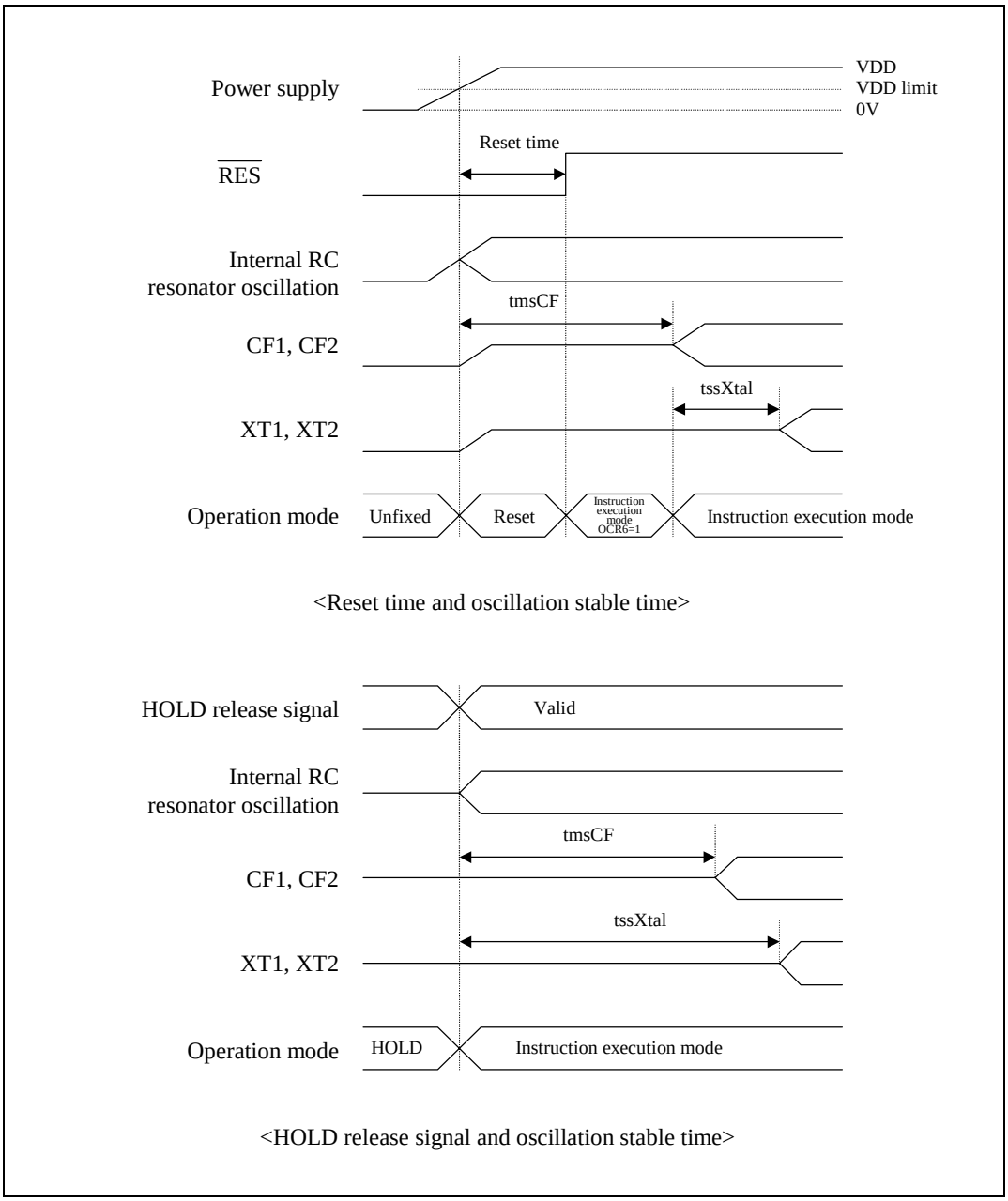
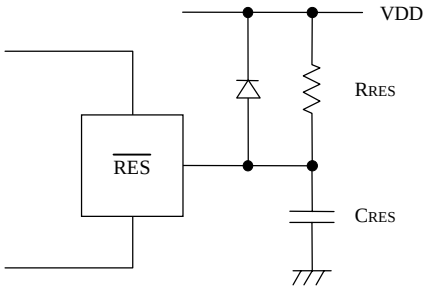


Figure 3 Oscillation stable time



(Note) Fix the value of CRES, RRES that is sure to reset until 200μs, after Power supply has been over inferior limit of supply voltage.

Figure 4 Reset circuit

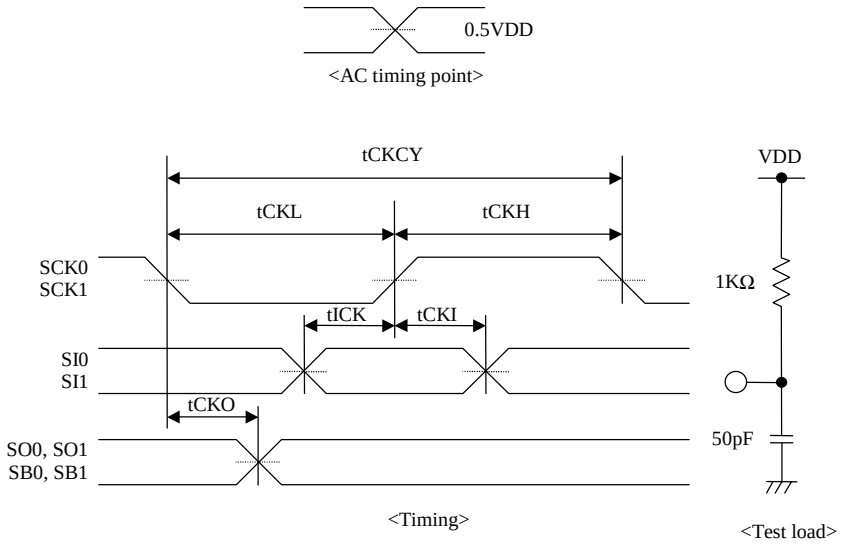


Figure 5 Serial input / output test condition

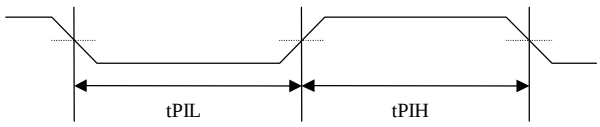


Figure 6 Pulse input timing condition

memo: