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**LC863332/28/24/20/16A**


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## 8-Bit Single Chip Microcontroller

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### Preliminary

#### Overview

The LC863332/28/24/20/16A are 8-bit single chip microcontrollers with the following on-chip functional blocks:

- CPU : Operable at a minimum bus cycle time of 0.424 $\mu$ s
- On-chip ROM capacity
  - Program ROM : 32K/28K/24K/20K/16K bytes
  - CGROM : 16K bytes
- On-chip RAM capacity : 512 bytes
- OSD RAM : 352  $\times$  9 bits
- Five channels  $\times$  8-bit AD Converter
- Three channels  $\times$  7-bit PWM
- Two 16-bit timer/counters, 14-bit base timer
- 8-bit synchronous serial interface circuit
- IIC-bus compliant serial interface circuit (Multi-master type)
- ROM correction function
- 15-source 9-vectored interrupt system
- Integrated system clock generator and display clock generator
  - X'tal oscillator (32.768kHz) for PLL reference is used for TV control.

All of the above functions are fabricated on a single chip.

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- (6) AD converter  
- 5 channels  $\times$  8-bit AD converters
- (7) Serial interfaces  
- IIC-bus compliant serial interface (Multi-master type)  
Consists of a single built-in circuit with two I/O channels. The two data lines and two clock lines can be connected internally.  
- Synchronous 8-bit serial interface
- (8) PWM output  
- 3 channels  $\times$  7-bit PWM
- (9) Timer  
- Timer 0 : 16-bit timer/counter  
With 2-bit prescaler + 8-bit programmable prescaler  
Mode 0 : Two 8-bit timers with a programmable prescaler  
Mode 1 : 8-bit timer with a programmable prescaler + 8-bit counter  
Mode 2 : 16-bit timer with a programmable prescaler  
Mode 3 : 16-bit counter  
The resolution of timer is 1 tCYC.  
- Timer 1 : 16-bit timer/PWM  
Mode 0 : Two 8-bit timers  
Mode 1 : 8-bit timer + 8-bit PWM  
Mode 2 : 16-bit timer  
Mode 3 : Variable bit PWM (9 to 16 bits)  
In mode0/1,the resolution of Timer1/PWM is 1 tCYC  
In mode2/3,the resolution is selectable by program; tCYC or 1/2 tCYC  
- Base timer  
Generate every 500ms overflow for a clock application (using 32.768kHz crystal oscillation for the base timer clock)  
Generate every 976 $\mu$ s, 3.9ms, 15.6ms, 62.5ms overflow (using 32.768kHz crystal oscillation for the base timer clock)  
Clock for the base timer is selectable from 32.768kHz crystal oscillation, system clock or programmable prescaler output of Timer 0
- (10) Remote control receiver circuit (connected to the P73/INT3/T0IN terminal)  
- Noise rejection function  
- Polarity switching
- (11) Watchdog timer  
External RC circuit is required  
Interrupt or system reset is activated when the timer overflows
- (12) ROM correction function  
Max 128 bytes / 2 addresses
- (13) Interrupts  
- 15 sources 9 vectored interrupts
1. External Interrupt INT0
  2. External Interrupt INT1
  3. External Interrupt INT2, Timer/counter T0L (Lower 8 bits)
  4. External Interrupt INT3, base timer
  5. Timer/counter T0H (Upper 8 bits)
  6. Timer T1H,T1L
  7. SIO0
  8. Vertical synchronous signal interrupt ( $\overline{VS}$ ), horizontal line ( $\overline{HS}$ ), AD
  9. IIC, Port 0

- Interrupt priority control

Three interrupt priorities are supported (low, high and highest) and multi-level nesting is possible. Low or high priority can be assigned to the interrupts from 3 to 9 listed above. For the external interrupt INT0 and INT1, high or highest priority can be set.

(14) Sub-routine stack level

- A maximum of 128 levels (stack is built in the internal RAM)

(15) Multiplication/division instruction

- 16 bits × 8 bits (7 instruction cycle times)
- 16 bits / 8 bits (7 instruction cycle times)

(16) 3 oscillation circuits

- Built-in RC oscillation circuit used for the system clock
- Built-in VCO circuit used for the system clock and OSD
- X'tal oscillation circuit used for base timer, system clock and PLL reference

(17) Standby function

- HALT mode

The HALT mode is used to reduce the power dissipation. In this operation mode, the program execution is stopped. This mode can be released by the interrupt request or the system reset.

- HOLD mode

The HOLD mode is used to stop the oscillations; RC (internal), VCO, and X'tal oscillations. This mode can be released by the following conditions.

- Pull the reset terminal ( $\overline{RES}$ ) to low level.
- Feed the selected level to either P70/INT0 or P71/INT1.
- Input the interrupt condition to Port 0.

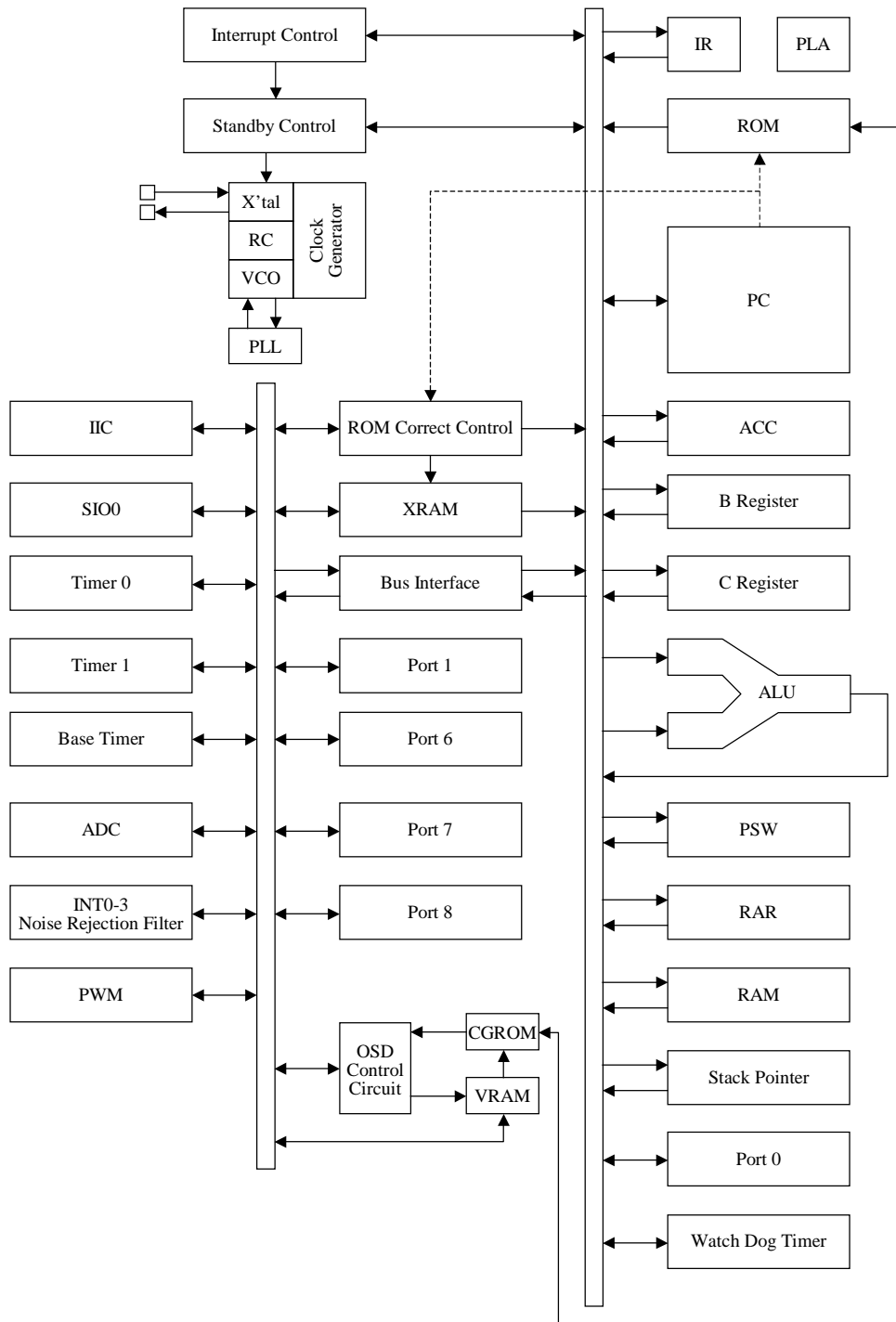
(18) Package

- DIP42S
- QIP48E

(19) Development tools

- Flash EEPROM: LC86F3348A
- Evaluation chip: LC863096
- Emulator: EVA86000 (main) + ECB863200 (evaluation chip board)  
+ POD863300 (pod: DIP42S) or POD863301 (QIP48E)

System Block Diagram





## Pin Description

Pin Description Table

Terminal	I/O	Function Description	Option														
VSS	-	Negative power supply															
XT1	I	Input terminal for crystal oscillator															
XT2	O	Output terminal for crystal oscillator															
VDD	-	Positive power supply															
$\overline{\text{RES}}$	I	Reset terminal															
FILT	O	Filter terminal for PLL															
$\overline{\text{VS}}$	I	Vertical synchronization signal input terminal															
$\overline{\text{HS}}$	I	Horizontal synchronization signal input terminal															
R	O	Red (R) output terminal of RGB image output															
G	O	Green (G) output terminal of RGB image output															
B	O	Blue (B) output terminal of RGB image output															
I	O	Intensity ( I ) output terminal of RGB image output															
BL	O	Fast blanking control signal Switch TV image signal and OSD image signal															
Port 0 P00 - P07	I/O	<ul style="list-style-type: none"> <li>•8-bit input/output port, Input/output can be specified in nibble unit</li> <li>•Other functions HOLD release input Interrupt input</li> </ul>	Pull-up resistor provided/not provided Output Format CMOS/Nch-OD														
Port 1 P10 - P17	I/O	<ul style="list-style-type: none"> <li>•8-bit input/output port Input/output can be specified in a bit</li> <li>•Other functions               <table border="1" data-bbox="474 991 899 1213"> <tr> <td>P10</td> <td>SIO0 data output</td> </tr> <tr> <td>P11</td> <td>SIO0 data input/bus input/output</td> </tr> <tr> <td>P12</td> <td>SIO0 clock input/output</td> </tr> <tr> <td>P13</td> <td>PWM1 output</td> </tr> <tr> <td>P14</td> <td>PWM2 output</td> </tr> <tr> <td>P15</td> <td>PWM3 output</td> </tr> <tr> <td>P17</td> <td>Timer1 (PWM) output</td> </tr> </table> </li> </ul>	P10	SIO0 data output	P11	SIO0 data input/bus input/output	P12	SIO0 clock input/output	P13	PWM1 output	P14	PWM2 output	P15	PWM3 output	P17	Timer1 (PWM) output	Output Format CMOS/Nch-OD
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P15	PWM3 output																
P17	Timer1 (PWM) output																
Port 6 P60 - P63	I/O	<ul style="list-style-type: none"> <li>•4-bit input/output port Input/output can be specified for each bit</li> <li>•Other functions               <table border="1" data-bbox="466 1344 899 1472"> <tr> <td>P60</td> <td>IIC0 data I/O</td> </tr> <tr> <td>P61</td> <td>IIC0 clock output</td> </tr> <tr> <td>P62</td> <td>IIC1 data I/O</td> </tr> <tr> <td>P63</td> <td>IIC1 clock output</td> </tr> </table> </li> </ul>	P60	IIC0 data I/O	P61	IIC0 clock output	P62	IIC1 data I/O	P63	IIC1 clock output							
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P62	IIC1 data I/O																
P63	IIC1 clock output																

Terminal	I/O	Function Description	Option																																											
Port 7 P70 P71 - P73	I/O	<ul style="list-style-type: none"> <li>•4-bit input/output port Input or output can be specified for each bit</li> <li>•Other function <table border="1" style="margin-left: 20px;"> <tr> <td>P70</td> <td>INT0 input/HOLD release input/ Nch-Tr. output for watchdog timer</td> </tr> <tr> <td>P71</td> <td>INT1 input/HOLD release input</td> </tr> <tr> <td>P72</td> <td>INT2 input/Timer 0 event input</td> </tr> <tr> <td>P73</td> <td>INT3 input (noise rejection filter connected)/ Timer 0 event input</td> </tr> </table> </li> </ul> <p>Interrupt receiver format, vector addresses</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th></th> <th>rising</th> <th>falling</th> <th>rising/ falling</th> <th>H level</th> <th>L level</th> <th>vector</th> </tr> </thead> <tbody> <tr> <td>INT0</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> <td>03H</td> </tr> <tr> <td>INT1</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> <td>0BH</td> </tr> <tr> <td>INT2</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> <td>13H</td> </tr> <tr> <td>INT3</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> <td>1BH</td> </tr> </tbody> </table>	P70	INT0 input/HOLD release input/ Nch-Tr. output for watchdog timer	P71	INT1 input/HOLD release input	P72	INT2 input/Timer 0 event input	P73	INT3 input (noise rejection filter connected)/ Timer 0 event input		rising	falling	rising/ falling	H level	L level	vector	INT0	enable	enable	disable	enable	enable	03H	INT1	enable	enable	disable	enable	enable	0BH	INT2	enable	enable	enable	disable	disable	13H	INT3	enable	enable	enable	disable	disable	1BH	
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INT3	enable	enable	enable	disable	disable	1BH																																								
Port 8 P83 P84-P87	I I/O	<ul style="list-style-type: none"> <li>•1-bit input port</li> <li>4-bit input/output port Input or output can be specified for each bit</li> <li>•Other function AD converter input port (5 lines)</li> </ul>																																												
NC	-	unused terminal Leave open																																												

- Output form and existence of pull-up resistor for all ports can be specified for each bit.
- Programmable pull-up resistor is always connected regardless of port option, CMOS or N-ch open drain output in port 1.
- Port status in reset

Terminal	I/O	Pull-up resistor status at selecting pull-up option
Port 0	I	Pull-up resistor OFF, ON after reset release
Port 1	I	Programmable pull-up resistor OFF



## 1. Absolute Maximum Ratings at VSS=0V and Ta=25°C

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD[V]	min.	typ.		max.
Supply voltage	VDDMAX	VDD			-0.3		+7.0	V
Input voltage	VI(1)	• $\overline{\text{RES}}$ , $\overline{\text{HS}}$ , $\overline{\text{VS}}$ , P83			-0.3		VDD+0.3	
Output voltage	VO(1)	R, G, B, I, BL, FILT			-0.3		VDD+0.3	
Input/output voltage	VIO	•Ports 0, 1, 6, 7, 84 to 87			-0.3		VDD+0.3	
High level output current	Peak output current	IOPH(1)	•Ports 0, 1, 7, 84 to 87	•CMOS output •For each pin.	-4			mA
		IOPH(2)	R, G, B, I, BL	•CMOS output •For each pin.	-5			
	Total output current	$\Sigma$ IOAH(1)	•Ports 0, 1	The total of all pins.	-20			
		$\Sigma$ IOAH(2)	Ports 7, 84 to 87	The total of all pins.	-10			
	$\Sigma$ IOAH(3)	R, G, B, I, BL	The total of all pins.	-15				
Low level output current	Peak output current	IOPL(1)	Ports 0, 1, 6, 84 to 87	For each pin.			20	
		IOPL(2)	Port 7	For each pin.			15	
		IOPL(3)	R, G, B, I, BL	For each pin.			5	
	Total output current	$\Sigma$ IOAL(1)	Ports 0, 1	The total of all pins.			40	
		$\Sigma$ IOAL(2)	Ports 6, 7, 84 to 87	The total of all pins.			40	
		$\Sigma$ IOAL(3)	R, G, B, I, BL	The total of all pins.			15	
Maximum power dissipation	Pdmax	DIP42S	Ta=-10 to +70°C				800	mW
		QIP48E					400	
Operating temperature range	Topr				-10		+70	°C
Storage temperature range	Tstg				-55		+125	

2. Recommended Operating Range at Ta= -10°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD[V]	min.	typ.		max.
Operating supply voltage range	VDD(1)	VDD	$0.844\mu\text{s} \leq t_{\text{CYC}} \leq 0.852\mu\text{s}$		4.5		5.5	V
	VDD(2)		$4\mu\text{s} \leq t_{\text{CYC}} \leq 400\mu\text{s}$		4.5		5.5	
Hold voltage	VHD	VDD	RAMs and the registers data are kept in HOLD mode.		2.0		5.5	
High level input voltage	VIH(1)	Port 0 (Schmitt)	Output disable	4.5 - 5.5	0.6VDD		VDD	
	VIH(2)	•Ports 1,6 (Schmitt) •Port 7 (Schmitt) port input/interrupt •HS, $\overline{\text{VS}}$ , $\overline{\text{RES}}$ (Schmitt)	Output disable	4.5 - 5.5	0.75VDD		VDD	
	VIH(3)	Port 70 Watchdog timer input	Output disable	4.5 - 5.5	VDD-0.5		VDD	
	VIH(4)	•Port 8 port input	Output disable	4.5 - 5.5	0.7VDD		VDD	
Low level input voltage	VIL(1)	Port 0 (Schmitt)	Output disable	4.5 - 5.5	VSS		0.2VDD	
	VIL(2)	•Ports 1,6 (Schmitt) •Port 7 (Schmitt) port input/interrupt •HS, $\overline{\text{VS}}$ , $\overline{\text{RES}}$ (Schmitt)	Output disable	4.5 - 5.5	VSS		0.25VDD	
	VIL(3)	Port 70 Watchdog timer input	Output disable	4.5 - 5.5	VSS		0.6VDD	
	VIL(4)	Port 8 port input	Output disable	4.5 - 5.5	VSS		0.3VDD	
Operation cycle time	tCYC(1)		•All functions operating	4.5 - 5.5	0.844	0.848	0.852	$\mu\text{s}$
	tCYC(2)		•AD converter operating •OSD is not operating	4.5 - 5.5	0.844		30	
	tCYC(3)		•OSD and AD converter are not operating	4.5 - 5.5	0.844		400	
Oscillation frequency range	FmRC		Internal RC oscillation	4.5 - 5.5	0.4	0.8	3.0	MHz

## 3. Electrical Characteristics at Ta=-10°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD[V]	min.	typ.		max.
High level input current	I <sub>IH</sub> (1)	Ports 0, 1, 6, 7, 8	<ul style="list-style-type: none"> <li>•Output disable</li> <li>•Pull-up MOS Tr. OFF</li> <li>•VIN=VDD (including the off-leak current of the output Tr.)</li> </ul>	4.5 - 5.5			1	μA
	I <sub>IH</sub> (2)	<ul style="list-style-type: none"> <li>•<math>\overline{\text{RES}}</math></li> <li>•<math>\overline{\text{HS}}</math>, <math>\overline{\text{VS}}</math></li> </ul>	•VIN=VDD	4.5 - 5.5			1	
Low level input current	I <sub>IL</sub> (1)	Ports 0, 1, 6, 7, 8	<ul style="list-style-type: none"> <li>•Output disable</li> <li>•Pull-up MOS Tr. OFF</li> <li>•VIN=VSS (including the off-leak current of the output Tr.)</li> </ul>	4.5 - 5.5	-1			
	I <sub>IL</sub> (2)	<ul style="list-style-type: none"> <li>•<math>\overline{\text{RES}}</math></li> <li>•<math>\overline{\text{HS}}</math>, <math>\overline{\text{VS}}</math></li> </ul>	VIN=VSS	4.5 - 5.5	-1			
High level output voltage	V <sub>OH</sub> (1)	•CMOS output of ports 0, 1, 71 - 73, 84 - 87	I <sub>OH</sub> =-1.0mA	4.5 - 5.5	VDD-1			V
	V <sub>OH</sub> (2)	R, G, B, I, BL	I <sub>OH</sub> =-0.1mA	4.5 - 5.5	VDD-0.5			
Low level output voltage	V <sub>OL</sub> (1)	Ports 0, 1, 71 - 73, 84 - 87	I <sub>OL</sub> =10mA	4.5 - 5.5			1.5	
	V <sub>OL</sub> (2)	Ports 0, 1, 71 - 73, 84 - 87	I <sub>OL</sub> =1.6mA	4.5 - 5.5			0.4	
	V <sub>OL</sub> (3)	<ul style="list-style-type: none"> <li>•R, G, B, I, BL</li> <li>•Port 6</li> </ul>	I <sub>OL</sub> =3.0mA	4.5 - 5.5			0.4	
	V <sub>OL</sub> (4)	Port 6	I <sub>OL</sub> =6.0mA	4.5 - 5.5			0.6	
	V <sub>OL</sub> (5)	Port 70	I <sub>OL</sub> =1mA	4.5 - 5.5			0.4	
Pull-up MOS Tr. resistance	R <sub>pu</sub>	•Ports 0, 1, 7, 8	V <sub>OH</sub> =0.9VDD	4.5 - 5.5	13	38	80	kΩ
Bus terminal short circuit resistance (SCL0-SCL1, SDA0-SDA1)	R <sub>BS</sub>	<ul style="list-style-type: none"> <li>•P60-P62</li> <li>•P61-P63</li> </ul>		4.5 - 5.5			130	Ω
Hysteresis voltage	V <sub>HIS</sub>	<ul style="list-style-type: none"> <li>•Ports 0, 1, 6, 7</li> <li>•<math>\overline{\text{RES}}</math></li> <li>•<math>\overline{\text{HS}}</math>, <math>\overline{\text{VS}}</math></li> </ul>	Output disable	4.5 - 5.5		0.1VDD		V
Pin capacitance	C <sub>P</sub>	All pins	<ul style="list-style-type: none"> <li>•f=1MHz</li> <li>•Every other terminals are connected to VSS.</li> <li>•Ta=25°C</li> </ul>	4.5 - 5.5		10		pF

4. Serial Input/Output Characteristics at Ta= -10°C to +70°C, VSS=0V

Parameter		Symbol	Pins	Conditions	VDD[V]	Ratings			unit
						min.	typ.	max.	
Serial clock	Input clock	Cycle	tCKCY(1)	•SCK0 •SCLK0	Refer to figure 4.	4.5 - 5.5	2		tCYC
		Low Level pulse width	tCKL(1)				1		
		High Level pulse width	tCKH(1)				1		
	Output clock	Cycle	tCKCY(2)	•SCK0 •SCLK0	•Use pull-up resistor (1kΩ) when Nch open-drain output. •Refer to figure 4.	4.5 - 5.5	2		
		Low Level pulse width	tCKL(2)					1/2tCKCY	
		High Level pulse width	tCKH(2)					1/2tCKCY	
Serial input	Data set up time	tICK	SIO	•Data set-up to SCK0. •Data hold from SCK0. •Refer to figure 4.	4.5 - 5.5	0.1		μs	
	Data hold time	tCKI				0.1			
Serial output	Output delay time (Using external clock)	tCKO(1)	SO0	•Data hold from SCK0. •Use pull-up resistor (1kΩ) when Nch open-drain output. •Refer to figure 4.	4.5 - 5.5			7/12tCYC +0.2	
	Output delay time (Using internal clock)	tCKO(2)	SO0		4.5 - 5.5			1/3tCYC +0.2	

5. IIC Input/Output Conditions at Ta=-10°C to +70°C, VSS=0V

Parameter	Symbol	Standard		High speed		unit
		min.	max.	min.	max.	
SCL Frequency	fSCL	0	100	0	400	kHz
BUS free time between stop - start	tBUF	4.7	-	1.3	-	μs
HOLD time of start, restart condition	tHD;STA	4.0	-	0.6	-	μs
L time of SCL	tLOW	4.7	-	1.3	-	μs
H time of SCL	tHIGH	4.0	-	0.6	-	μs
Set-up time of restart condition	tSU;STA	4.7	-	0.6	-	μs
HOLD time of SDA	tHD;DAT	0	-	0	0.9	μs
Set-up time of SDA	tSU;DAT	250	-	100	-	ns
Rising time of SDA, SCL	tR	-	1000	20+0.1Cb	300	ns
Falling time of SDA, SCL	tF	-	300	20+0.1Cb	300	ns
Set-up time of stop condition	tSU;STO	4.0	-	0.6	-	μs

Refer to figure 9

(Note) Cb : Total capacitance of all BUS (unit : pF)

6. Pulse Input Conditions at Ta=-10°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				VDD[V]	min.	typ.	
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN	•Interrupt acceptable •Timer0-countable	4.5 - 5.5	1		tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (1/1 is selected for noise rejection clock.)	•Interrupt acceptable •Timer0-countable	4.5 - 5.5	2		
	tPIH(3) tPIL(3)	INT3/T0IN (1/16 is selected for noise rejection clock.)	•Interrupt acceptable •Timer0-countable	4.5 - 5.5	32		
	tPIH(4) tPIL(4)	INT3/T0IN (1/64 is selected for noise rejection clock.)	•Interrupt acceptable •Timer0-countable	4.5 - 5.5	128		
	tPIL(5)	$\overline{\text{RES}}$	Reset acceptable	4.5 - 5.5	200		μs
	tPIH(6) tPIL(6)	$\overline{\text{HS}}$ , $\overline{\text{VS}}$	•Display position controllable (Note) •The active edge of $\overline{\text{HS}}$ and $\overline{\text{VS}}$ must be apart at least 1 tCYC. •Refer to figure 6.	4.5 - 5.5	8		
Rising/falling time	tTHL tTLH	$\overline{\text{HS}}$	Refer to figure 6.	4.5 - 5.5			500 ns

7. AD Converter Characteristics at Ta=-10°C to + 70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				VDD[V]	min.	typ.	
Resolution	N			4.5 - 5.5		8	bit
Absolute precision	ET		(Note 3)			±1.5	LSB
Conversion time	tCAD		ADCR2=0 (Note 4)		16		tCYC
			ADCR2=1 (Note 4)		32		
Analog input voltage range	VAIN	AN3 - AN7			VSS	VDD	V
Analog port input current	IAINH		VAIN=VDD			1	μA
	IAINL		VAIN=VSS	-1			

(Note 3) Absolute precision does not include quantizing error (1/2LSB).

(Note 4) Conversion time is the time till the complete digital conversion value for analog input value is set to a register after the instruction to start conversion is sent.

## 8. Sample Current Dissipation Characteristics at Ta=-10°C to +70°C, VSS=0V

The sample current dissipation characteristics is the measurement result of Sanyo provided evaluation board when the recommended circuit parameters shown in the sample oscillation circuit characteristics are used externally. The currents through the output transistors and the pull-up MOS transistors are ignored.

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD[V]	min.	typ.		max.
Current dissipation during basic operation (Note 3)	IDDOP(1)	VDD	<ul style="list-style-type: none"> <li>•FmX'tal=32.768kHz X'tal oscillation</li> <li>•System clock : VCO</li> <li>•VCO for OSD operating</li> <li>•Internal RC oscillation stops</li> </ul>	4.5 - 5.5		17	30	mA
Current dissipation in HALT mode (Note 3)	IDDHALT(1)	VDD	<ul style="list-style-type: none"> <li>•HALT mode</li> <li>•FmX'tal=32.768kHz X'tal oscillation</li> <li>•System clock : VCO</li> <li>•VCO for OSD stops</li> <li>•Internal RC oscillation stops</li> </ul>	4.5 - 5.5		7	12	mA
	IDDHALT(2)	VDD	<ul style="list-style-type: none"> <li>•HALT mode</li> <li>•FmX'tal=32.768kHz X'tal oscillation</li> <li>•VCO for system stops</li> <li>•VCO for OSD stops</li> <li>•System clock : Internal RC</li> </ul>	4.5 - 5.5		300	1200	μA
	IDDHALT(3)	VDD	<ul style="list-style-type: none"> <li>•HALT mode</li> <li>•FmX'tal=32.768kHz X'tal oscillation</li> <li>•VCO for system stops</li> <li>•VCO for OSD stops</li> <li>•System clock : X'tal</li> </ul>	4.5 - 5.5		50	200	μA
Current dissipation in HOLD mode (Note 3)	IDDHOLD	VDD	<ul style="list-style-type: none"> <li>•HOLD mode</li> <li>•All oscillation stops.</li> </ul>	4.5 - 5.5		0.05	20	μA

(Note 3) The currents through the output transistors and the pull-up MOS transistors are ignored.

Recommended Oscillation Circuit and Sample Characteristics

The sample oscillation circuit characteristics in the table below is based on the following conditions:

- Recommended circuit parameters are verified by an oscillator manufacturer using a Sanyo provided oscillation evaluation board.
- Sample characteristics are the result of the evaluation with the recommended circuit parameters connected externally.

Recommended oscillation circuit and sample characteristics (Ta = -10 to +70°C)

Frequency	Manufacturer	Oscillator	Recommended circuit parameters				Operating supply voltage range	Oscillation stabilizing time		Notes
			C1	C2	Rf	Rd		typ.	max	
32.768kHz	Seiko Epson	C-002RX	18pF	18pF	Open	390kΩ	4.5 – 5.5V	1.00s	1.50s	

Notes The oscillation stabilizing time period is the time until the VCO oscillation for the internal system becomes stable after the following conditions. (Refer to Figure 2.)

1. The VDD becomes higher than the minimum operating voltage after the power is supplied.
2. The HOLD mode is released.

The sample oscillation circuit characteristics may differ applications. For further assistance, please contact with oscillator manufacturer with the following notes in your mind.

- Since the oscillation frequency precision is affected by wiring capacity of the application board, etc., adjust the oscillation frequency on the production board.
- The above oscillation frequency and the operating supply voltage range are based on the operating temperature of -10°C to +70°C. For the use with the temperature outside of the range herein, or in the applications requiring high reliability such as car products, please consult with oscillator manufacturer.
- When using the oscillator which is not shown in the sample oscillation circuit characteristics, please consult with Sanyo sales personnel.

Since the oscillation circuit characteristics are affected by the noise or wiring capacity because the circuit is designed with low gain in order to reduce the power dissipation, refer to the following notices.

- The distance between the clock I/O terminal (XT1 terminal XT2 terminal) and external parts should be as short as possible.
- The capacitors' VSS should be allocated close to the microcontroller's GND terminal and be away from other GND.
- The signal lines with rapid state changes or with large current should be allocated away from the oscillation circuit.

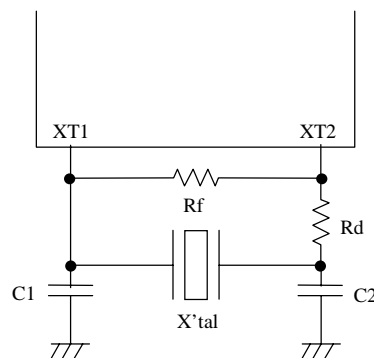


Figure 1 Recommended oscillation circuit.

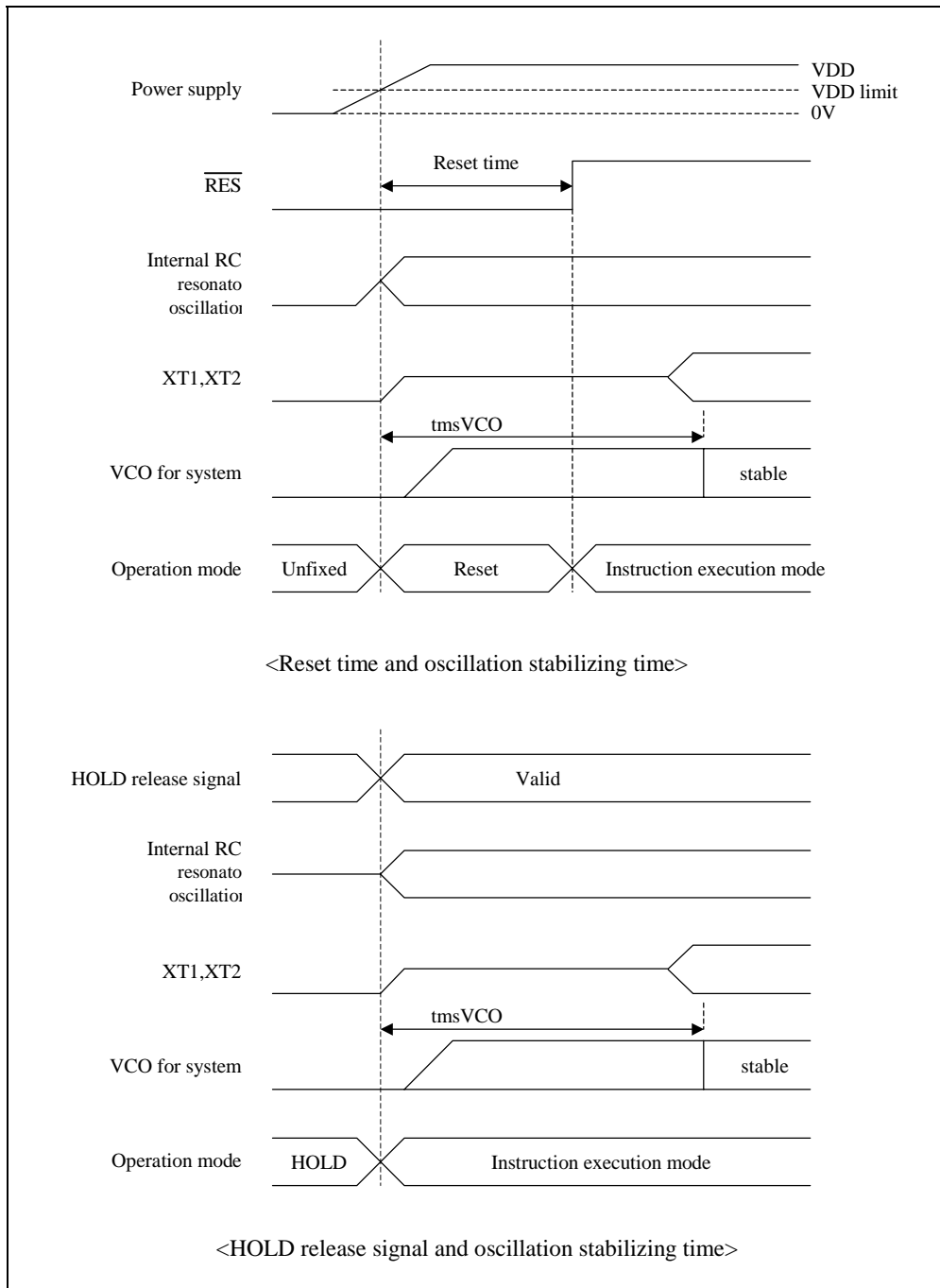
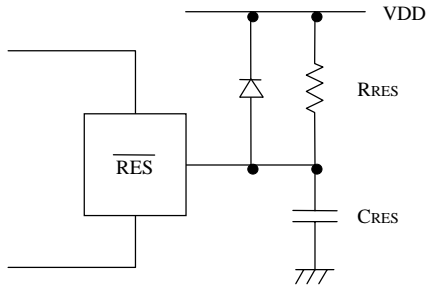


Figure 2 Oscillation stabilizing time



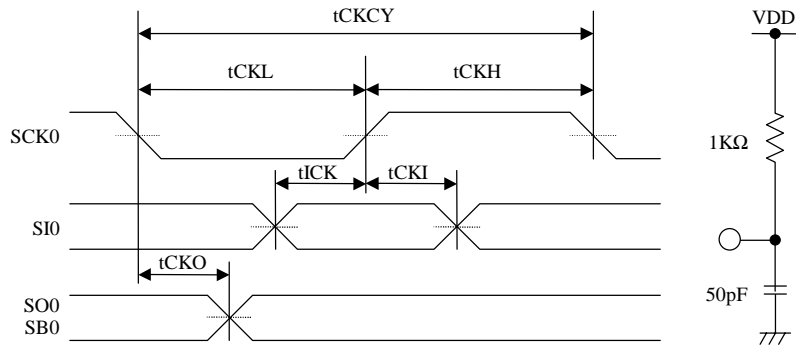


(Note) Determine the CRES, RRES value to generate more than 200μs reset time.

Figure 3 Reset circuit



< AC timing measurement point >



< Timing >

< Test load >

Figure 4 Serial input / output test condition

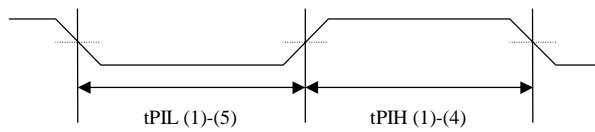


Figure 5 Pulse input timing condition - 1

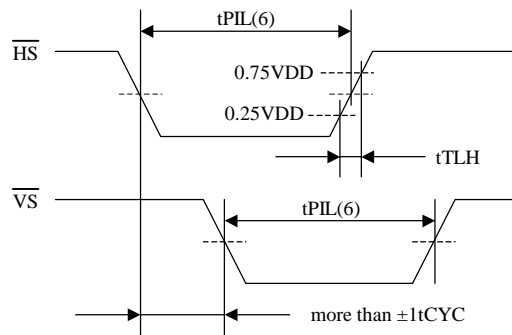


Figure 6 Pulse input timing condition - 2

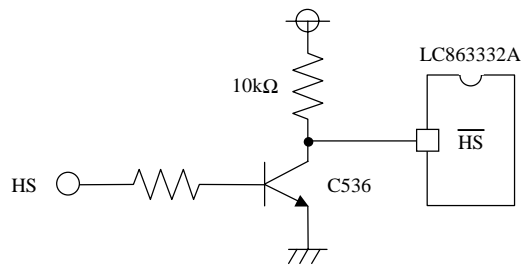


Figure 7 Recommended Interface circuit

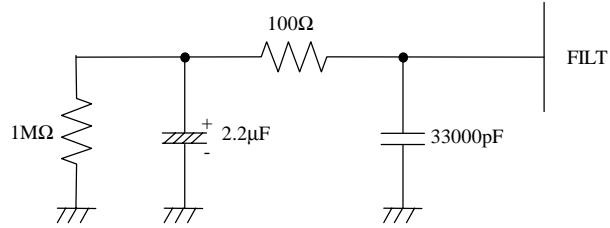
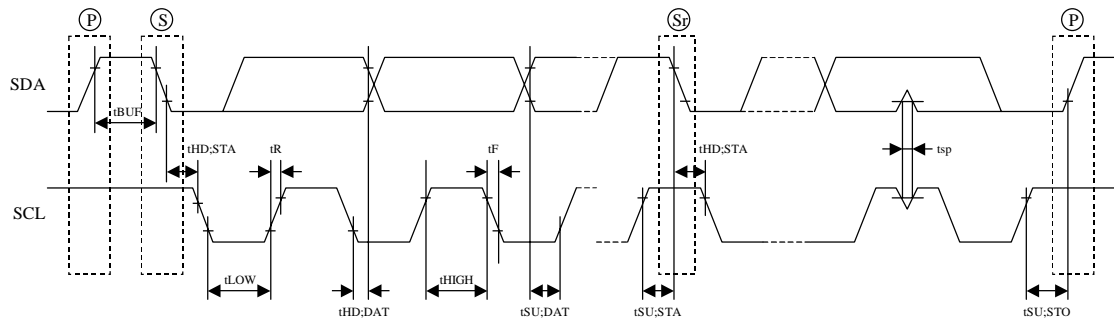


Figure 8 FILT recommended circuit

(Note) Place FILT parts on board as close to the microcontroller as possible.



S : start condition  
 P : stop condition  
 Sr : restart condition

tsp : Spike suppression

Standard mode : not exist  
 High speed mode : less than 50ns

Figure 9 IIC timing

memo:

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