CMOS LSI

LC72E32

Single Chip Microcontroller Plus PLL LSI with On-Chip UVEPROM

Preliminary

Overview

The LC72E32 microcontroller is an on-chip UVEPROM version of the LC7232N single-chip microcontroller plus PLL product. The LC72E32 has the same functions and pin assignment as the LC7232N mask ROM version. Its on-chip EPROM has an 8-Kbyte capacity and a 4-Kword by 16-bit organization. Since programs can be rewritten multiple times, the LC72E32 is optimal for program development.
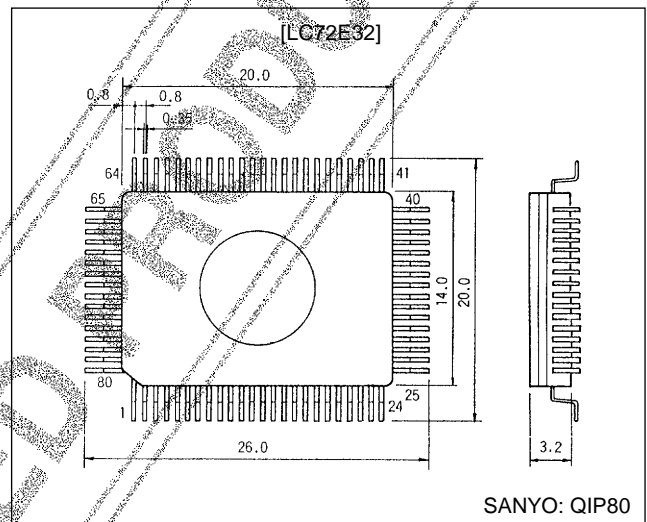
Features

- Options can be switched with EPROM data
  The LC7232N option functions can be specified with EPROM data. This allows the actual mass production printed circuit board to be used for test product evaluation.
- 8 Kbytes (with a 4-Kword by 16-bit organization) of UVEPROM on chip
  The LC72E32 includes 8 Kbytes of UVEPROM (ultraviolet erasable EPROM) on chip.
- The pin arrangement is identical to that of the LC7232N mask ROM version, i.e., pin compatibility is maintained.

Package Dimensions

unit: mm

3152A-QFP80

[LC72E32]

20.0

0.8

0.8

0.35

64

65

41

40

80

1

24

25

14.0

20.0

26.0

3.2

SANYO: QIP80

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Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +6.5	V
Input voltage	$V_{IN}1$	HOLD, INT, RES, ADI, SNS, and the G port	–0.3 to +13	V
	$V_{IN}2$	Inputs other than $V_{IN}1$	–0.3 to V_{DD} + 0.3	V
Output voltage	$V_{OUT}1$	H port	–0.3 to +15	V
	$V_{OUT}2$	Outputs other than $V_{OUT}1$	–0.3 to V_{DD} + 0.3	V
Output current	$I_{OUT}1$	All D and H port pins	0 to 5	mA
	$I_{OUT}2$	All E and F port pins	0 to 3	mA
	$I_{OUT}3$	All B and C port pins	0 to 1	mA
	$I_{OUT}4$	S1 to S28 and all I port pins	0 to 1	mA
Allowable power dissipation	Pd max	Topg = 10 to 40°C	400	mW
Operating temperature	Topr		10 to 40	°C
Storage temperature	Tstg		–45 to +125	°C

Note: There are circuits in this IC with reduced resistance to damage from static electricity. Thus special care is required when handling this product.

## Allowable Operating Ranges at Ta = 10 to 40°C, V_{DD} = 3.5 to 5.5 V

Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
Supply voltage	$V_{DD}1$	CPU and PLL operating	4.5		5.5	V
	$V_{DD}2$	CPU operating	3.5		5.5	V
	$V_{DD}3$	Memory retention voltage	1.3		5.5	V
Input high level voltage	$V_{IH}1$	G port	0.7 V_{DD}		8.0	V
	$V_{IH}2$	RES, INT, HOLD	0.8 V_{DD}		8.0	V
	$V_{IH}3$	SNS	2.5		8.0	V
	$V_{IH}4$	A port	0.6 V_{DD}		V_{DD}	V
	$V_{IH}5$	E and F ports	0.7 V_{DD}		V_{DD}	V
	$V_{IH}6$	LCTR (period measurement), $V_{DD}1$	0.8 V_{DD}		V_{DD}	V
Input low level voltage	$V_{IL}1$	G port	0		0.3 V_{DD}	V
	$V_{IL}2$	RES, INT	0		0.2 V_{DD}	V
	$V_{IL}3$	SNS	0		1.3	V
	$V_{IL}4$	A port	0		0.2 V_{DD}	V
	$V_{IL}5$	E and F ports	0		0.3 V_{DD}	V
	$V_{IL}6$	LCTR (period measurement), $V_{DD}1$	0		0.2 V_{DD}	V
	$V_{IL}7$	HOLD	0		0.4 V_{DD}	V
Input frequency	$f_{IN}1$	XIN	4.0	4.5	5.0	MHz
	$f_{IN}2$	FMIN, $V_{IN}2$, $V_{DD}1$	10		130	MHz
	$f_{IN}3$	FMIN, $V_{IN}3$, $V_{DD}1$	10		150	MHz
	$f_{IN}4$	AMIN (L), $V_{IN}4$, $V_{DD}1$	0.5		10	MHz
	$f_{IN}5$	AMIN (H), $V_{IN}5$, $V_{DD}1$	2.0		40	MHz
	$f_{IN}6$	HCTR, $V_{IN}6$, $V_{DD}1$	0.4		12	MHz
	$f_{IN}7$	LCTR (frequency), $V_{IN}7$, $V_{DD}1$	100		500	kHz
	$f_{IN}8$	LCTR (period), $V_{IH}6$, $V_{IL}6$, $V_{DD}1$	1		20×10^3	Hz
Input amplitude	$V_{IN}1$	XIN	0.50		1.5	Vrms
	$V_{IN}2$	FMIN	0.10		1.5	Vrms
	$V_{IN}3$	FMIN	0.15		1.5	Vrms
	$V_{IN}4, 5$	AMIN	0.10		1.5	Vrms
	$V_{IN}6, 7$	LCTR, HCTR	0.10		1.5	Vrms
Input voltage range	$V_{IN}8$	ADI	0		V_{DD}	V

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
Hysteresis	V_H	LCTR (period), RES, INT	$0.1\ V_{DD}$			V
Rejected pulse width	P_{REJ}	SNS			50	μs
Power-down detection voltage	V_{DET}		3.0	3.5	4.0	V
Input high level current	$I_{IH}1$	INT, HOLD, RES, ADI, SNS, and G port: $V_I = 5.5\ V$			3.0	μA
	$I_{IH}2$	A, E, and F ports: E and F ports with outputs off, A port with no R_{PD}, $V_I = V_{DD}$			3.0	μA
	$I_{IH}3$	XIN: $V_I = V_{DD} = 5.0\ V$	2.0	5.0	15	μA
	$I_{IH}4$	FMIN, AMIN, HCTR, LCTR: $V_I = V_{DD} = 5.0\ V$	4.0	10	30	μA
	$I_{IH}5$	A port: With an R_{PD}, $V_I = V_{DD} = 5.0\ V$		50		μA
Input low level current	$I_{IL}1$	INT, HOLD, RES, ADI, SNS, and G port: $V_I = V_{SS}$			3.0	μA
	$I_{IL}2$	A, E, and F ports: E and F ports with outputs off, A port with no R_{PD}, $V_I = V_{SS}$			3.0	μA
	$I_{IL}3$	XIN: $V_{IN} = V_{SS}$	2.0	5.0	15	μA
	$I_{IL}4$	FMIN, AMIN, HCTR, LCTR: $V_I = V_{SS}$	4.0	10	30	μA
Input floating voltage	V_{IF}	A port: With an R_{PD}			$0.05\ V_{DD}$	V
Pull-down resistance	R_{PD}	A port: With an R_{PD}, $V_{DD} = 5.0\ V$	75	100	200	kΩ
Output high level off leakage current	$I_{OFFH}1$	EO1, EO2: $V_O = V_{DD}$		0.01	10	nA
	$I_{OFFH}2$	B, C, D, E, F, and I ports: $V_O = V_{DD}$			3.0	μA
	$I_{OFFH}3$	H port: $V_O = 13\ V$			5.0	μA
Output low level off leakage current	$I_{OFFL}1$	EO1, EO2: $V_O = V_{SS}$		0.01	10	nA
	$I_{OFFL}2$	B, C, D, E, F, and I ports: $V_O = V_{DD}$			3.0	μA
Output high level voltage	$V_{OH}1$	B and C ports: $I_O = 1\ mA$	$V_{DD} - 2.0$	$V_{DD} - 1.0$	$V_{DD} - 0.5$	V
	$V_{OH}2$	E and F ports: $I_O = 1\ mA$	$V_{DD} - 1.0$			V
	$V_{OH}3$	EO1, EO2: $I_O = 500\ μA$	$V_{DD} - 1.0$			V
	$V_{OH}4$	XOUT: $I_O = 200\ μA$	$V_{DD} - 1.0$			V
	$V_{OH}5$	S1 to S28 and I port: $I_O = -0.1\ mA$	$V_{DD} - 1.0$			V
	$V_{OH}6$	D port: $I_O = 5\ mA$	$V_{DD} - 1.0$			V
	$V_{OH}7$	COM1 and COM2: $I_O = 25\ μA$	$V_{DD} - 0.75$	$V_{DD} - 0.5$	$V_{DD} - 0.3$	V
Output low level voltage	$V_{OL}1$	B and C ports: $I_O = 50\ μA$	0.5	1.0	2.0	V
	$V_{OL}2$	E and F ports: $I_O = 1\ mA$			1.0	V
	$V_{OL}3$	EO1, EO2: $I_O = 500\ μA$			1.0	V
	$V_{OL}4$	XOUT: $I_O = 200\ μA$			1.0	V
	$V_{OL}5$	S1 to S28 and I port: $I_O = 0.1\ mA$			1.0	V
	$V_{OL}6$	D port: $I_O = 5\ mA$			1.0	V
	$V_{OL}7$	COM1, COM2: $I_O = 25\ μA$	0.3	0.5	0.75	V
	$V_{OL}8$	H port: $I_O = 5\ mA$	(150 Ω) 0.75		(400 Ω) 2.0	V
Output middle level voltage	V_M1	COM1, COM2: $V_{DD} = 5.0\ V$, $I_O = 20\ μA$	2.0	2.5	3.0	V
A/D conversion error		ADI: $V_{DD}1$	$-1/2$		$1/2$	LSB
Current drain	$I_{DD}1$	$V_{DD}1$, $f_{IN}2 = 130\ MHz$		15	20	mA
	$I_{DD}2$	$V_{DD} = 5.0\ V$, PLL stopped, CT = 2.67 μs (HOLD mode, Figure 1)		2.7		mA
	$I_{DD}3$	$V_{DD} = 5.0\ V$, PLL stopped, CT = 13.33 μs (HOLD mode, Figure 1)		1.7		mA
	$I_{DD}4$	$V_{DD} = 5.0\ V$, PLL stopped, CT = 40.00 μs (HOLD mode, Figure 1)		1.5		mA
	$I_{DD}5$	$V_{DD} = 5.5\ V$, oscillator stopped, Ta = 25°C (BACK UP mode, Figure 2)			5	μA
		$V_{DD} = 2.5\ V$, oscillator stopped, Ta = 25°C (BACK UP mode, Figure 2)			1	μA

Test Circuits
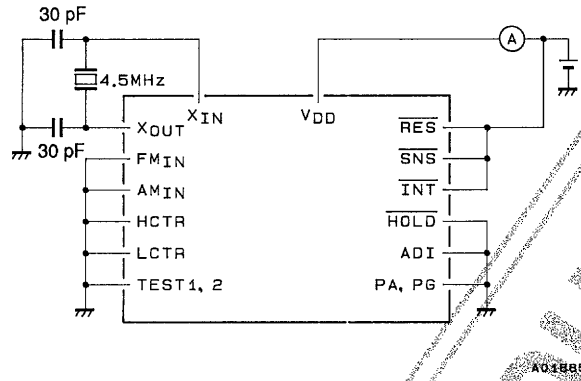
Note: PB to PF, PH, and PI are all open. However, PE and PF are output-selected.

Figure 1 $I_{DD}2$ to $I_{DD}4$ in HOLD Mode
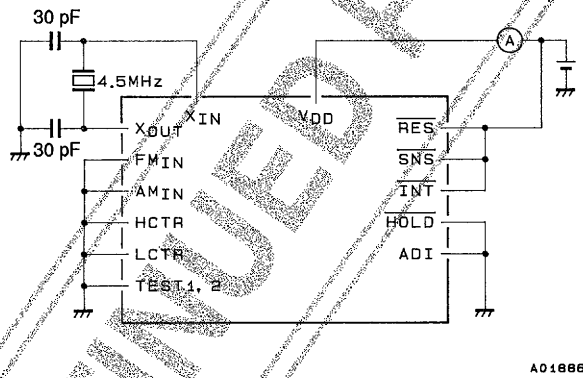
Note: PA to PI, S1 to S24, COM1, and COM2 are all open.

Figure 2 $I_{DD}5$ in BACK UP Mode
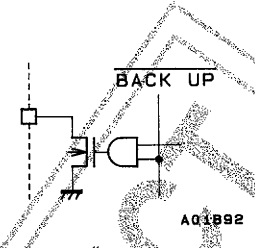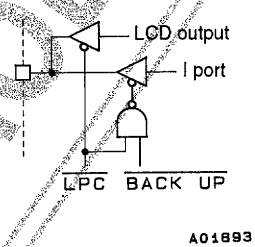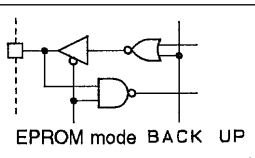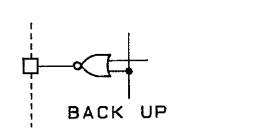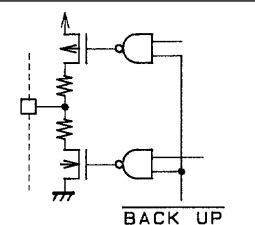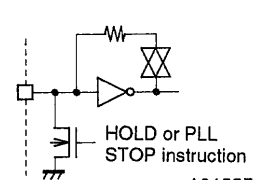
Pin Functions

Pin	Pin No.	Function	I/O	I/O circuit type	EPROM mode function
PA0 PA1 PA2 PA3	35 34 33 32	Low threshold type dedicated input port These pins can be used, for example, for key data acquisition. Built-in pull-down resistors can be specified as an option. This option is in 4-pin units, and cannot be specified for individual pins. Input through these pins is disabled in BACKUP mode.	Input	BACK UP Option A01887	
PB0 PB1 PB2 PB3 PC0 PC1 PC2 PC3	30 29 28 27 26 25 24 23	Dedicated output ports Since the output transistor impedances are unbalanced CMOS, these pins can be effectively used for functions such as key scan timing. These pins go to the output high impedance state in BACKUP mode. These pins go to the low level during a reset, i.e., when the RES pin is low.	Output	BACK UP A01888	
PD0 PD1 PD2 PD3	22 21 20 19	Dedicated output port These are normal CMOS outputs. These pins go to the output high impedance state in BACKUP mode. These pins go to the low level during a reset, i.e., when the RES pin is low.			
PE0 PE1 PE2 PE3	18 17 16 15	I/O port These pins are switched between input and output as follows. Once an input instruction (IN, TPT, or TPF) is executed, these pins latch in the input mode. Once an output instruction (OUT, SPB, or RPB) is executed, they latch in the output mode. These pins go to the input mode during a reset, i.e., when the RES pin is low. In BACKUP mode these pins go to the input mode with input disabled.	I/O	BACK UP EPROM mode A01889	Data I/O PE0: D0 PE1: D1 PE2: D2 PE3: D3 PF0: D4 PF1: D5 PF2: D6 PF3: D7
PF0 PF1 PF2 PF3	14 13 12 11	I/O port These pins are switched between input and output by the FPC instruction. The I/O states of this port can be specified for individual pins. These pins go to the input mode during a reset, i.e., when the RES pin is low. In BACKUP mode these pins go to the input mode with input disabled.			
PG0 PG1	6 5		Input	BACK UP EPROM mode A01890	EPROM control signal inputs PG0: CE PG1: OE
PG2 PG3	4 3	Dedicated input port Input through these pins is disabled in BACKUP mode.		BACK UP A01891	
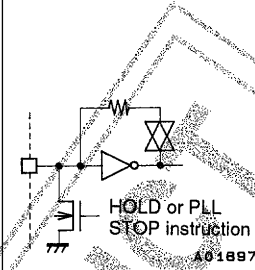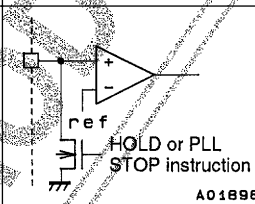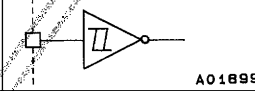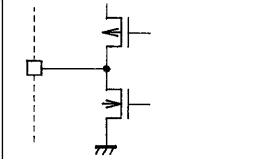
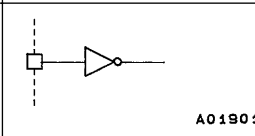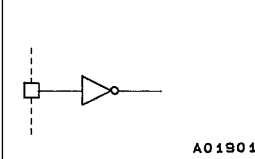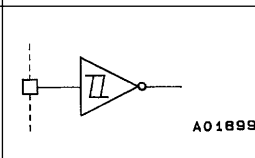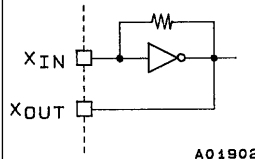Continued from preceding page.

Pin	Pin No.	Function	I/O	I/O circuit type	EPROM mode function
PH0 PH1 PH2 PH3	10 9 8 7	Dedicated output port Since these pins are high breakdown voltage n-channel transistor open-drain outputs, they can be effectively used for functions such as band power supply switching. Note that PH2 and PH3 also function as the DAC1 and DAC2 outputs. These pins go to the high impedance state during a reset, i.e., when the RES pin is low, and in BACKUP mode.	Output	BACK UP A01892	
PI0/S25 PI1/S26 PI2/S27 PI3/S28	39 38 37 36	Dedicated output port While these pins have a CMOS output circuit structure, they can be switched to function as LCD drivers. Their function is switched by the SS and RS instructions. These pins cannot be switched individually. The LCD driver function is selected and a segment off signal is output when power is first applied or when RES is low. These pins are held at the low level in BACKUP mode. Note that when the general-purpose port use option is specified, these pins output the contents of IPORT when LPC is 1, and the contents of the general-purpose output port LATCH when LPC is 0.	Output	LCD output I port LPC BACK UP A01893	
S1 to S14	63 to 50	LCD driver segment outputs A frame frequency of 100 Hz and a 1/2 duty, 1/2 bias drive type are used. A segment off signal is output when power is first applied or when RES is low. These pins are held at the low level in BACKUP mode. The use of these pins as general-purpose output ports can be specified as an option.	I/O	EPROM mode BACK UP A01894	Address input S1: A0 to S14: A13
S15 to S24	49 to 40		Output	BACK UP A01895	
COM1 COM2	65 64	LCD driver common outputs A 1/2 duty, 1/2 bias drive type is used. The output when power is first applied or when RES is low is identical to the normal operating mode output. These pins are held at the low level in BACKUP mode.	Output	BACK UP A01896	
FMIN	74	FM VCO (local oscillator) input The input must be capacitor-coupled. The input frequency range is from 10 to 130 MHz.	Input	HOLD or PLL STOP instruction A01897	
AMIN	75	AM VCO (local oscillator) input The band supported by this pin can be selected using the PLL instruction. High (2 to 40 MHz) → SW Low (0.5 to 10 MHz) → LW and MW			

Continued from preceding page.

Pin	Pin No.	Function	I/O	I/O circuit type	EPROM mode function
HCTR	70	Universal counter input The input should be capacitor-coupled. The input frequency range is from 0.4 to 12 MHz. This input can be effectively used for FM IF or AM IF counting.	Input	A01897	
LCTR	71	Universal counter input The input should be capacitor-coupled for input frequencies in the range 100 to 150 kHz. Capacitor coupling is not required for input frequencies from 1 to 20 Hz. This input can be effectively used for AM IF counting.			
ADI	69	A/D converter input A 1.28 ms period is required for a 6-bit sequential comparison conversion. The full scale input is $((63/96) \cdot V_{DD})$ for a data value of 3FH.	Input	A01898	
INT	66	Interrupt request input An interrupt is generated when the INTEN flag is set (by an SS instruction) and a falling edge is input.	Input	A01899	
EO1 EO2	77 78	Reference frequency and programmable divisor phase comparison error outputs Charge pump circuits are built in. EO1 and EO2 are the same.	Output	A01900	
SNS	72	Input pin used to determine if a power outage has occurred in BACKUP mode This pin can also be used as a normal input port.	Input	A01901	
HOLD	67	Input pin used to force the LC72E32 to HOLD mode The LC72E32 goes to HOLD mode when the HOLDEN flag is set (by an SS instruction) and the HOLD input goes low. A high breakdown voltage circuit is used so that this input can be used in conjunction with the normal power switch.	Input	A01901	
RES	68	System reset input This signal should be held low for 75 ms after power is first applied to effect a power-up reset. The reset starts when a low level has been input for at least six reference clock cycles.	Input	A01899	
XIN XOUT	1 80	Crystal oscillator connections (4.5 MHz) A feedback resistor is built in.	Input Output	A01902	
TEST1 TEST2	79 2	LSI test pins. These pins must be connected to V_{SS}.			
V_{DD}	31, 73	Power supply + connections. Both pins must be connected.			EPROM write power Vpp
V_{SS}	76	Power supply – connection.			

Option

No.	Description	Selections
1	WDT (watchdog timer) inclusion selection	WDT included
		No WDT
2	Port A pull-down resistor inclusion selection	Pull-down resistors included
		No pull-down resistors
3	Cycle time selection	2.67 µs
		13.33 µs
		40.00 µs
4	LCD port/general-purpose port selection	LCD ports
		General-purpose output ports

Usage Notes

The LC72E32 is provided for development of LC7232N application programs and for LC7232N function evaluation. The points listed below required attention when using the LC72E32.

1. Differences between the LC72E32 and the LC7232N

Item		LC72E32	LC7232N
Operating temperature (Topr)		10 to 40 °C	−40 to +85℃
Operation immediately following power on		After the 75 ms power on reset period, the LSI internal option settings are set up during a period of about 1 ms. After that operation completes, program execution starts with the program counter set to location 0.	After the 75 ms power on reset period, program execution starts with the program counter set to location 0.
Input type of the A port immediately following power on*		No pull-down resistors	Pull-down resistors are included or not according to the option specifications.
Output type of the S1 to S28 outputs immediately following power on*		LCD ports	These pins function as either LCD ports or general-purpose output ports according to the option specifications.
Power-down detection voltage (V_{DET})		Minimum: 3.0 V Typical: 3.5 V Maximum: 4.0 V	Minimum: 2.7 V Typical: 3.0 V Maximum: 3.3 V
Current drain	$I_{DD}2$	Conditions: V_{DD} = 5.0 V, PLL stopped CT = 2.67 µs (HOLD mode, Figure 1) Typical: 2.7 mA	Conditions: $V_{DD}2$, PLL stopped CT = 2.67 µs (HOLD mode, Figure 1) Typical: 1.5 mA
	$I_{DD}3$	Conditions: V_{DD} = 5.0 V, PLL stopped CT = 13.33 µs (HOLD mode, Figure 1) Typical: 1.7 mA	Conditions: $V_{DD}2$, PLL stopped CT = 13.33 µs (HOLD mode, Figure 1) Typical: 1.0 mA
	$I_{DD}4$	Conditions: V_{DD} = 5.0 V, PLL stopped CT = 40.00 µs (HOLD mode, Figure 1) Typical: 1.5 mA	Conditions: $V_{DD}2$, PLL stopped CT = 40.00 µs (HOLD mode, Figure 1) Typical: 0.7 mA
The TEST1 and TEST2 pins		These are LSI test pins and must be connected to V_{SS}.	These are LSI test pins and must be either left open or connected to V_{SS}.

Note: * This refers to the option setup time of about 1 ms that occurs following the period of about 75 ms from power application.

2. PLA and options

   The LC72E32 uses location 2000H to 201FH as program memory for PLA pattern specification, and locations 2020H to 2033H for option specification. This option specification allows the LC72E32 to support option setups identical to those available with the LC7232N.

LC72E32 Option Types

Symbol	Option Type	Selections
WDT	WDT (watchdog timer) inclusion selection	WDT included
		No WDT
APPDN	A port pull-down resistor inclusion selection	Pull-down resistors included
		No pull-down resistors
CTIM	Cycle time selection	2.67 µs
		13.33 µs
		40.00 µs
LCDP	LCD port/general-purpose port selection	LCD ports
		General-purpose output ports

Note that these options are not determined until the option setting period of about 1 ms, which follows a period of about 75 ms from power application, has passed.

3. Use of the mass produced unit printed circuit board

When using the printed circuit board for the massed produced end product with the LC72E32, be sure to connect the TEST1 and TEST2 pins to V_{SS} and be sure to connect both pins 31 and 73 (the V_{DD} pins) to the plus side of the power supply.

4. EPROM address space

2033H	All locations set to 00H	Option specification area
2024H		
2023H	LCDP	
2022H	CTIM	
2021H	APPDN	
2020H	WDT	
201FH	PLA2	PLA specification area
2010H		
200FH	PLA1	
2000H		
1FFFH	Program area 8 Kbytes (4 Kwords by 16 bits)	
0000H		

Note: Due to their structure, on-chip EPROM microcontrollers (products in which the EPROM has not been written) cannot be fully tested prior to shipment. As a result, the yield after writing may be decreased.

Usage Techniques

1. Writing the on-chip EPROM

   There are two techniques that can be used to write to the LC72E32's on-chip EPROM.

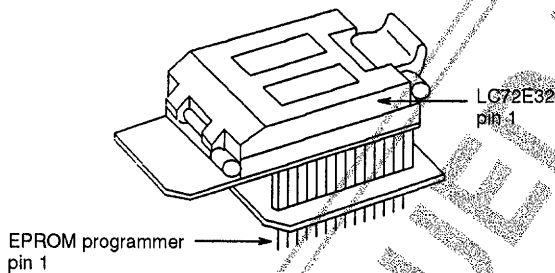   • Use of a general-purpose EPROM programmer

     The LC72E32's EPROM can be written using a general-purpose EPROM programmer. This requires the use of a special-purpose adapter, the LC72E32 Adapter for EPROM Programmer. Use the Intel 27512 (Vpp = 12.5 V) high-speed writing technique, and specify the address settings as locations 0 to 2033H.

   • Use of the RE32 in-circuit emulator

     The LC72E32's EPROM can be written using the RE32 in-circuit emulator. This requires the use of a special-purpose adapter, the LC72E32 Adapter for RE32. Use the PGOTP command as the writing technique.

2. Special-purpose EPROM writing adapters

   As mentioned above, there are two EPROM writing techniques, each of which requires the use of the appropriate adapter.

   Note: The external dimensions of these two adapters are essentially identical.

   General-purpose EPROM programmer adapter:
       Product name: LC72E32 Adapter for EPROM Programmer
       Product code: NDK-DC-001-A
   RE32 in-circuit emulator adapter:
       Product name: LC72E32 Adapter for RE32
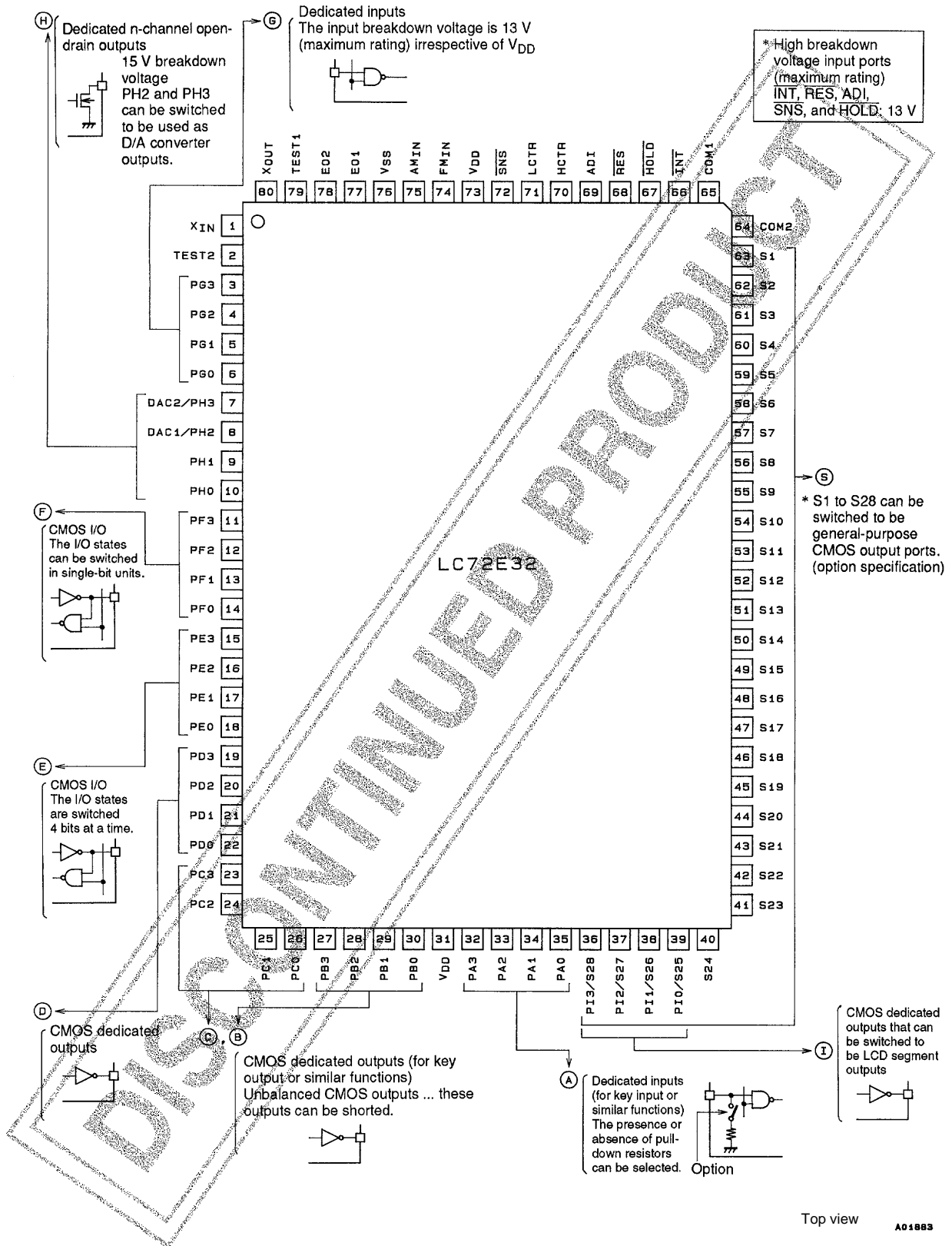   Product code: NDK-DC-003-A

   • Erasure

     Use a general-purpose EPROM eraser to erase written data.

   • Light Seal

     The LC72E32 includes UVEPROM, i.e., ultraviolet erasable EPROM. When actually using an LC72E32, its window should be covered with UV-opaque tape.
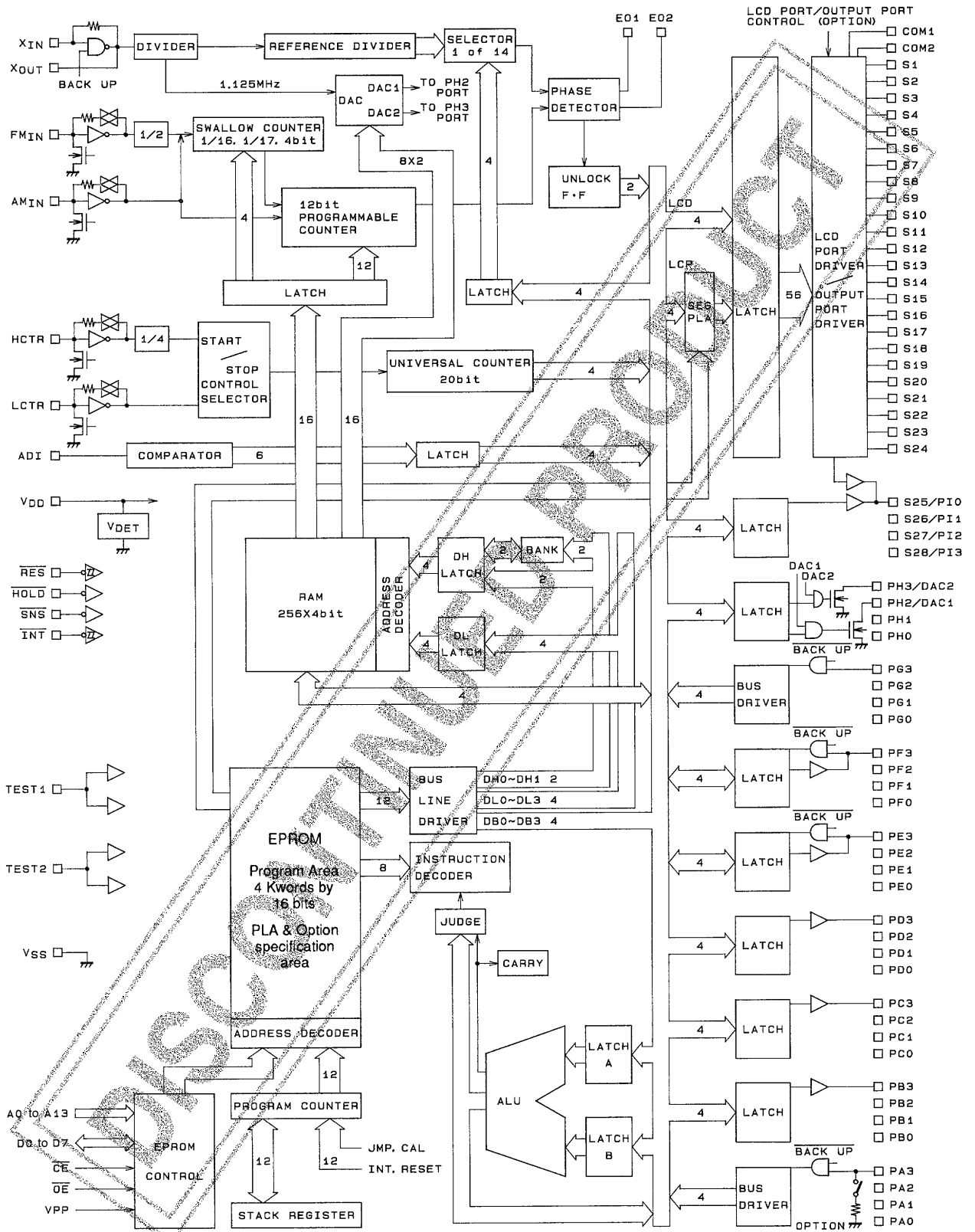
Pin Assignment

Top view   A01883

Block Diagram

LC72E32 Instruction Table

Abbreviations:

ADDR: Program memory address [12 bits]
b: Borrow
B: Bank number [2 bits]
C: Carry
DH: Data memory address high (row address) [2 bits]
DL: Data memory address low (column address) [4 bits]
I: Immediate data [4 bits]
M: Data memory address
N: Bit position [4 bits]
Pn: Port number [4 bits]
r: General register (one of the locations 00 to 0FH in bank 0)
Rn: Register number [4 bits]
( ):   Contents of register or memory
( )n: Contents of bit N of register or memory

Instruction Group	Mnemonic	Operand		Function	Operation	Machine code									
		1st	2nd			D15	14	13	12	11	10	9 8	7 6 5 4	3 2 1 D0	
Addition instructions	AD	r	M	Add M to r	$r \leftarrow (r) + (M)$	0	1	0	0	0	0	DH	DL	Rn	
	ADS	r	M	Add M to r, then skip if carry	$r \leftarrow (r) + (M)$ skip if carry	0	1	0	0	0	1	DH	DL	Rn	
	AC	r	M	Add M to r with carry	$r \leftarrow (r) + (M) + C$	0	1	0	0	1	0	DH	DL	Rn	
	ACS	r	M	Add M to r with carry, then skip if carry	$r \leftarrow (r) + (M) + C$ skip if carry	0	1	0	0	1	1	DH	DL	Rn	
	AI	M	I	Add I to M	$M \leftarrow (M) + I$	0	1	0	1	0	0	DH	DL	I	
	AIS	M	I	Add I to M, then skip if carry	$M \leftarrow (M) + I$ skip if carry	0	1	0	1	0	1	DH	DL	I	
	AIC	M	I	Add I to M with carry	$M \leftarrow (M) + I + C$	0	1	0	1	1	0	DH	DL	I	
	AICS	M	I	Add I to M with carry, then skip if carry	$M \leftarrow (M) + I + C$ skip if carry	0	1	0	1	1	1	DH	DL	I	
Subtraction instructions	SU	r	M	Subtract M from r	$r \leftarrow (r) - (M)$	0	1	1	0	0	0	DH	DL	Rn	
	SUS	r	M	Subtract M from r, then skip if borrow	$r \leftarrow (r) - (M)$ skip if borrow	0	1	1	0	0	1	DH	DL	Rn	
	SB	r	M	Subtract M from r with borrow	$r \leftarrow (r) - (M) - b$	0	1	1	0	1	0	DH	DL	Rn	
	SBS	r	M	Subtract M from r with borrow, then skip if borrow	$r \leftarrow (r) - (M) - b$ skip if borrow	0	1	1	0	1	1	DH	DL	Rn	
	SI	M	I	Subtract I from M	$M \leftarrow (M) - I$	0	1	1	1	0	0	DH	DL	I	
	SIS	M	I	Subtract I from M, then skip if borrow	$M \leftarrow (M) - I$ skip if borrow	0	1	1	1	0	1	DH	DL	I	
	SIB	M	I	Subtract I from M with borrow	$M \leftarrow (M) - I - b$	0	1	1	1	1	0	DH	DL	I	
	SIBS	M	I	Subtract I from M with borrow, then skip if borrow	$M \leftarrow (M) - I - b$ skip if borrow	0	1	1	1	1	1	DH	DL	I	
Comparison instructions	SEQ	r	M	Skip if r equals M	$r - M$ skip if zero	0	0	0	0	0	1	DH	DL	Rn	
	SGE	r	M	Skip if r is greater than or equal to M	$r - M$ skip if not borrow $(r) \geq (M)$	0	0	0	0	1	1	DH	DL	Rn	
	SEQI	M	I	Skip if M equal to I	$M - I$ skip if zero	0	0	1	1	0	1	DH	DL	I	
	SGEI	M	I	Skip if M is greater than or equal to I	$M - I$ skip if not borrow $(M) \geq I$	0	0	1	1	1	1	DH	DL	I	

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Instruction Group	Mnemonic	Operand 1st	Operand 2nd	Function	Operation	Machine code D15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 D0
Logical operation instructions	AND	M	I	AND I with M	M ← (M) ∧ I	0 0 1 1	0 0 DH	DL	I
	OR	M	I	OR I with M	M ← (M) ∨ I	0 0 1 1	1 0 DH	DL	I
	EXL	r	M	Exclusive OR M with r	r ← (r) ⊕ (M)	0 0 1 0	0 0 DH	DL	Rn
Transfer instructions	LD	r	M	Load M to r	r ← (M)	1 0 0 0	0 0 DH	DL	Rn
	ST	M	r	Store r to M	M ← (r)	1 0 0 0	0 1 DH	DL	Rn
	MVRD	r	M	Move M to destination M referring to r in the same row	[DH, Rn] ← (M)	1 0 0 0	1 0 DH	DL	Rn
	MVRS	M	r	Move source M referring to r to M in the same row	M ← [DH, Rn]	1 0 0 0	1 1 DH	DL	Rn
	MVSR	M1	M2	Move M to M in the same row	[DH, DL1] ← [DH, DL2]	1 0 0 1	0 0 DH	DL1	DL2
	MVI	M	I	Move I to M	M ← I	1 0 0 1	0 1 DH	DL	I
	PLL	M	r	Load M to PLL registers	PLL r ← PLL DATA	1 0 0 1	1 0 DH	DL	Rn
Bit test instructions	TMT	M	N	Test M bits, then skip if all bits specified are true	if M (N) = all 1s, then skip	1 0 1 0	0 1 DH	DL	N
	TMF	M	N	Test M bits, then skip if all bits specified are false	if M (N) = all 0s, then skip	1 0 1 0	1 1 DH	DL	N
Jump and subroutine call instructions	JMP	ADDR		Jump to the address	PC ← ADDR	1 0 1 1	ADDR (12 bits)		
	CAL	ADDR		Call subroutine	PC ← ADDR Stack ← (PC) + 1	1 1 0 0	ADDR (12 bits)		
	RT			Return from subroutine	PC ← Stack	1 1 0 1	0 1 0 0	0 0 0 0	0 0 0 0
	RTI			Return from interrupt	PC ← Stack	1 1 0 1	0 1 0 1	0 0 0 0	0 0 0 0
F/F test instructions	TTM	N		Test timer F/F then skip if it has not been set	if timer F/F = 0, then skip	1 1 0 1	0 1 1 0	0 0 0 0	N
	TUL	N		Test unlock F/F then skip if it has not been set	if UL F/F = 0, then skip	1 1 0 1	0 1 1 1	0 0 0 0	N
Status register instructions	SS	N		Set status register	(Status register 1) N ← 1	1 1 0 1	1 1 0 0	0 0 0 0	N
	RS	N		Reset status register	(Status register 1) N ← 0	1 1 0 1	1 1 0 1	0 0 0 0	N
	TST	N		Test status register true	if (Status register 2) N = all 1s, then skip	1 1 0 1	1 1 1 0	0 0 0 0	N
	TSF	N		Test status register false	if (Status register 2) N = all 0s, then skip	1 1 0 1	1 1 1 1	0 0 0 0	N
Bank switching instructions	BANK	B		Select bank	BANK ← B	1 1 0 1	0 0 B	0 0 0 0	0 0 0 0

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Instruction Group	Mnemonic	Operand 1st	Operand 2nd	Function	Operation	Machine code D15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 D0
I/O instruction Group	LCD	M	I	Output segment pattern to LCD digit direct	LCD (DIGIT) ← M	1 1 1 0	0 0 DH	DL	DIGIT
	LCP	M	I	Output segment pattern to LCD digit through PLA	LCD (DIGIT) ← PLA ← M	1 1 1 0	0 1 DH	DL	DIGIT
	IN	M	P	Input port data to M	M ← (Port (P))	1 1 1 0	1 0 DH	DL	P
	OUT	M	P	Output contents of M to port	(Port (P)) ← M	1 1 1 0	1 1 DH	DL	P
	SPB	P	N	Set port bits	(Port (P)) N ← 1	1 1 1 1	0 0 0 0	P	N
	RPB	P	N	Reset port bits	(Port (P)) N ← 0	1 1 1 1	0 1 0 1	P	N
	TPT	P	N	Test port bits, then skip if all bits specified are true	if (Port (P)) N = all 1s, then skip	1 1 1 1	0 1 0	P	N
	TPF	P	N	Test port bits, then skip if all bits specified are false	if (Port (P)) N = all 0s, then skip	1 1 1 1	1 1 1	P	N
Universal counter instructions	UCS	I		Set I to UCCW1	UCCW1 ← I	0 0 0 0	0 0 0 1	0 0 0 0	I
	UCC	I		Set I to UCCW2	UCCW2 ← I	0 0 0 0	0 0 1 1	0 0 0 0	I
Other instructions	FPC	N		F port I/O control	FPC latch ← N	0 0 0 1	0 0 0 0	0 0 0 0	N
	CKSTP			Clock stop	Stop clock if HOLD = 0	0 0 0 1	0 0 0 1	0 0 0 0	0 0 0 0
	DAC	I		Load M to D/A registers	DAreg ← DAC DATA	0 0 0 0	0 0 1 0	0 0 0 0	I
	NOP			No operation		0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

This catalog provides information as of September, 1998. Specifications and information herein are subject to change without notice.