

**SANYO**

No. 4916A

**LC35256A, AS, AM, AT-70/85/10****256K (32768 words × 8 bits) SRAM with  $\overline{OE}$   
and  $\overline{CE}$  Control Pins**

## Overview

The LC35256A, AS, AM, and AT are 32768 words × 8-bits asynchronous silicon gate CMOS SRAMs. These products feature a 6-transistor full-CMOS memory cell, low voltage operation, a low operating current, and an ultra-low standby current.

The LC35256A series product control signal inputs include both an  $\overline{OE}$  pin for high-speed access and a chip enable ( $\overline{CE}$ ) pin device selection; thus the LC35256A series products allow easy memory expansion and are optimal for systems that require low power battery backup.

The ultra low standby current allows capacitor backup to be used.

The 3 volt operation means that the LC35256A series is optimal for use in portable battery-operated systems.

## Features

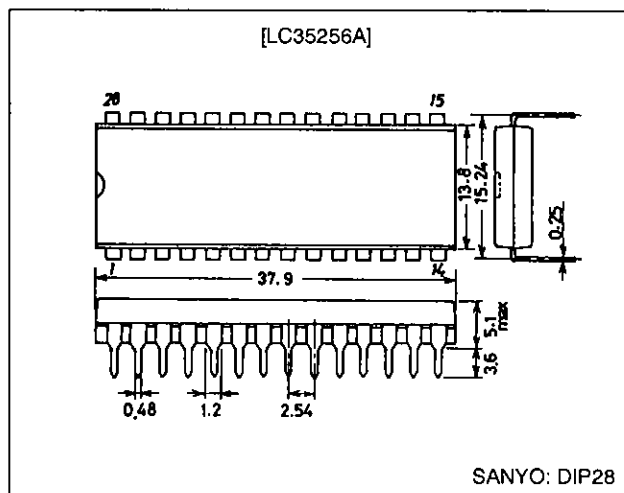
- Supply voltage range: 2.7 to 5.5 V
  - 5 V operation: 5.0 V ±10%
  - 3 V operation: 2.7 to 3.6 V
- Access times
  - 5 V operation
    - LC35256A, AS, AM, AT-70: 70 ns (max.)
    - LC35256A, AS, AM, AT-85: 85 ns (max.)
    - LC35256A, AS, AM, AT-10: 100 ns (max.)
  - 3 V operation
    - LC35256A, AS, AM, AT-70: 200 ns (max.)
    - LC35256A, AS, AM, AT-85: 250 ns (max.)
    - LC35256A, AS, AM, AT-10: 500 ns (max.)
- Standby current
  - 5 V operation: 1.0 μA ( $T_a \leq 60^\circ\text{C}$ ), 5.0 μA ( $T_a \leq 85^\circ\text{C}$ )
  - 3 V operation: 0.8 μA ( $T_a \leq 60^\circ\text{C}$ ), 4.0 μA ( $T_a \leq 85^\circ\text{C}$ )
- Operating temperature range: -40 to +85°C
- Data retention supply voltage: 2.0 to 5.5 V
- Input levels
  - 5 V operation: TTL compatible
  - 3 V operation:  $V_{CC} - 0.2 \text{ V}/0.2 \text{ V}$
- 28-pin DIP (600 mil) plastic package: LC35256A Series
- 28-pin DIP (300 mil) plastic package: LC35256AS Series
- 28-pin SOP (450 mil) plastic package: LC35256AM Series

- 28-pin TSOP ( $8 \times 13.4\text{mm}$ ) plastic package: LC35256AT
- Shared I/O pins, three-state outputs
- No clock required (completely static circuit)

## Package Dimensions

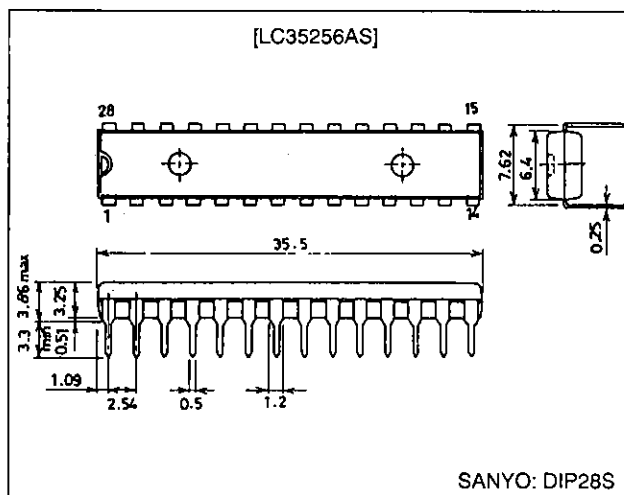
unit: mm

### 3012A-DIP28



unit: mm

### 3133-DIP28S

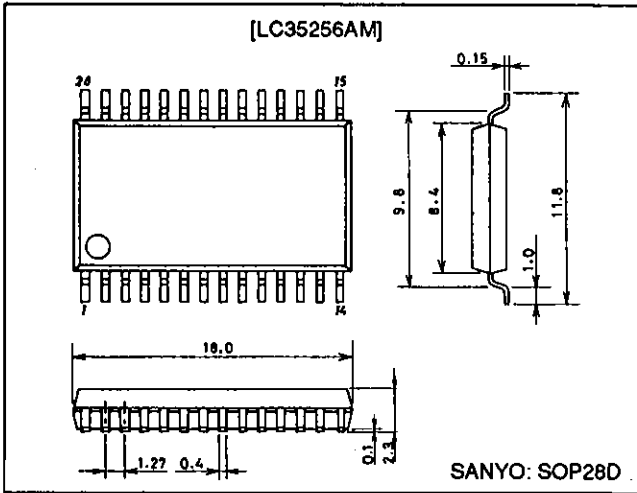
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LC35256A, AS, AM, AT-70/85/10

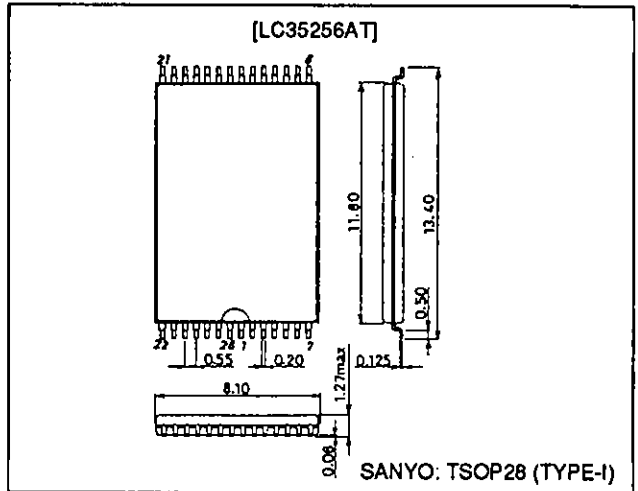
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3187-SOP28D

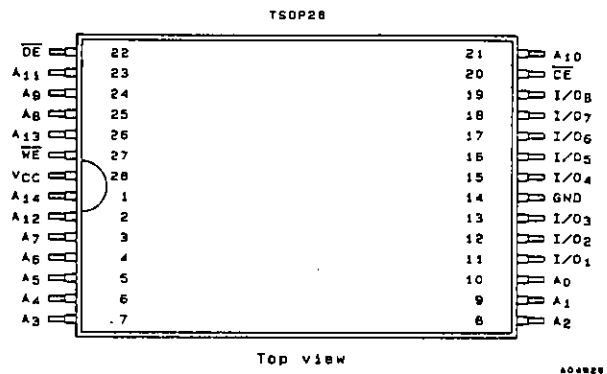
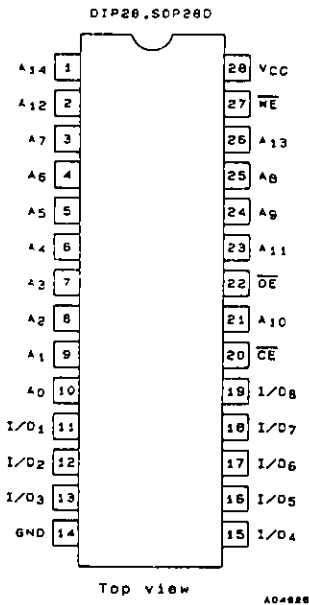


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3221-TSOP28



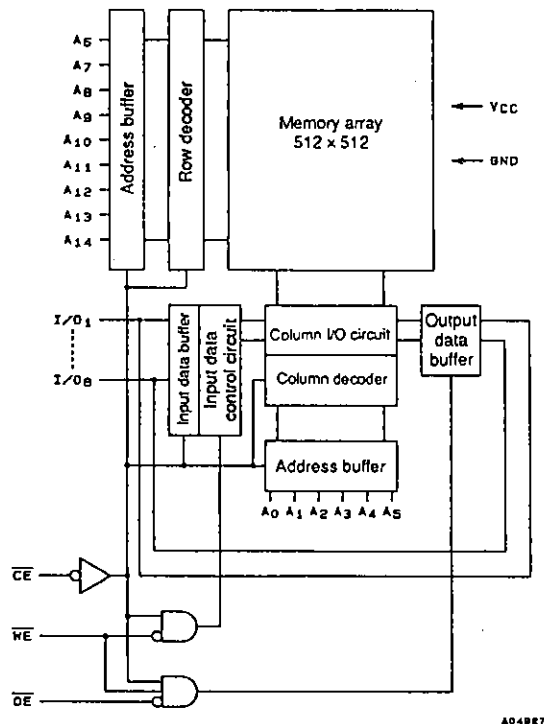
Pin Assignments



Pin Functions

A <sub>0</sub> to A <sub>14</sub>	Address input
WE	Read/write control input
OE	Output enable input
CE	Chip enable input
I/O <sub>1</sub> to I/O <sub>8</sub>	Data I/O
V <sub>CC</sub> , GND	Power, ground

Block Diagram



**LC35256A, AS, AM, AT-70/85/10**

**Truth Table**

Mode	CE	OE	WE	I/O	Current
Read cycle	L	L	H	Data output	$I_{CCA}$
Write cycle	L	X	L	Data input	$I_{CCA}$
Output disable	L	H	H	High impedance	$I_{CCA}$
Unselected	H	X	X	High impedance	$I_{CCS}$

X: H or L

**Specifications**

**Absolute Maximum Ratings**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC\ max}$		7.0	V
Input pin voltage	$V_{IN}$		-0.3* to $V_{CC} + 0.3$	V
I/O pin voltage	$V_{IO}$		-0.3 to $V_{CC} + 0.3$	V
Operating temperature	$T_{opr}$		-40 to +85	°C
Storage temperature	$T_{stg}$		-55 to +125	°C

Note: \* A minimum value of -3.0 V is allowable for pulse widths under 30 ns.

**Input/Output Capacitances at  $T_a = 25^\circ\text{C}$ ,  $f = 1\ \text{MHz}$**

Parameter	Symbol	Conditions	min	typ	max	Unit
I/O pin capacitance	$C_{IO}$	$V_{IO} = 0\ \text{V}$		6	10	pF
Input pin capacitance	$C_{IN}$	$V_{IN} = 0\ \text{V}$		6	10	pF

Note: \* These values are sampled values, and are not measured for all products.

**5 V Operation**

**DC Recommended Operating Ranges at  $T_a = -40$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 4.5$  to  $5.5\ \text{V}$**

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	$V_{CC}$		4.5	5.0	5.5	V
Input voltage	$V_{IH}$		2.2		$V_{CC} + 0.3$	V
	$V_{IL}$		-0.3*		0.8	V

Note: \* A minimum value of -3.0V is allowable for pulse widths under 30 ns.

**DC Electrical Characteristics at  $T_a = -40$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 4.5$  to  $5.5\ \text{V}$**

Parameter	Symbol	Conditions	min	typ*	max	Unit
Input leakage current	$I_{LI}$	$V_{IN} = 0$ to $V_{CC}$	-1.0		+1.0	$\mu\text{A}$
Output leakage current	$I_{LO}$	$V_{CE} = V_{IH}$ or $V_{OE} = V_{IH}$ or $V_{WE} = V_{IL}$ , $V_{IO} = 0$ to $V_{CC}$	-1.0		+1.0	$\mu\text{A}$
Output high level voltage	$V_{OH}$	$I_{OH} = -1.0\ \text{mA}$	2.4			V
Output low level voltage	$V_{OL}$	$I_{OL} = 2.0\ \text{mA}$			0.4	V
Operating current	$I_{CCA2}$	$V_{CE} = V_{IL}$ , $I_{IO} = 0\ \text{mA}$ , $V_{IN} = V_{IH}$ or $V_{IL}$			5.0	mA
	$I_{CCA3}$	$V_{CE} = V_{IL}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ , $I_{IO} = 0\ \text{mA}$ , duty 100%	min cycle	LC35256A, AS, AM, AT-70	35	40
			1 $\mu\text{s}$ cycle	LC35256A, AS, AM, AT-85	30	35
			LC35256A, AS, AM, AT-10	25	30	
				3.5	6.0	
Standby current	$V_{CC} - 0.2\ \text{V}$ / $0.2\ \text{V}$ Inputs	$I_{CCS1}$	$V_{CE} \geq V_{CC} - 0.2\ \text{V}$ , $V_{IN} = 0$ to $V_{CC}$	$T_a \leq 25^\circ\text{C}$	0.01	$\mu\text{A}$
				$T_a \leq 60^\circ\text{C}$		
	$T_a \leq 85^\circ\text{C}$	1.0				
	TTL Inputs	$I_{CCS2}$	$V_{CE} = V_{IH}$ , $V_{IN} = 0$ to $V_{CC}$		1.0	mA

Note: \* Reference values when  $V_{CC} = 5\ \text{V}$  and  $T_a = 25^\circ\text{C}$ .

## LC35256A, AS, AM, AT-70/85/10

### AC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$ , $V_{CC} = 4.5$ to $5.5$ V

#### AC test conditions

Input pulse voltage level: 0.6 to 2.4 V

Input rise and fall times: 5 ns

Input and output timing level: 1.5 V

Output load LC35256A, AS, AM, AT-70: 30 pF + 1 TTL gate (including the jig capacitance)

LC35256A, AS, AM, AT-85/10: 100 pF + 1 TTL gate (including the jig capacitance)

#### Read Cycle

Parameter	Symbol	LC35256A, AS, AM, AT						Unit
		-70		-85		-10		
		min	max	min	max	min	max	
Read cycle time	$t_{RC}$	70		85		100		ns
Address access time	$t_{AA}$		70		85		100	ns
$\overline{CE}$ access time	$t_{CA}$		70		85		100	ns
$\overline{OE}$ access time	$t_{OA}$		35		45		50	ns
Output hold time	$t_{OH}$	10		10		10		ns
$\overline{CE}$ output enable time	$t_{COE}$	10		10		10		ns
$\overline{OE}$ output enable time	$t_{OOE}$	5		5		5		ns
$\overline{CE}$ output disable time	$t_{COD}$		30		30		30	ns
$\overline{OE}$ output disable time	$t_{OOD}$		25		25		25	ns

#### Write Cycle

Parameter	Symbol	LC35256A, AS, AM, AT						Unit
		-70		-85		-10		
		min	max	min	max	min	max	
Write cycle time	$t_{WC}$	70		85		100		ns
Address setup time	$t_{AS}$	0		0		0		ns
Write pulse width	$t_{WP}$	55		55		60		ns
$\overline{CE}$ setup time	$t_{CW}$	60		65		70		ns
Write recovery time	$t_{WR}$	0		0		0		ns
$\overline{CE}$ write recovery time	$t_{WR1}$	0		0		0		ns
Data setup time	$t_{DS}$	35		40		40		ns
Data hold time	$t_{DH}$	0		0		0		ns
$\overline{CE}$ data hold time	$t_{DH1}$	0		0		0		ns
$\overline{WE}$ output enable time	$t_{WOE}$	5		5		5		ns
$\overline{WE}$ output disable time	$t_{WOD}$		30		30		30	ns

### 3 V Operation

#### DC Recommended Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$ , $V_{CC} = 2.7$ to $3.6$ V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	$V_{CC}$		2.7	3.0	3.6	V
Input voltage	$V_{IH}$		$V_{CC} - 0.2$		$V_{CC} + 0.3$	V
	$V_{IL}$		-0.3*		0.2	V

Note: \* A minimum value of -2.0 V is allowable for pulse widths under 30 ns.

## LC35256A, AS, AM, AT-70/85/10

### DC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$ , $V_{CC} = 2.7$ to $3.6$ V

Parameter	Symbol	Conditions	min	typ*	max	Unit		
Input leakage current	$I_{LI}$	$V_{IN} = 0$ to $V_{CC}$	-1.0		+1.0	$\mu\text{A}$		
Output leakage current	$I_{LO}$	$V_{CE} = V_{IH}$ or $V_{OE} = V_{IH}$ or $V_{WE} = V_{IL}$ , $V_{IO} = 0$ to $V_{CC}$	-1.0		+1.0	$\mu\text{A}$		
Output high level voltage	$V_{OH}$	$I_{OH} = -0.5$ mA	$V_{CC} - 0.2$			V		
Output low level voltage	$V_{OL}$	$I_{OL} = 1.0$ mA			0.2	V		
Operating current	$V_{CC} - 0.2$ V/ 0.2 V inputs	$I_{CCA4}$	$V_{CE} = V_{IL}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ , $I_{IO} = 0$ mA, duty 100%	min cycle	LC35256A, AS, AM, AT-70	7	10	mA
					LC35256A, AS, AM, AT-85	6	8	
					LC35256A, AS, AM, AT-10	3	5	
			1 $\mu\text{s}$ cycle			1.5	2.5	
Standby current	$V_{CC} - 0.2$ V/ 0.2 V inputs	$I_{CCS1}$	$V_{CE} \geq V_{CC} - 0.2$ V, $V_{IN} = 0$ to $V_{CC}$	$T_a \leq 25^\circ\text{C}$		0.01		$\mu\text{A}$
				$T_a \leq 60^\circ\text{C}$			0.8	
				$T_a \leq 85^\circ\text{C}$			4.0	

Note: Reference values when  $V_{CC} = 3$  V and  $T_a = 25^\circ\text{C}$ .

### AC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$ , $V_{CC} = 2.7$ to $3.6$ V

#### AC test conditions

Input pulse voltage level: 0.2 V to  $V_{CC} - 2.0$  V

Input rise and fall times: 10 ns

Input and output timing level: 1.5 V

Output load LC35256A, AS, AM, AT-70: 30 pF (including the jig capacitance)

LC35256A, AS, AM, AT-85/10: 100 pF (including the jig capacitance)

#### Read Cycle

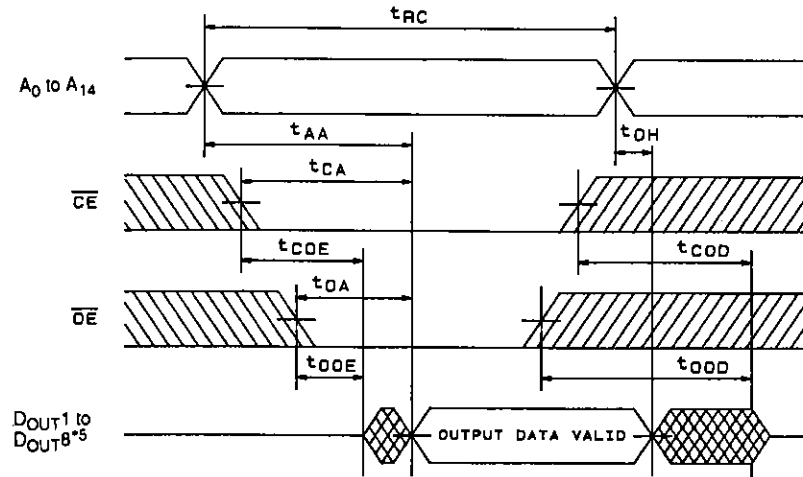
Parameter	Symbol	LC35256A, AS, AM, AT						Unit
		-70		-85		-10		
		min	max	min	max	min	max	
Read cycle time	$t_{RC}$	200		250		500		ns
Address access time	$t_{AA}$		200		250		500	ns
$\overline{\text{CE}}$ access time	$t_{CA}$		200		250		500	ns
$\overline{\text{OE}}$ access time	$t_{OA}$		100		130		250	ns
Output hold time	$t_{OH}$	20		20		20		ns
$\overline{\text{CE}}$ output enable time	$t_{COE}$	20		20		20		ns
$\overline{\text{OE}}$ output enable time	$t_{OOE}$	10		10		10		ns
$\overline{\text{CE}}$ output disable time	$t_{COD}$		60		80		120	ns
$\overline{\text{OE}}$ output disable time	$t_{OOD}$		50		70		100	ns

#### Write Cycle

Parameter	Symbol	LC35256A, AS, AM, AT						Unit
		-70		-85		-10		
		min	max	min	max	min	max	
Write cycle time	$t_{WC}$	200		250		500		ns
Address setup time	$t_{AS}$	0		0		0		ns
Write pulse width	$t_{WP}$	140		160		200		ns
$\overline{\text{CE}}$ setup time	$t_{CW}$	150		180		250		ns
Write recovery time	$t_{WR}$	0		0		0		ns
$\overline{\text{CE}}$ write recovery time	$t_{WR1}$	0		0		0		ns
Data setup time	$t_{DS}$	130		150		180		ns
Data hold time	$t_{DH}$	0		0		0		ns
$\overline{\text{CE}}$ data hold time	$t_{DH1}$	0		0		0		ns
$\overline{\text{WE}}$ output enable time	$t_{WOE}$	10		10		10		ns
$\overline{\text{WE}}$ output disable time	$t_{WOD}$		60		80		120	ns

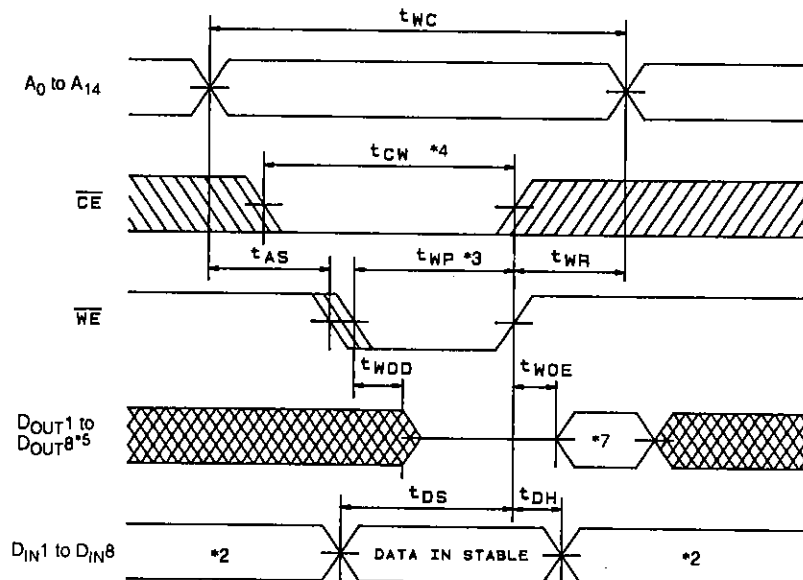
Timing Chart

Read Cycle\*1



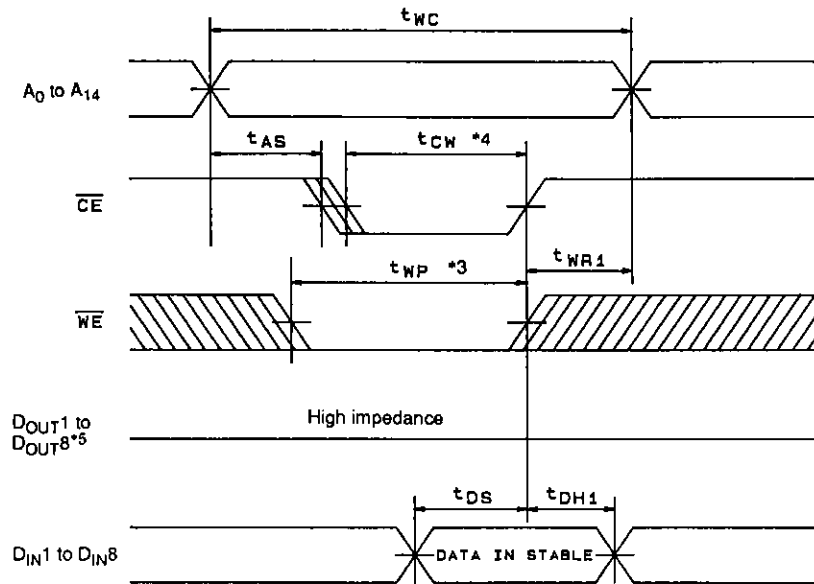
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Write Cycle 1 ( $\overline{WE}$  write)\*6



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Write Cycle 2 ( $\overline{CE}$  write)\*6



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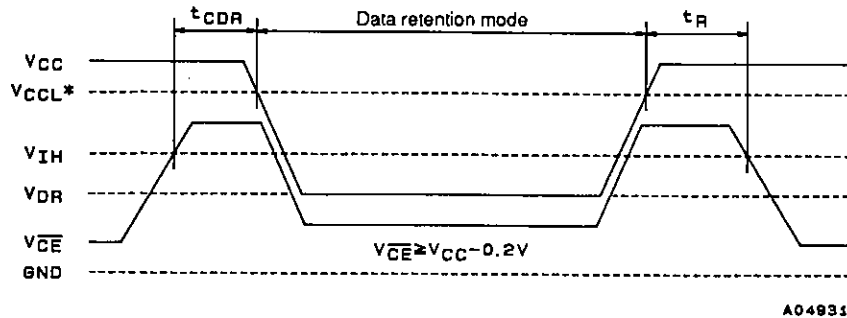
- Note:
1. Set  $\overline{WE}$  high during the read cycle.
  2. External reverse phase signals must not be applied when  $D_{OUT}$  is in the output state.
  3. The  $t_{WP}$  period is defined to be the period where both  $\overline{CE}$  and  $\overline{WE}$  are low. In particular, it is the period between the point where  $\overline{WE}$  falls and the rise of  $\overline{CE}$  or  $\overline{WE}$ , whichever rises first.
  4. The  $t_{CW}$  period is defined to be the period where both  $\overline{CE}$  and  $\overline{WE}$  are low. In particular, it is the period between the point where  $\overline{CE}$  falls and the rise of  $\overline{CE}$  or  $\overline{WE}$ , whichever rises first.
  5.  $D_{OUT}$  goes to the high impedance state in any of the following conditions: when  $\overline{OE}$  is high, when  $\overline{CE}$  is high, or when  $\overline{WE}$  is low.
  6.  $\overline{OE}$  must be held either high or low during the write cycle.
  7.  $D_{OUT}$  has the same phase as the write data for this write cycle.

Data Retention Characteristics at  $T_a = -40$  to  $+85^\circ\text{C}$

Parameter	Symbol	Conditions	min	typ*1	max	Unit
Data retention supply voltage	$V_{DR}$	$V_{\overline{CE}} \geq V_{CC} - 0.2\text{ V}$	2.0		5.5	V
Data retention supply current	$I_{CCDR}$	$V_{CC} = 3.0\text{ V}, V_{\overline{CE}} \geq V_{CC} - 0.2\text{ V}$	$T_a \leq 25^\circ\text{C}$	0.01		$\mu\text{A}$
			$T_a \leq 60^\circ\text{C}$		0.7	
			$T_a \leq 85^\circ\text{C}$		3.5	
Chip enable setup time	$t_{CDR}$		0			ns
Chip enable hold time	$t_R$		$t_{RC}$ *2			ns

- Note:
1. Reference values when  $V_{CC} = 3\text{ V}$  and  $T_a = 25^\circ\text{C}$ .
  2.  $t_{RC}$ : read cycle time

## Data Retention Waveforms



\*  $V_{CCL}$  —  $\left\{ \begin{array}{l} 5V \text{ operation: } 4.5V \\ 3V \text{ operation: } 2.7V \end{array} \right.$

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