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# LB11988HR

## Monolithic Digital IC Fan Motor Driver

### Overview

LB11988HR is a motor driver IC optimal for driving the DC fan motors.

### Functions

- Three-phase full-wave current linear drive
- Built-in current limiter circuit
- Built-in saturation prevention circuits in both the upper and lower sides of the output stage
- Forward/backward rotation direction setting circuit built in
- FG amplifier
- Thermal shutdown circuit

### Specifications

#### Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter                   | Symbol       | Conditions     | Ratings     | Unit             |
|-----------------------------|--------------|----------------|-------------|------------------|
| Maximum supply voltage      | $V_{CC}$ max |                | 24          | V                |
|                             | $V_S$ max    |                | 24          | V                |
| Maximum output current      | $I_O$ max    |                | 1.3         | A                |
| Allowable power dissipation | $P_d$ max    | Independent IC | 0.8         | W                |
| Operating temperature       | $T_{opr}$    |                | -40 to +85  | $^\circ\text{C}$ |
| Storage temperature         | $T_{stg}$    |                | -55 to +150 | $^\circ\text{C}$ |

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

#### Allowable Operating Ratings at $T_a = 25^\circ\text{C}$

| Parameter            | Symbol     | Conditions          | Ratings              | Unit  |
|----------------------|------------|---------------------|----------------------|-------|
| Supply voltage       | $V_S$      |                     | 5 to 22              | V     |
|                      | $V_{CC}$   |                     | 5 to 22              | V     |
| Hall input amplitude | $V_{HALL}$ | Between Hall inputs | $\pm 30$ to $\pm 80$ | mVo-p |

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**Electrical Characteristics** at  $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 12\text{V}$ ,  $V_S = 12\text{V}$

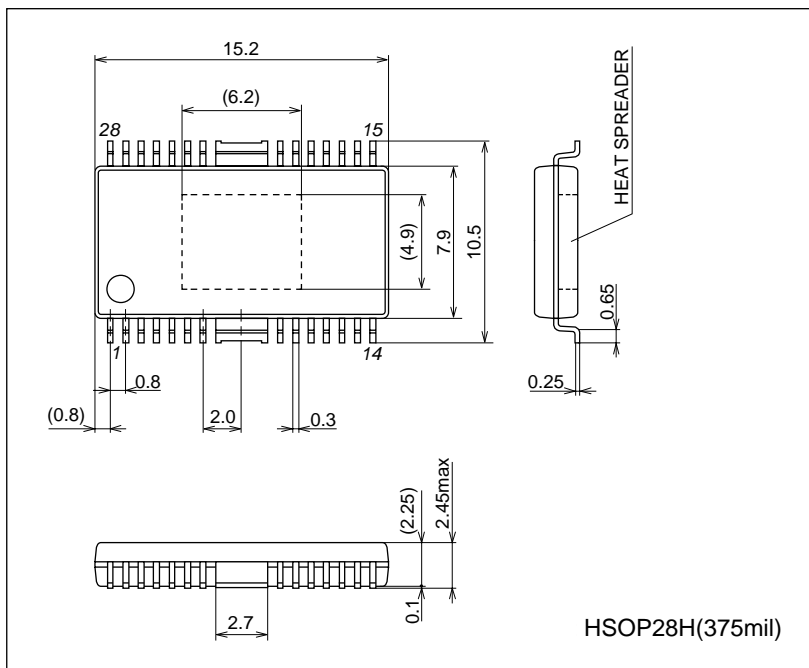
| Parameter  | Symbol           | Conditions   | Ratings |      |              | Unit             |
|--|------------------|--|---------|------|--------------|------------------|
|  |                  |  | min     | typ  | max          |                  |
| $V_{CC}$ current drain                                   | $I_{CC}$         | $R_L = 560\Omega$ (Y)  |         | 15   | 24           | mA               |
| <b>Output</b>  |                  |  |         |      |              |                  |
| Output saturation voltage                                | $V_{Osat1}$      | $I_O = 500\text{mA}$ , $R_f = 0.5\Omega$ , Sink + Source<br>(Saturation prevention function included)    |         | 2.1  | 2.6          | V                |
|  | $V_{Osat2}$      | $I_O = 1.0\text{A}$ , $R_f = 0.5\Omega$ , Sink + Source<br>(Saturation prevention function included)     |         | 2.6  | 3.5          | V                |
| Output leakage current                                   | $I_{Oleak}$      |  |         |      | 1.0          | mA               |
| <b>Hall amplifier</b>                                    |                  |  |         |      |              |                  |
| Input offset voltage                                     | $V_{Off}$ (HALL) |  | -6      |      | +6           | mV               |
| Input bias current                                       | $V_b$ (HALL)     | $V_{IN}$ , $W_{IN}$  |         | 1    | 3            | $\mu\text{A}$    |
| Common-mode input voltage                                | $V_{cm1}$ (HALL) | $V_{CC}=V_S=12\text{V}$  | 3       |      | $V_{CC}-3$   | V                |
|  | $V_{cm2}$ (HALL) | $V_{CC}=V_S=5\text{V}$   | 1.5     |      | $V_{CC}-1.5$ | V                |
| <b>FR</b>  |                  |  |         |      |              |                  |
| Threshold voltage  | $V_{FRTH}$       |  | 4       |      | 8            | V                |
| Input bias current                                       | $I_b$ (FR)       |  | -5      |      |              | $\mu\text{A}$    |
| <b>Current limiter</b>                                   |                  |  |         |      |              |                  |
| LIM pin current limit level                              | $I_{LIM}$        | $R_f = 0.5\Omega$ , With the Hall input logic states fixed<br>(U, V, W = high, high, low)                |         | 1    |              | A                |
| <b>Saturation</b>  |                  |  |         |      |              |                  |
| Saturation prevention circuit lower side voltage setting | $V_{Osat}$ (DET) | $R_L = 560\Omega$ (Y), $R_f = 0.5\Omega$ , The voltage between each output and the corresponding $R_f$ . |         | 0.28 |              | V                |
| <b>FG amplifier</b>                                      |                  |  |         |      |              |                  |
| Upper side output saturation voltage                     | $V_{satu}$ (SH)  |  | 11.8    |      |              | V                |
| Lower side output saturation voltage                     | $V_{satd}$ (SH)  |  |         |      | 0.3          | V                |
| Hysteresis   | $V_{hys}$        |  |         | 23   |              | mV               |
| TSD operating temperature                                | T-TSD            | Design target value*   |         | 170  |              | $^\circ\text{C}$ |

Note \* : Items shown to be design target values in the conditions column are not measured.

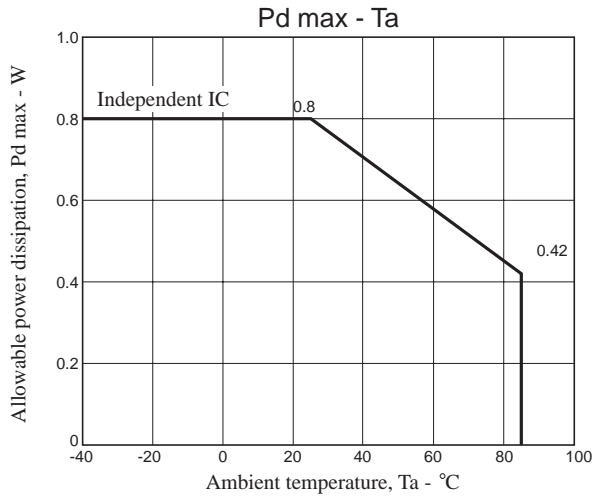
## Package Dimensions

unit : mm (typ)

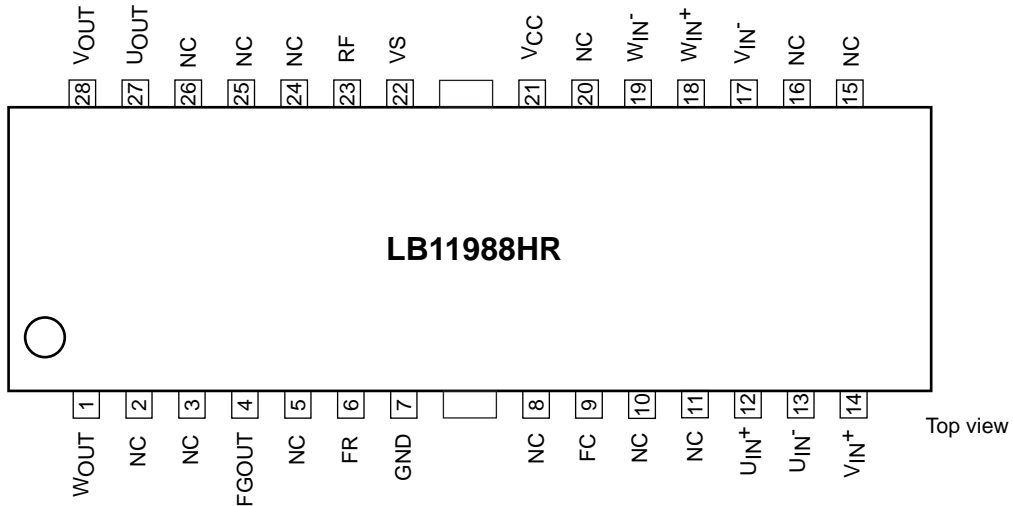
3233B



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## Pin Assignment



## Truth Table and Control Functions

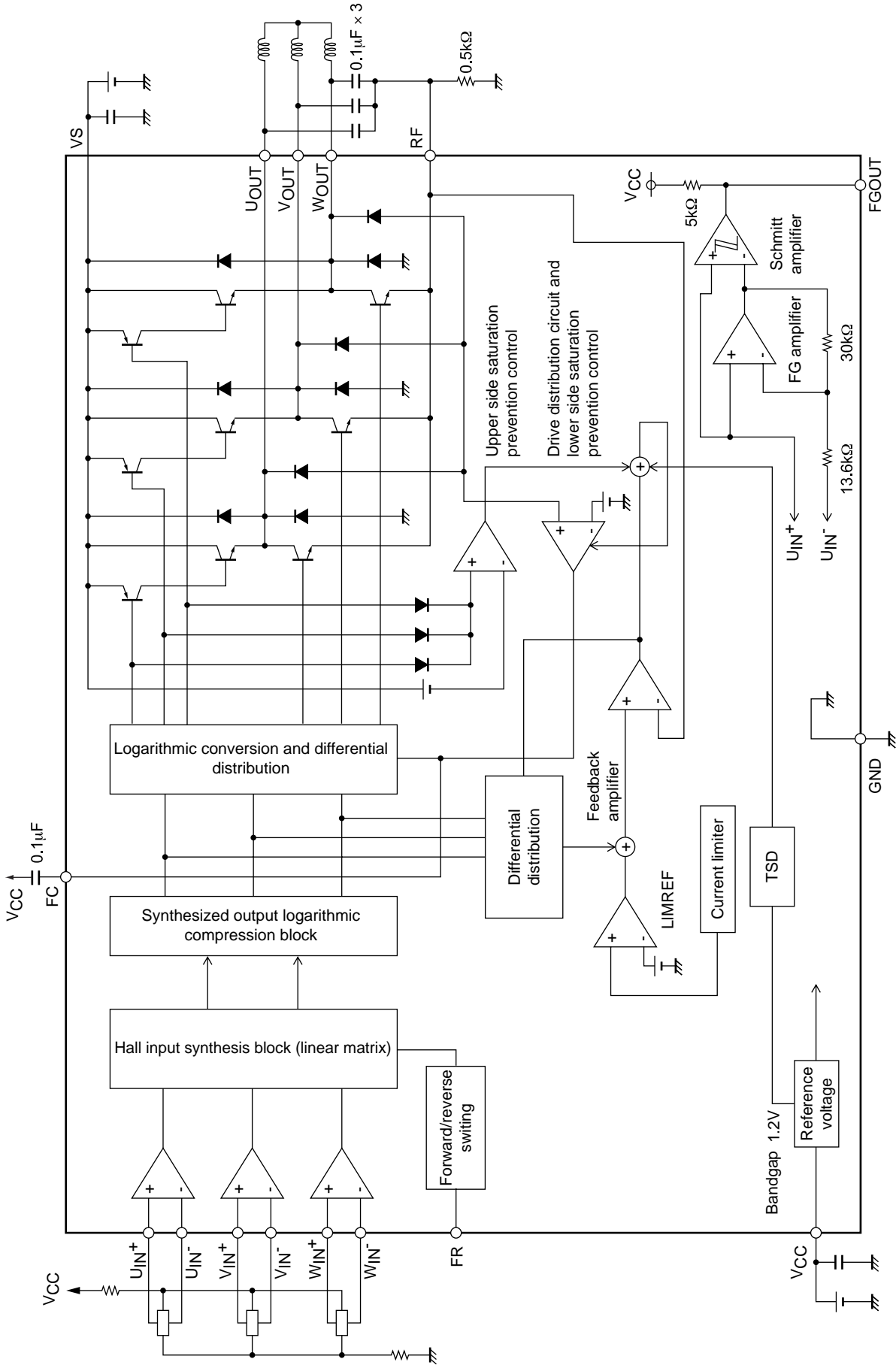
|   | Source→Sink | Hall input |   |   | FR |
|---|-------------|------------|---|---|----|
|   |             | U          | V | W |    |
| 1 | V → W       | H          | H | L | H  |
|   | W → V       |            |   |   | L  |
| 2 | U → W       | H          | L | L | H  |
|   | W → U       |            |   |   | L  |
| 3 | U → V       | H          | L | H | H  |
|   | V → U       |            |   |   | L  |
| 4 | W → V       | L          | L | H | H  |
|   | V → W       |            |   |   | L  |
| 5 | W → U       | L          | H | H | H  |
|   | U → W       |            |   |   | L  |
| 6 | V → U       | L          | H | L | H  |
|   | U → V       |            |   |   | L  |

Note : The "H" state for FR is defined as a voltage of 8V or higher, and the "L" state for FR is defined as a voltage of 4V or lower. (When  $V_{CC} = 12V$ .)

Note : For the Hall inputs, the input high state is defined to be the state where the (+) input is higher than the corresponding (-) input by 0.01V or higher, and the input low state is defined to be the state where the (+) input is lower than the corresponding (-) input by 0.01V or higher.

Note : Since this drive technique is a 180° current application scheme, the phases other than the sink and the source phases will not turn off.

Block Diagram



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## Equivalent Circuit

| Pin name   | Equivalent circuit |
|--|--------------------|
| $U_{IN}^+$<br>$U_{IN}^-$<br>$V_{IN}^+$<br>$V_{IN}^-$<br>$W_{IN}^+$<br>$W_{IN}^-$ |                    |
| $U_{OUT}$<br>$V_{OUT}$<br>$W_{OUT}$<br>$R_F$<br>$V_S$                            |                    |
| FR   |                    |
| FC   |                    |
| FGOUT  |                    |

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## Pin Functions

| Pin No.                    | Pin name  | Function   |
|----------------------------|---|--|
| 7<br>FRAME                 | GND   | Ground for circuits other than the output transistors.<br>Note that the Rf pin will be at the lowest potential of the output transistors.  |
| 4                          | FGOUT   | This is the FG amplifier output pin. Internally, it is a resistive load. (Pull up)   |
| 6                          | FR  | Forward/reverse switching pin  |
| 9                          | FC  | Corrects the frequency characteristics of the saturation prevention circuit loop and current limiter circuit.  |
| 12, 13<br>14, 17<br>18, 19 | $U_{IN}^+$ , $U_{IN}^-$<br>$V_{IN}^+$ , $V_{IN}^-$<br>$W_{IN}^+$ , $W_{IN}^-$ | U-phase Hall input. Logic high refers to the state where $IN^+ > IN^-$ .<br>V-phase Hall input. Logic high refers to the state where $IN^+ > IN^-$ .<br>W-phase Hall input. Logic high refers to the state where $IN^+ > IN^-$ .   |
| 21                         | $V_{CC}$  | Power supply provided to all IC internal circuits other than the output block.<br>This voltage must be stabilized so that ripple and noise do not enter the IC.  |
| 22                         | $V_S$   | Output block power supply  |
| 23                         | RF  | Used for output current detection. The current limiter circuit operates using the resistor (Rf) connected between this pin and ground.<br>Note that the lower side saturation prevention circuit operates according to the voltage that appears on this pin. Since the over-saturation level is set by this voltage, the level of the lower side saturation prevention circuit may be degraded in the large current region if the value of Rf is made extremely small. |
| 27<br>28<br>1              | $U_{OUT}$<br>$V_{OUT}$<br>$W_{OUT}$   | U-phase Hall output.<br>V-phase Hall output.<br>W-phase Hall output. } (These pins include internal spark killer diodes.)  |

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