



SANYO Semiconductors

DATA SHEET

LA5693AM

Monolithic Linear IC

Voltage Regulator Driver with Watchdog Timer

Overview

The LA5693AM is a single-chip voltage regulator for microcomputer system monitor use that performs the functions of 5V output voltage control, watchdog timer, and voltage detector. Since the LA5693AM can hold the reset output, it is especially suited for use in peripheral control and monitor output applications including valves used in refrigeration equipment, hot water supply system. In addition, as the LA5693AM assures reliable operation over a wide range of operating temperatures (-40 to +125°C), it can find many applications in microcontroller systems for use in automobiles and other industrial equipment.

Features

- An external PNP transistor can be used to provide a low-saturation voltage regulator.
- Since the CK input has no edge detector, a high degree of flexibility is allowed in applications.
- Variable detection voltage.
- The watchdog time can be made longer.

Functions

- Output voltage 5V control.
- Watchdog timer.
- Power-ON reset function.
- Reset hold output [$\overline{\text{RES}}$ (2)] (Cleared with CK reininput).

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Control pin voltage	$V_{\text{CONT max}}$	1sec	60	V
Control pin voltage	$V_{\text{CONT max}}$		41	V
Control pin current	$I_{\text{CONT max}}$	$*V_{\text{CC}} \geq 6\text{V}$	11	mA
CK input voltage	$V_{\text{CK max}}$		25	v
Reset pin voltage	$V_{\overline{\text{RES}}(1) \text{ max,}}$ $V_{\overline{\text{RES}}(2) \text{ max}}$		41	V

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Parameter	Symbol	Conditions	Ratings	Unit
Allowable power dissipation	Pd max		370	mW
Operating temperature	Topr		-40 to +125	°C
Storage temperature	Tstg		-55 to +150	°C

* : A PNP transistor is connected to the LA5693AM externally to provide a low-saturation voltage regulator.

Therefore, I_{CONT} ≈ 100mA will flow, as starting current, in the V_{CC} range where the output cannot be regulated.

Operating Conditions at Ta = -40 to +125°C

Parameter	Symbol	Conditions	Ratings	Unit
Control pin voltage	V _{CONT}		6 to 40	V
Control pin current	I _{CONT}		10	mA
Reset output current	I _{RES(1)} max, I _{RES(2)} max	$\overline{RES}(2)$: 10kΩ pull-up	8	mA
Reset detection voltage	V _S min		4	V

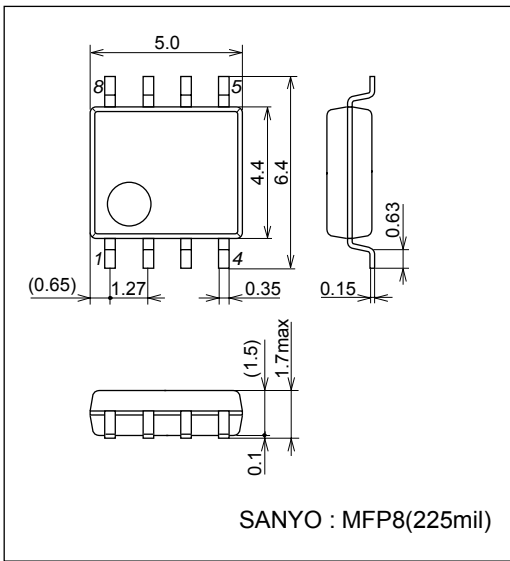
Operating Characteristics at Ta= -40 to +125°C, V_{CC}=14V, I_O=50mA, unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output voltage	V _O		4.8	5.0	5.2	V
Line regulation1	ΔV _{OLN1}	9V ≤ V _{CC} ≤ 16V		2	10	mV
Line regulation2	ΔV _{OLN2}	6V ≤ V _{CC} ≤ 40V		4	30	mV
Load regulation	ΔV _{OLD}	1mA ≤ I _O ≤ 50mA		4	30	mV
Current dissipation	I _{CC}	I _O = 0		4.4	6.5	mA
Output noise voltage	V _{NO}	10Hz ≤ f ≤ 100kHz, V _{CK} = 0		150		μV
Temperature coefficient of output voltage	ΔV _O / ΔTa	I _O = 5mA, -40°C ≤ Ta ≤ +85°C		±0.2		mV/°C
Reference voltage	V _{REF}		1.13	1.18	1.23	V
'H'-level CK input voltage	V _{IH}		2			V
'L'-level CK input voltage	V _{IL}				0.8	V
'H'-level CK input current	I _{IH}	V _{CK} = 5V		0.3	0.7	mV
'L'-level CK input current	I _{IL}	V _{CK} = 0V	-1.0	-0.1		μA
'H'-level reset output voltage	V _{ORH(1)} , V _{ORH(2)}	$\overline{RES}(2)$: 10kΩ pull-up	4.8	5.0	5.2	V
'L'-level reset output voltage1	V _{ORL(1)1} , V _{ORL(1)1}	$\overline{RES}(2)$: 10kΩ pull-up		40	200	mV
'L'-level reset output voltage2	V _{ORL(1)2} , V _{ORL(1)2}	I _{RES(1)} = I _{RES(2)} = 8mA		0.16	0.8	V
CK input pulse width	t _{CKW}	V _{CK} = 5V	3			μs
Reset output delay time	t _d	C _t = 1μF	7.0	10	20	ms
Watchdog time 1	t _{WD1}	C _t = 1μF (Ta = -40 to +125°C)	25	40	60	ms
Watchdog time 2	t _{WD2}	C _t = 1μF (Ta = -40 to +85°C)	25	40	53	ms
Watchdog reset time	t _{WR}	C _t = 1μF	0.1	0.25	0.4	ms
Reset hysteresis voltage	V _{hys}	V _S = 4.5V	100	200	300	mV

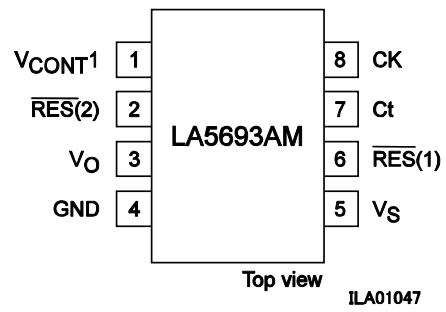
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Package Dimensions

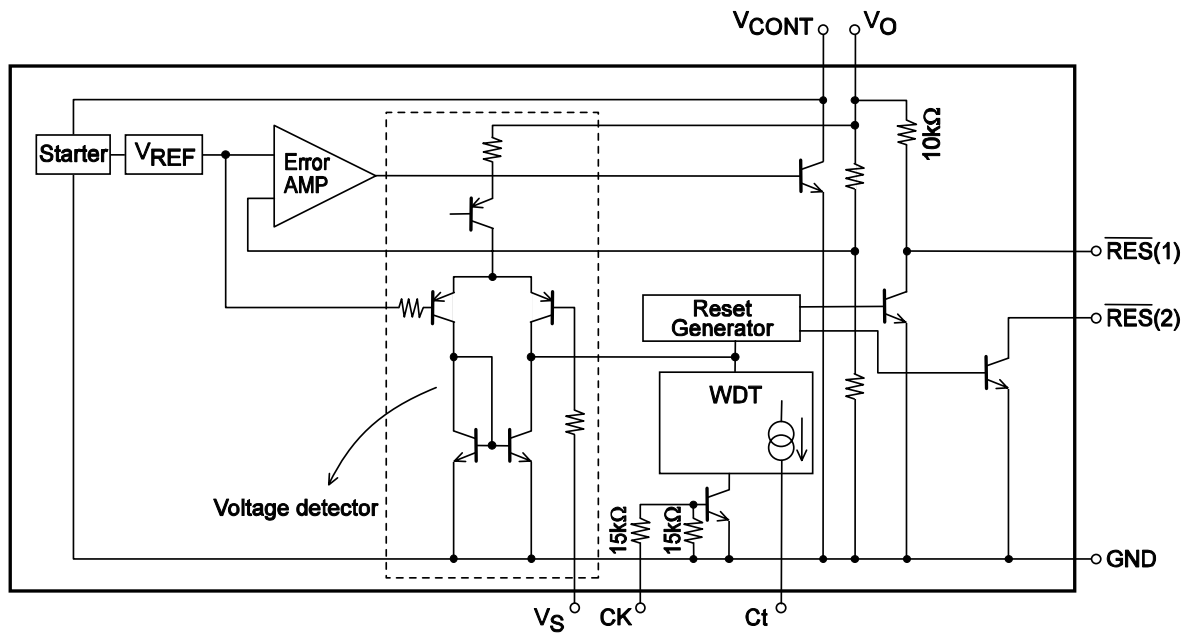
unit : mm
3032D



Pin Assignment



Block Diagram

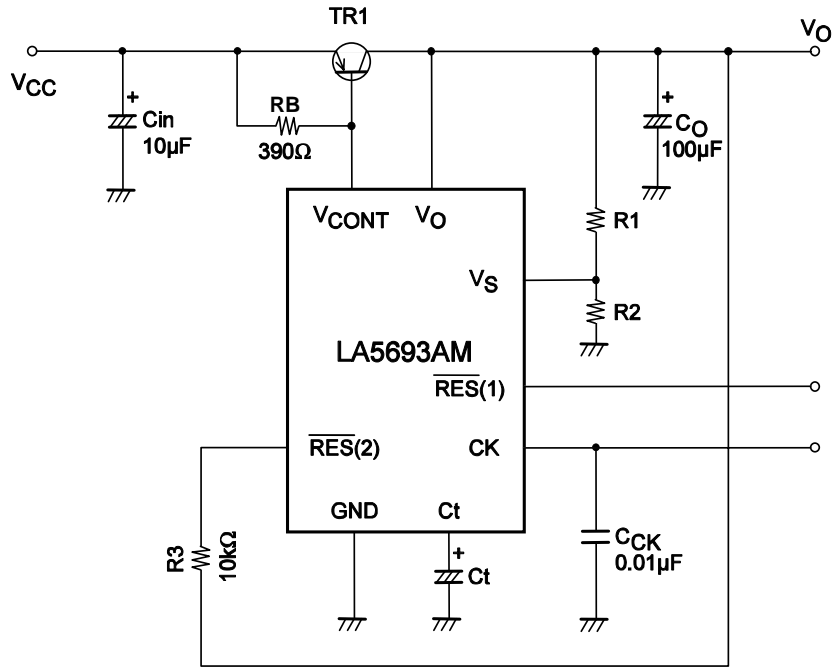


RES(1) : Contains a pull-up resistor of 10kΩ.
RES(2) : Open collector.

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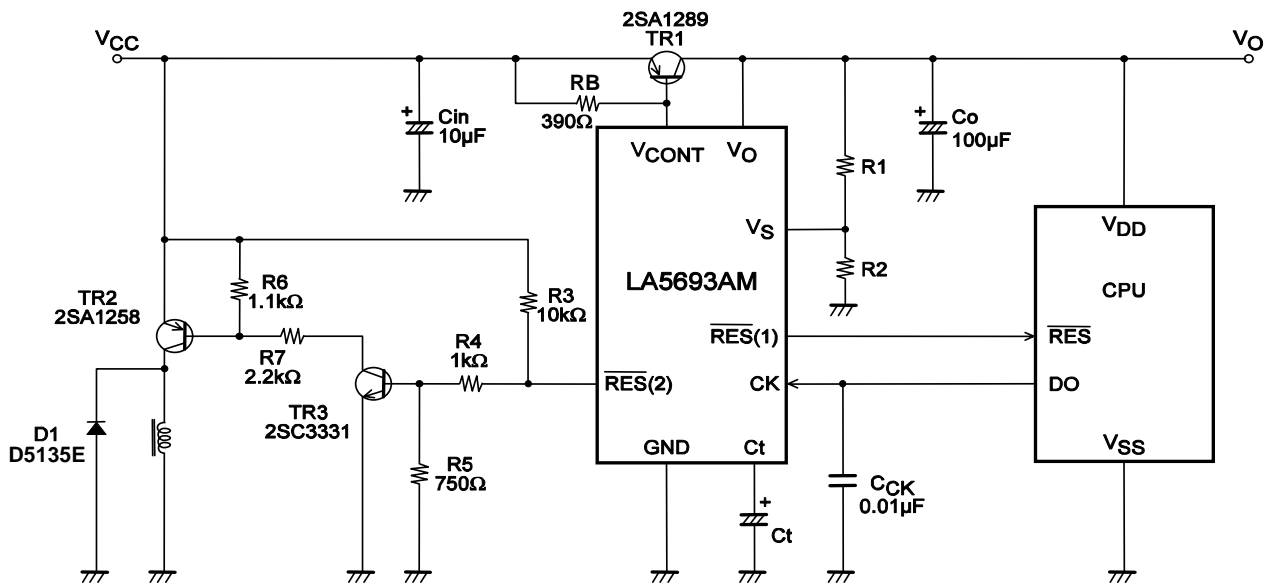
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Test Circuit



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Sample Application Circuit



$$V_S = V_{REF} \times \left(\frac{R_1}{R_2} + 1 \right)$$

$$V_{REF} \approx 1.18[V]$$

$$t_d = 10 \times C_t (\mu F) \quad [ms]$$

$$t_{WD} = 40 \times C_t (\mu F) \quad [ms]$$

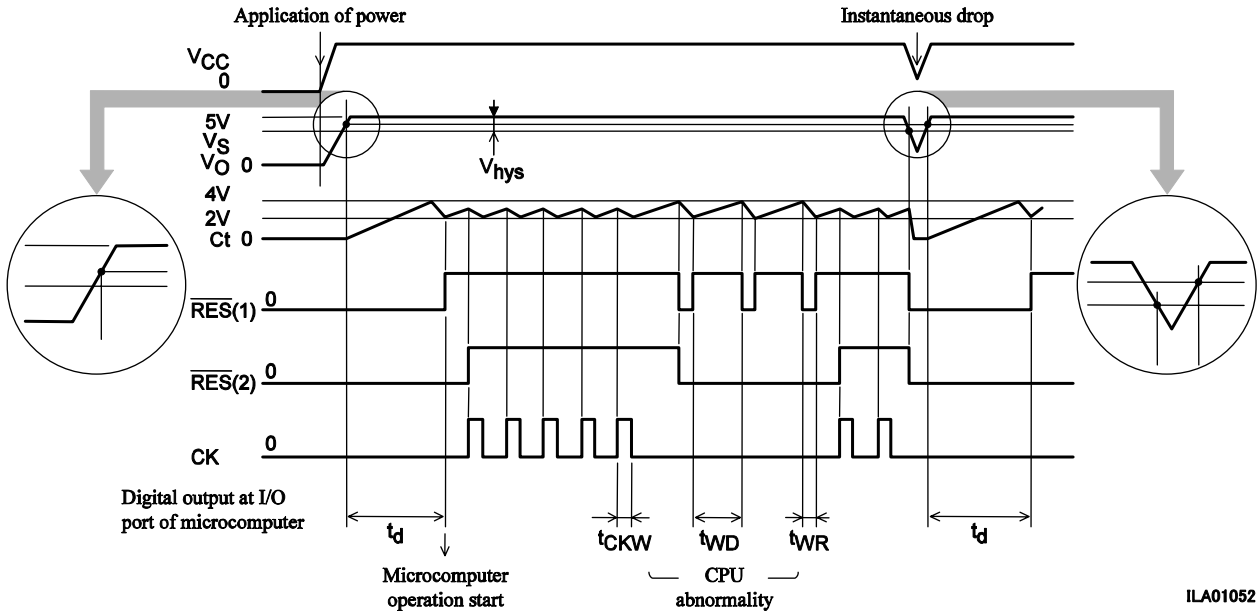
$$t_{WR} = 0.25 \times C_t (\mu F) \quad [ms]$$

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Note on application

1. For stable operation, place C_{in} , C_O , and $TR1$ as near to the IC as possible.
2. When used in $0^{\circ}C$ or below it, a capacitor of which impedance at high-frequency operation is low and has a good temperature characteristic (such as SANYO OS-CON capacitor or others) should be used to prevent oscillation.
3. Set V_S to the output voltage level where the circuit will be reset using external resistors $R1$ and $R2$. V_S should be set to 4V or greater due to internal circuit operation.
4. CCK must be inserted to cut the high range element of clock noise to prevent it from becoming a reset output noise.
5. For C_t , a capacitor which less varies the capacitance according to the temperature should be used.

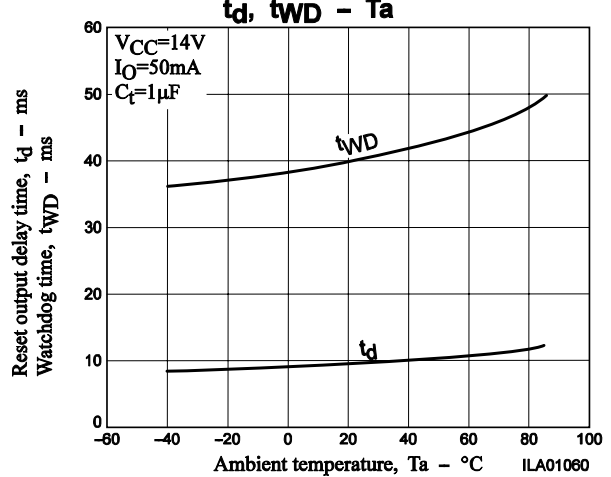
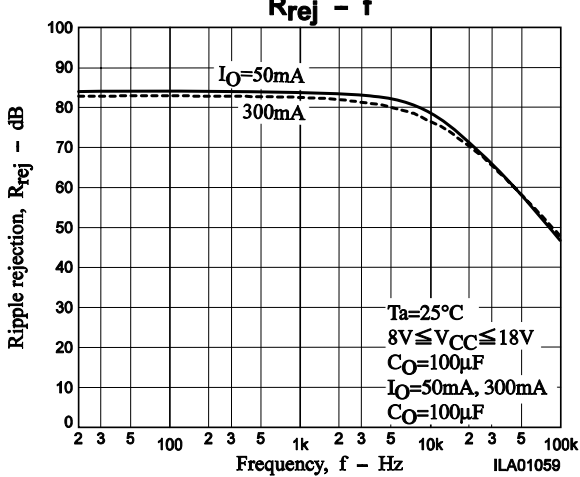
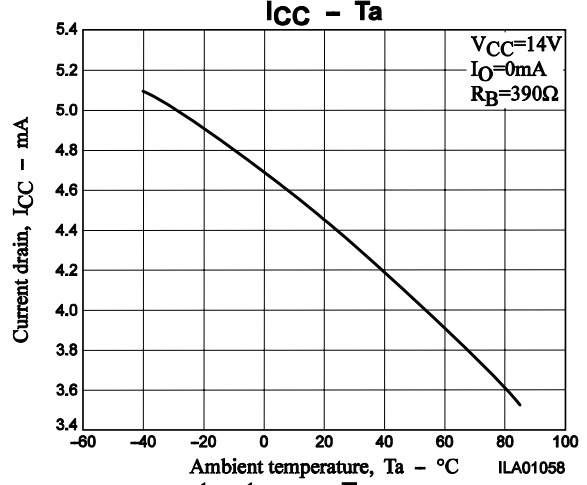
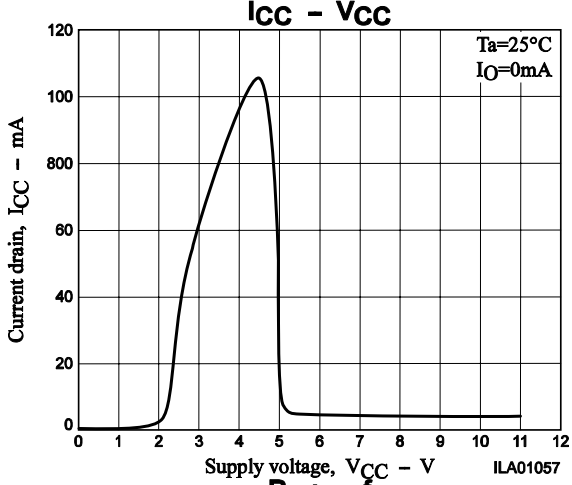
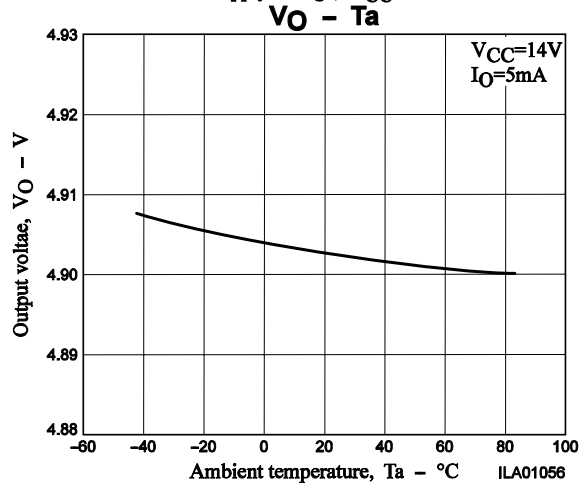
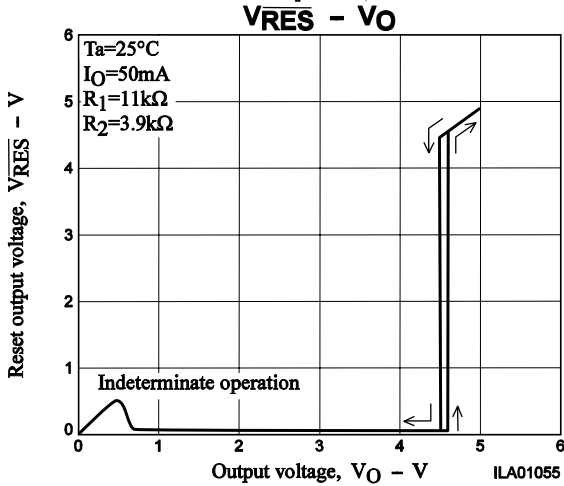
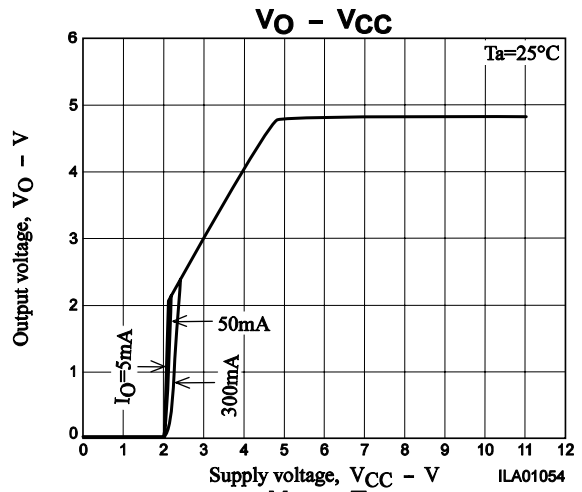
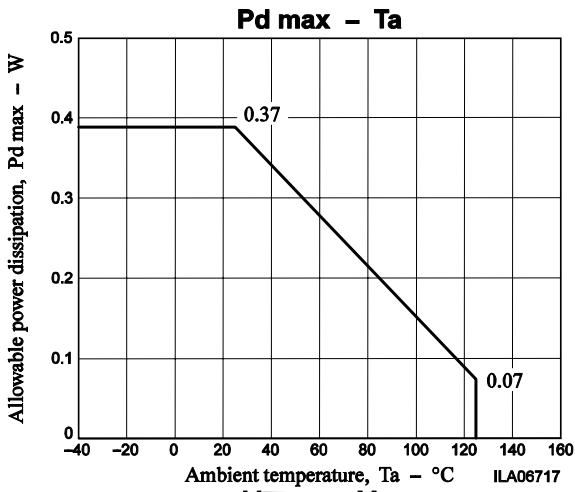
Timing Chart

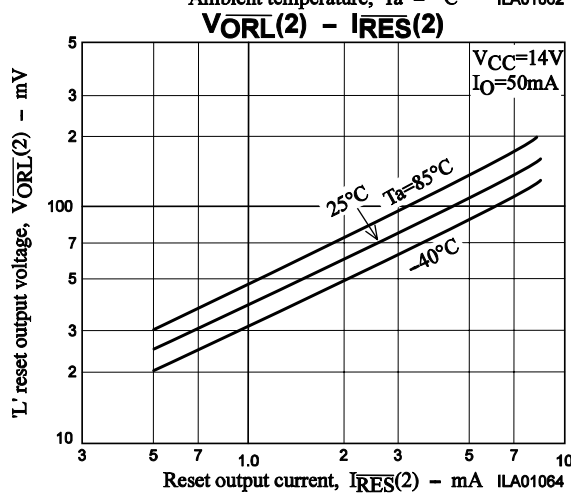
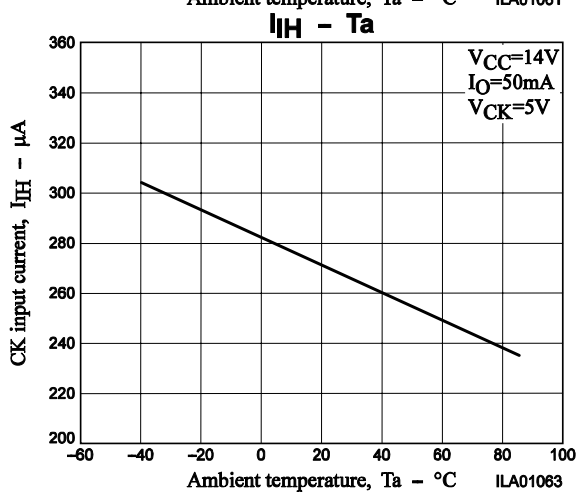
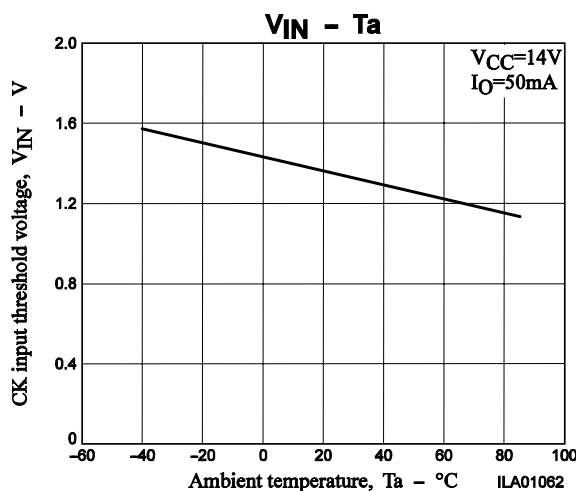
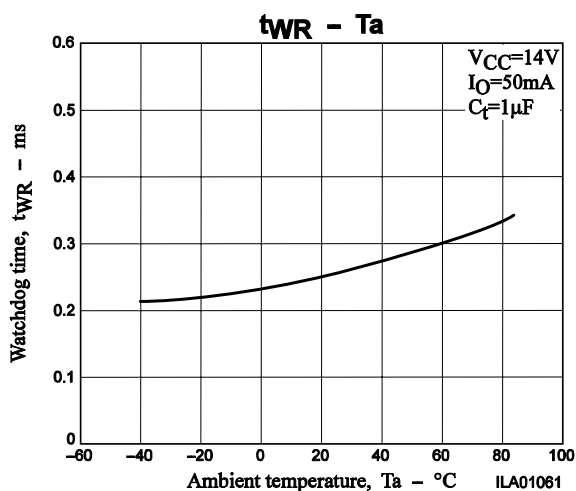


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Note : Edge-triggered at the point indicated by the arrow of CK signal.

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