Ordering number: EN5386

Monolithic Linear IC

LA5312V

Variable Divided Voltage Generator for LCDs

Overview

The LA5312V is a variable divided voltage generator IC for multiple drive of LCD matrix.

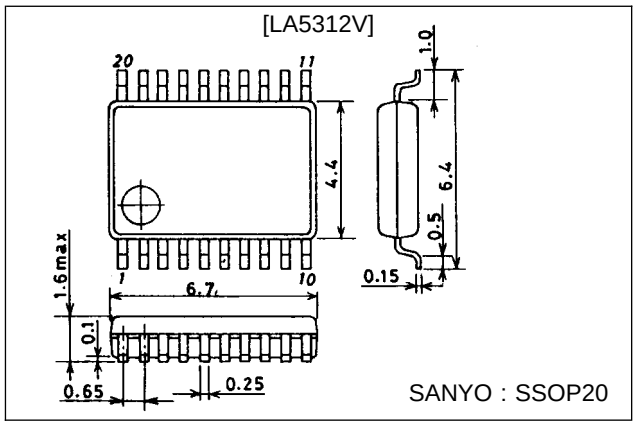
Features

- Power supply for variable bias LCD drive (1/5 to 1/19 bias available by internal resistors)
- Four voltage outputs generated by four operational amplifiers.
- Low current drain (0.18 mA typ.)
- Miniflat package for miniaturization.

Package Dimensions

unit : mm

3179-SSOP20



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{EE} max	$V_{CC} - V_{EE}$	36	V
Maximum output current	I_{OUT} max	V1 – V4	*Internal	mA
Allowable power dissipation	Pd max		330	mW
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–30 to +125	°C

Note 1: Continuous operation (without damage) is guaranteed in the above ranges.
Note 2: *The maximum output current is the value stipulated under the test conditions on page 4.
Note 3: Output pins V1 to V4-to-V_{CC} or GND short not exceeding 1 ms is acceptable. ($|V_{CC} - V_{EE}| < 35$ V)

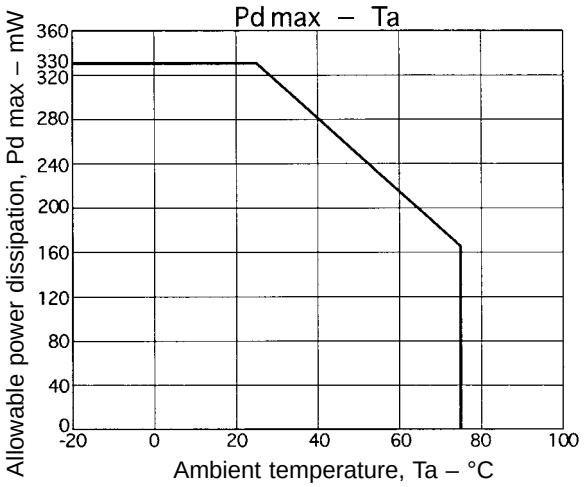
Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{EE}	$V_{CC} - V_{EE}$	–35.5 to –6	V
Input voltage	V_{REF}	$V_{REF} \geqq V_{EE}$: $V_{CC} - V_{REF}$	–35 to –6	V
Output current	I_{OUT}1,2	V1, V2	–0.5 to +5	mA
	I_{OUT}3,4	V3, V4	–10 to +5	mA

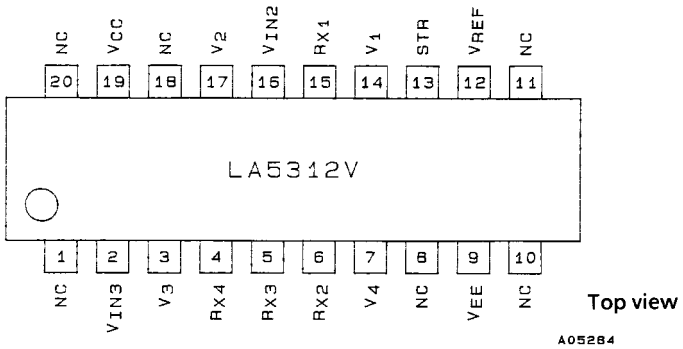
Note 4: Set V_{CC} and V_{EE} so that |V1| and $|V_{EE} - V4|$ are 1 V or more.

Operating Characteristics at Ta = 25°C, $V_{CC} - V_{EE}$ = 20 V, $V_{REF} = V_{EE}$, R_X = 8 R

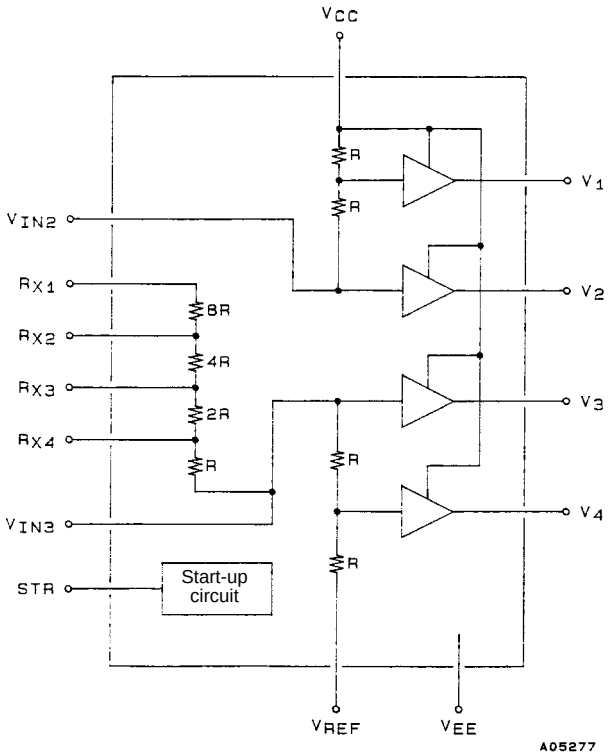
Parameter	Symbol	Conditions	min	typ	max	Unit
Current drain	I_{CC}, I_{EE}	STR = 5 V : V_{CC}, V_{EE}		0.18	0.3	mA
Input current	I_{STR}	STR = 5 V : STR		9	12	µA
Output voltage ratio	Ra1	V2 / V1	1.96	2.00	2.04	—
	Ra2	(V_{REF} – V3) / (V_{REF} – V4)	1.96	2.00	2.04	—
	Rb1	V_{REF} / V1	11.64	12.00	12.36	—
	Rb2	V_{REF} / V2	5.82	6.00	6.18	—
	Rb3	V_{REF} / (V_{REF} – V3)	5.82	6.00	6.18	—
	Rb4	V_{REF} / (V_{REF} – V4)	11.64	12.00	12.36	—
Internal resistance ratio	R_X1	Referenced to R across R_X4 and $V_{IN}3$: $R_X1 - R_X2$		8		—
	R_X2	: $R_X1 - R_X3$		12		—
	R_X3	: $R_X1 - R_X4$		14		—
	R_X4	: $R_X1 - V_{IN}3$		15		—
Resistance value	R	R value when voltage is applied across R_X4 and $V_{IN}3$ is 0.5 V : $R_X4 - V_{IN}3$		30		kΩ
Load regulation	△V1	+0.1 mA < $I_{OUT}1$ < +5 mA : V1			±20	mV
	△V2	+0.1 mA < $I_{OUT}2$ < +5 mA : V2			±20	mV
	△V3	+0.1 mA < $I_{OUT}3$ < +5 mA : V3			±20	mV
	△V4	+0.1 mA < $I_{OUT}4$ < +5 mA : V4			±20	mV
	–△V1	–0.5 mA < $I_{OUT}1$ < –0.1 mA : V1			±20	mV
	–△V2	–0.5 mA < $I_{OUT}2$ < –0.1 mA : V2			±20	mV
	–△V3	–10 mA < $I_{OUT}3$ < –0.1 mA : V3			±20	mV
	–△V4	–10 mA < $I_{OUT}4$ < –0.1 mA : V4 (Source I_{OUT} is negative and sink I_{OUT} is positive).			±20	mV



Pin Assignment

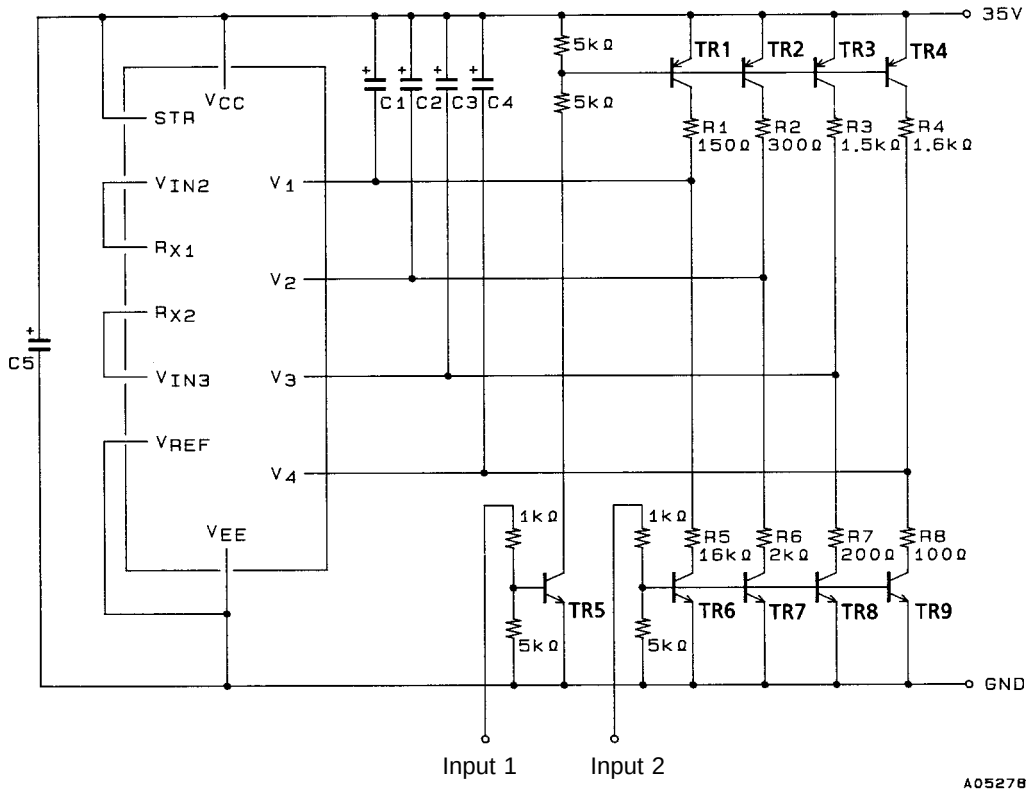


Block Diagram



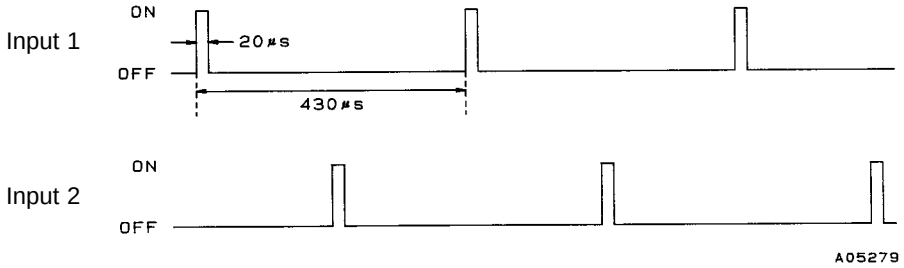
(The voltages $V_{RX}1$, $V_{RX}2$, $V_{RX}3$, and $V_{RX}4$ must obey the relationship $V_{RX}1 \geqq V_{RX}2 \geqq V_{RX}3 \geqq V_{RX}4$).

Maximum Output Current Load Test Conditions

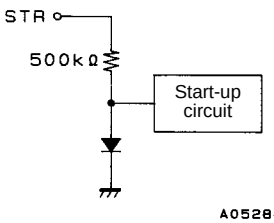


$V_{CC} - V_{EE}$ = 35 V R_X = 8 R C1 to 4 = 10 µF C5 = 33 µF R: 1 W or more
TR1 to 4: 2SA984 E or F rank
TR5 to 9: 2SC2274 E or F rank

The output load resistor values (R1 to R8) are set so that when an ''on'' level signal is input to inputs 1 and 2, a current of 15 to 30 mA max. flows to the sink side and the source side (approximately 2 mA on the V1 source side).

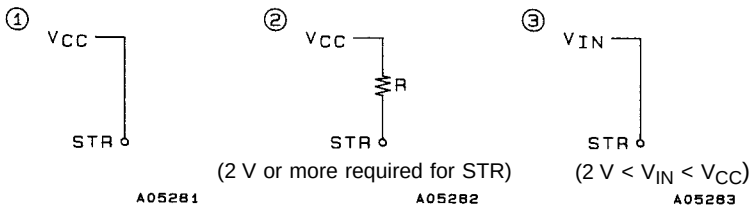


STR Pin Usage

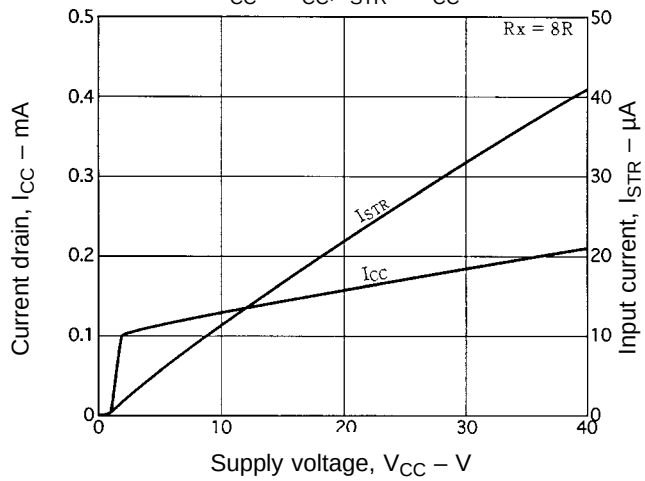


The STR input is configured as shown left.

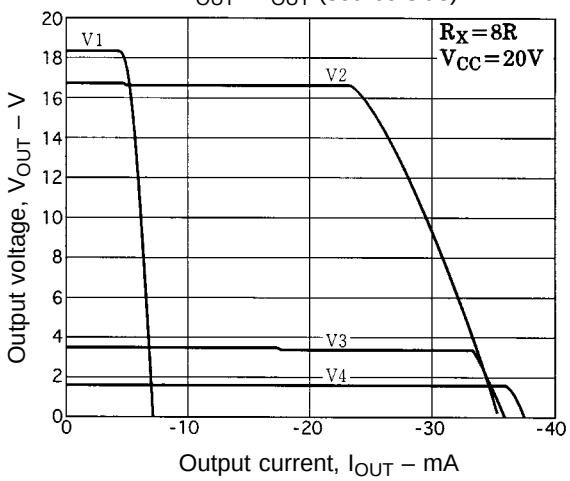
- The STR is either shorted with V_{CC} or connected to V_{CC} via an external resistor.
- It is possible to use a separate power supply (V_{IN}) such that 2 V < V_{IN} < V_{CC} for current saving.



I_{CC} – V_{CC}, I_{STR} – V_{CC}



V_{OUT} – I_{OUT} (source side)



V_{OUT} – I_{OUT} (sink side)