Ordering number : ENA0205

SANYO Semiconductors
DATA SHEET

Monolithic Linear IC

LA1654C — Time Code Reception IC

Overview

The LA1654C time code reception IC receives long-wave time standard broadcasts (such as the Japanese JJY and German DCF77 standards) and detects and outputs the time code superposed on the long-wave signal. Applications can automatically correct their clock's time setting by using the time code received by the LA1654C. Note that the LA1654C is a bare chip product that is not packaged.

Functions

- RF amplifier, rectifier, detector, time code output, and standby circuit.

Features

- Low-voltage operation (operating V_{CC} as low as 1.5V).
- Standby mode current drain less than or equal to 0.05μA.
  Japan : JJY 40/60kHz
  Germany : DCF77 77.5kHz

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		5.0	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	10	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-40 to +125	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Recommended supply voltage	V_{CC}		1.5		3.0	V
Operating supply voltage range	V_{CC} op		1.1		3.6	V

SANYO Semiconductor Co., Ltd.
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Operating Characteristics at Ta = 25°C, V_{CC} = 3.0V

* : Packaged in a VSON16 package and measured using the SON11T016-001-MF socket (Yamaichi Electronics Co., Ltd.)

Overall Characteristics

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current	I_{CCO}	No input, PAD15 = 0V, PAD10 = 3V	30	37	50	μA
Standby mode current drain	I_{STB}	PAD15 = 3.0V			0.05	μA

AGC Amplifier Input Characteristics

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input impedance	Z_I	PAD1		800		kΩ
Input frequency range	F_{IN}	PAD1	37.5		80.0	kHz
Minimum input voltage	V_{MIN}	PAD1 input level			1	μVrms
Maximum input voltage	V_{MAX}	PAD1 input level	100			mVrms

TCO Output Characteristics - Input signal = PAD1, fin = 40kHz, PAD10 = 3V, PAD15 = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
High-level output voltage	V_{OH}	PAD11 output level	2.9		3.0	V
Low-level output voltage	V_{OL}	PAD11 output level	0		0.1	V
Output pulse width (500 ms input)	T500	V_{IN} = 0 to 100dBμV, AM modulation (1Hz square wave, duty = 50%, 10:1 modulation)	400	520	600	ms
Output pulse width (800 ms input)	T800	V_{IN} = 0 to 100dBμV, AM modulation (1Hz square wave, duty = 80%, 10:1 modulation)	600	730	800	ms
Output pulse width (200 ms input)	T200	V_{IN} = 0 to 100dBμV, AM modulation (1Hz square wave, duty = 20%, 10:1 modulation)	200	300	400	ms

STB Control Characteristics

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Standby on voltage	V_{SH}	PAD15 DC voltage	2.9		3.0	V
Standby off voltage	V_{SL}	PAD15 DC voltage	0		0.1	V
High-level pin input current	I_{SH}	PAD15 = 3V			0.1	μA
Low-level pin input current	I_{SL}	PAD15 = 0V			0.3	μA

HOLD Control Characteristics - PAD15 = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Hold on voltage	V_{HL}	PAD10 DC voltage	0		0.1	V
Hold off voltage	V_{HH}	PAD10 DC voltage	2.9		3.0	V
High-level pin input current	I_{HH}	PAD10 = 3V			0.1	μA
Low-level pin input current	I_{HL}	PAD10 = 0V			0.3	μA

Chip Specifications

Parameter	Conditions	Ratings	Unit
Chip size		1.26×2.00	mm^2
Chip thickness		330(±20)	μm
Pad size		127.5×127.5	μm^2
Pad opening		105×105	μm^2

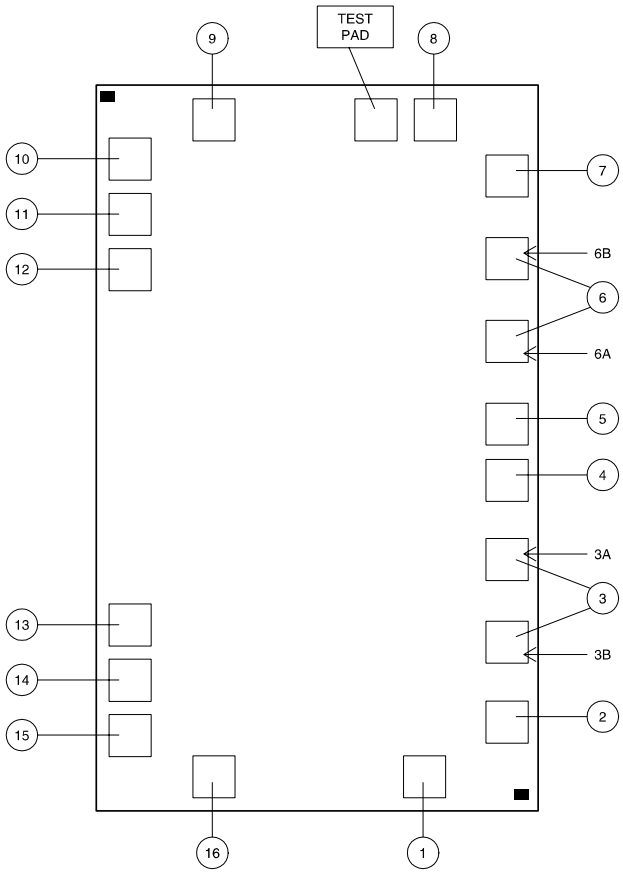
PAD Coordinates

PAD	X-Axis	Y-Axis	PAD	X-Axis	Y-Axis
P1	902	151	TEST PAD	776.5	1849
P2	1109	299.5	P9	368.5	1849
P3A	1109	717.5	P10	151	1747
P3B	1109	508.5	P11	151	1600
P4	1109	926.5	P12	151	1453
P5	1109	1073.5	P13	151	547
P6A	1109	1282.5	P14	151	400
P6B	1109	1491.5	P15	151	253
P7	1109	1700.5	P16	368.5	151
P8	926	1849			

Notes

1. The left upper corner of the Pad Layout Diagram on the following page is the origin, the X axis increases to the right and the Y axis increases in the downward direction.
2. Units : μm
3. The pad coordinates give the coordinate values of the center of the pads.
4. Both of each of the pairs P3A/P3B (V_{CC}) and P6A/P6B (ground) must be bonded.
5. The test pads must not be connected (NC).

Pad Layout Diagram



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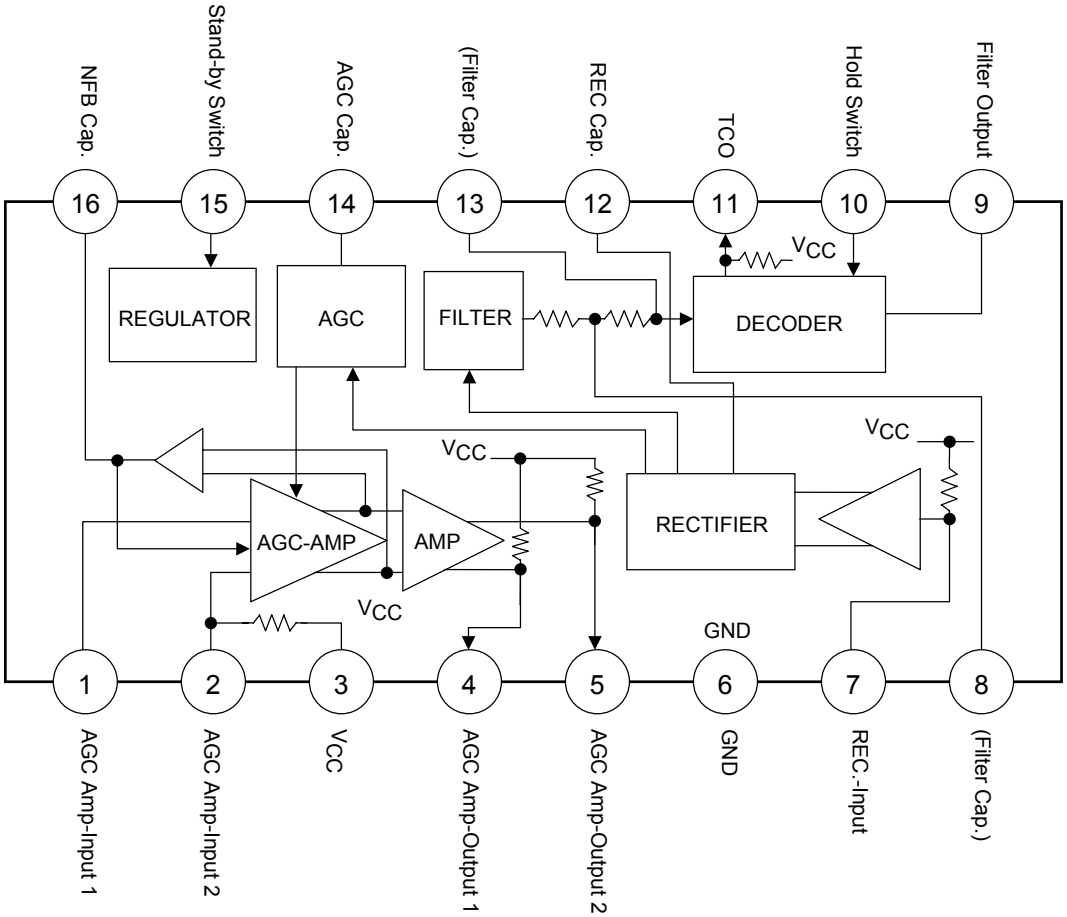
Block Diagram



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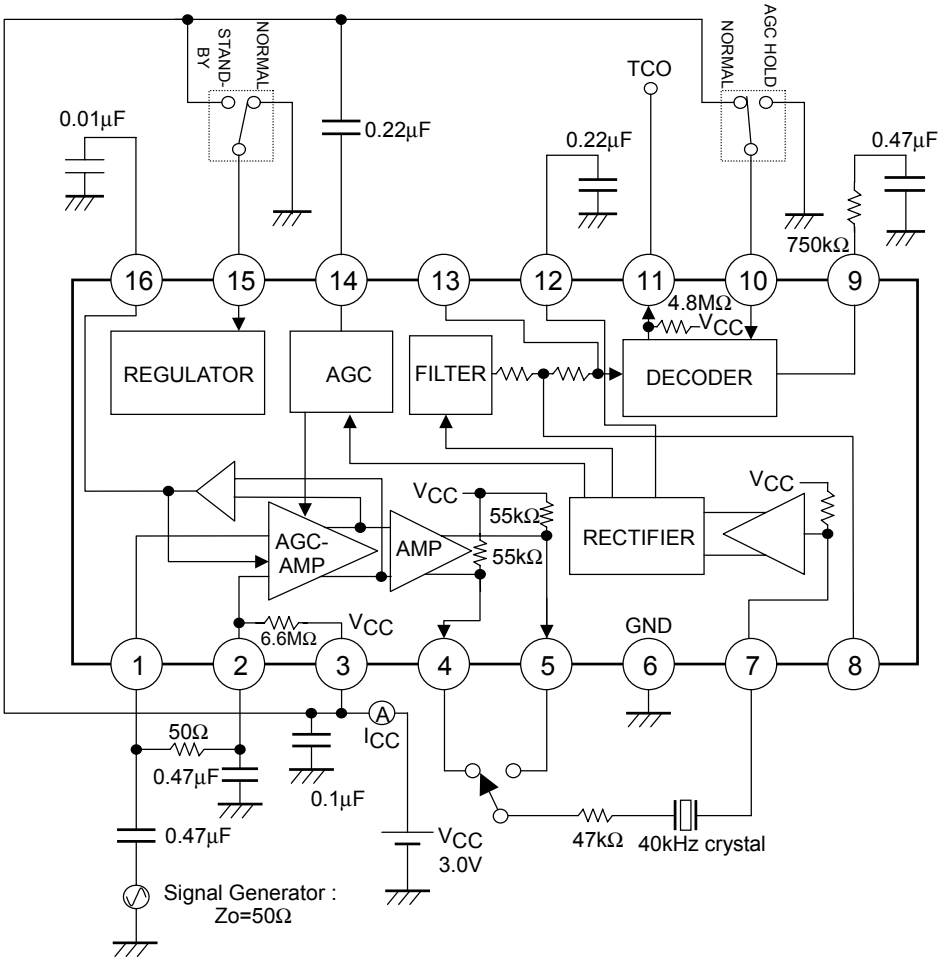
Test Circuit Diagram



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