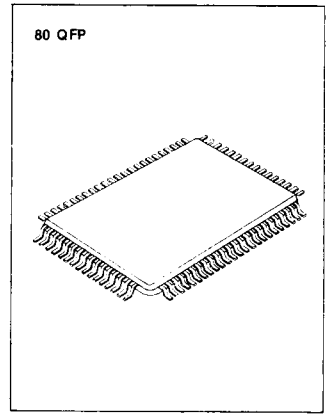
DIGITAL SIGNAL PROCESSOR

The KS9210 which is CDP DSP IC improved digital filter characteristic includes digital audio output to interface other system directly.



FEATURES

- **EFM Phase detector circuit**
- **EFM data demodulator**
- **Include sync frame detection, protection, and injection circuit**
- **Correction of C1, C2 error**
- **Interpolator**
- **Subcode data processor**
- **CLV-servo controller**
- **Tracking counter**
- **μ-com interface**
- **Digital filter (Linear-phase FIR)**
- **S-RAM address generator**
- **16K SRAM**
- **Digital Audio out**
- **1.2μm CMOS process**

ORDERING INFORMATION

Device	Package	Operating Temperature
KS9210	80 QFP	−20°C ~ +75°C

BLOCK DIAGRAM

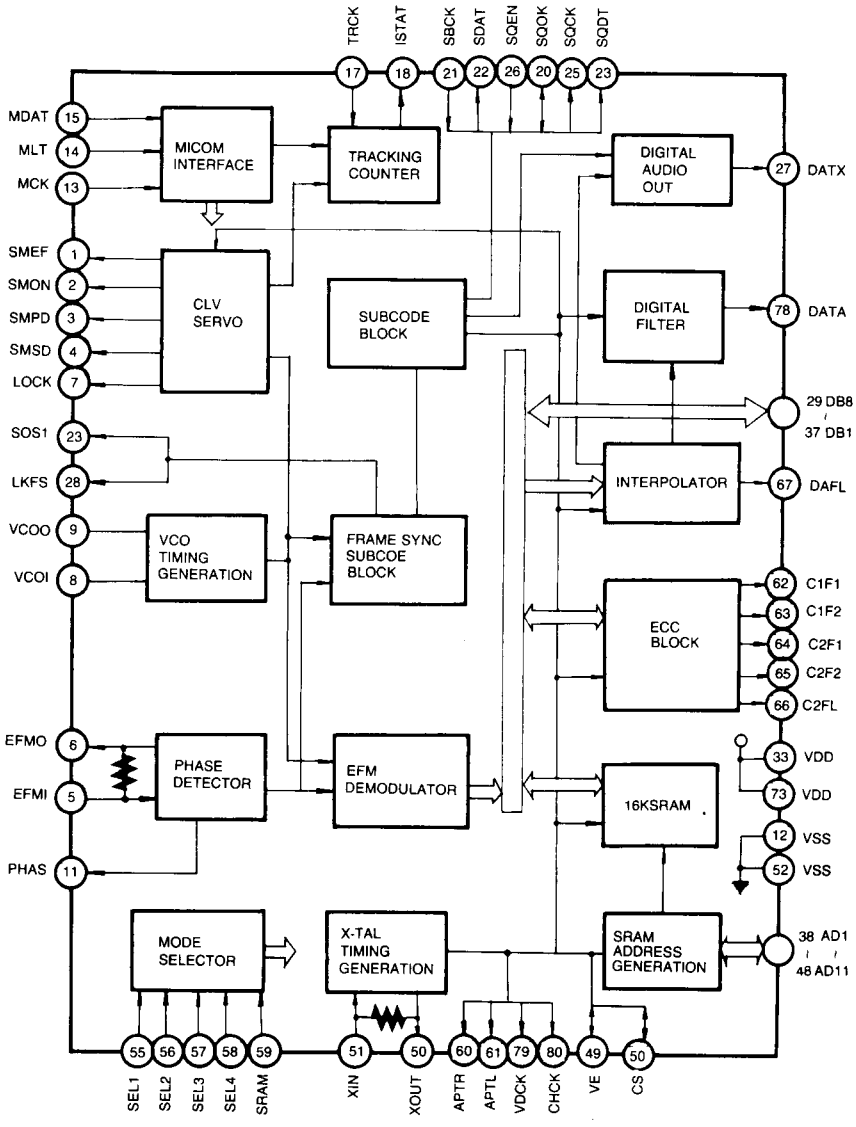


Fig. 1

PIN CONFIGURATION

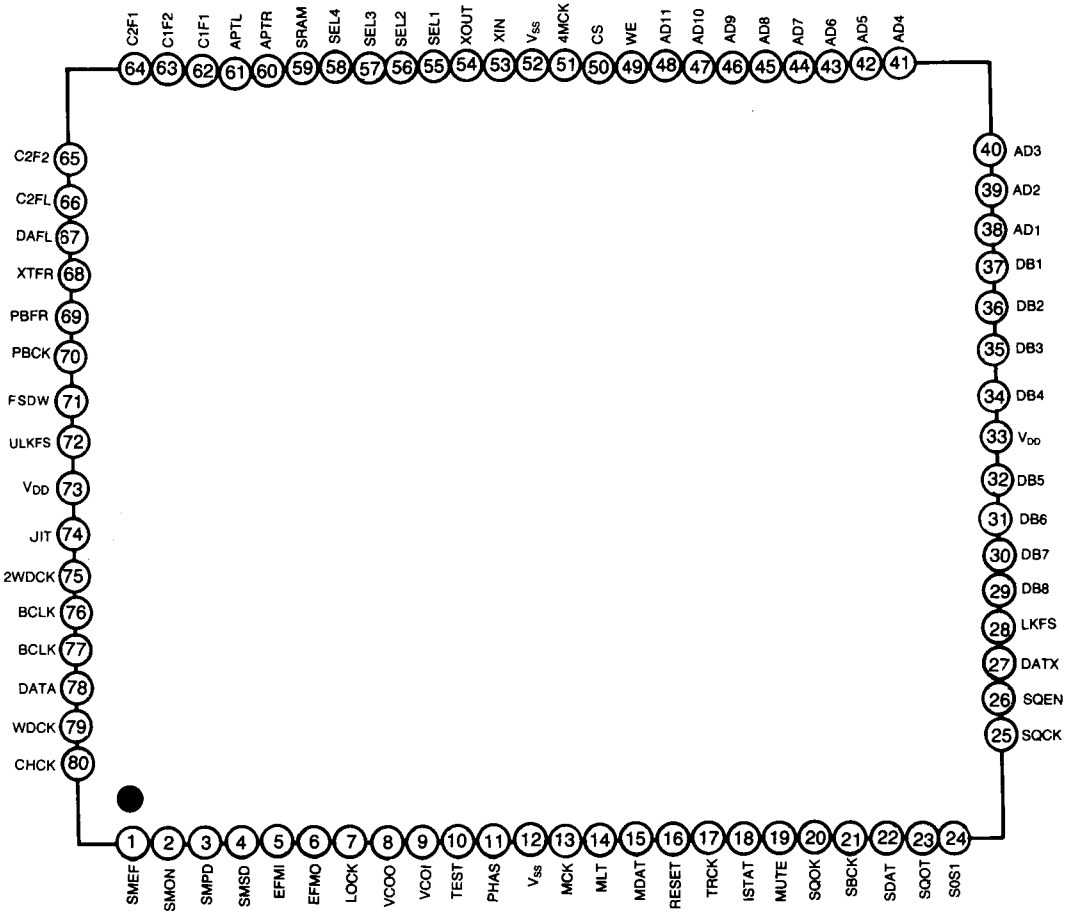


Fig. 2

PIN DESCRIPTION

Pin No	Symbol	I/O	Description
1	SMEF	O	LPF time constant control signal of the spindle motor error signal
2	SMON	O	On/Off control signal for the spindle motor
3	SMPD	O	Spindle motor drive, (Rough control in the S-Mode, phase control in the P-Mode)
4	SMSD	O	Spindle motor drive. Velocity control in the P-Mode
5	EFMI	I	EFM signal input terminal
6	EFMO	O	Slice level control signal of EFM signal
7	LOCK	O	Output signal of LKFS conditions sampled $\frac{PBFR}{16}$ (if LKFS is 'H', Lock is 'H'. If the LKFS is sampled "L" at test 8 times by $\frac{PBFR}{16}$, Lock is 'L')
8	V_{COO}	O	V_{CO} Output, when PBFR is locked the frequency is 8.6436 MHz
9	V_{COI}	I	V_{CO} Input
10	TEST	I	Momal operating is 'L', TEST is 'H'
11	PHAS	O	Phase comparison output signal between EFM and $V_{COI}/2$
12	V_{SS}	—	Ground
13	MCK	I	DATA Transportation clock from μ-com
14	MLT	I	LATCH CLOCK from μ-com
15	MDAT	I	DATA from μ-com
16	RESET	I	System reset at 'L'
17	TRCK	I	Tracking counter input pulse signal
18	ISTAT	O	Output internal condition as designated by address
19	MUTE	I	Muting input
20	SQOK	O	Output the CRC check result of sub mode Q Data
21	SBCK	I	Clock signal to output Subcode Data
22	SDAT	O	Serial output of Subcode Data
23	SQDT	O	Output of Subcode Q Data
24	S0S1	O	Output of Subcode Sync Signal (S0 + S1)
25	SQCK	I/O	Clock to output Subcode Q Data
26	SQEN	I	SQCK I/O selection terminal ('L': SQCK output, 'H': SQCK input)
27	DATX	O	Digital Audio Output
28	LKFS	O	Output the Lock Conditions of frame sync
29	DB8	I/O	CMSB
~	~	~	Hi-2 at the normal operating (TEST = "L", SRAM = "L")
32	DB5	I/O	Data In/output at SRAM TEST
33	V_{DD}	—	+5V
34	DB4	I/O	
~	~	~	
37	DB1	I/O	(LSB)

4

PIN DESCRIPTION (Continued)

Pin No	Symbol	I/O	Description
38	AD1	I/O	(LSB) Hi-2 at the normal operating (TEST = 'L', SRAM = 'L')
~	~	~	in/output at test (TEST = 'H', SRAM = 'H')
48	AD11	I/O	(MSB)
49	WE	I/O	Hi-Z output at the normal operating, and Write enable input at the SRAM test
50	CS	I/O	Hi-Z output at the normal operating Chip enable input at the SRAM test
51	4MCK	O	Divider output of X_{IN} f = 4.2336 MHz
52	V_{SS}	—	Ground
53	X_{IN}	I	Input terminal of crystal oscillation circuit. According to mode, f = 8.4672 MHz or 16.9344 MHz
54	X_{OUT}	O	Output terminal of crystal oscillation circuit
55	SEL1	I	Mode selection terminal 1
56	SEL2	I	Mode selection terminal 2
57	SEL3	I	Mode selection terminal 3
58	SEL4	I	Mode selection terminal 4
59	SRAM	I	Normal operating = 'L', TEST = 'H'
60	APTR	O	Output to compensate R-CH Aperture ('H' = R-CH)
61	APTL	O	Output to compensate L-CH Aperture ('H' = L-CH)
62	C1F1	O	Output when SEL4 is 'L'
63	C1F2	O	Output when SEL4 is 'L'
64	C2F1	O	Output when SEL4 is 'L'
65	C2F2	O	Output when SEL4 is 'L'
66	C2FL	O	Output when SEL4 is 'L'
67	DAFL	O	Output when SEL4 is 'L'
68	XTFR	O	Output when SEL4 is 'L'
69	PBFR	O	Output when SEL4 is 'L'
70	PBCK	O	Output when SEL4 is 'L'
71	FSDW	O	Output when SEL4 is 'L'
72	ULKFS	O	Output when SEL4 is 'L'
73	V_{DD}	—	+ 5V
74	JIT	O	Output when SEL4 is 'L'
75	2WDCK	O	Output when SEL4 is 'L'
76	BLCK	O	Output when SEL4 is 'L'
77	BLCK	O	Output when SEL4 is 'L'
78	DATA	O	Output when SEL4 is 'L'
79	WDCK	O	Strobe signal digital filter on = 176.4 KHz off = 88.2 KHz
80	CHCK	O	Strobe signal digital filter on = 88.2 KHz off = 44.1 KHz

Notes) 1. XTFR : 7.35 KHz frame sync signal made by X'tal.
2. PBFR : 7.35 KHz frame sync signal of PLAY BACK made by DATA which being reproduced.
3. $\overline{\text{PBCK}}$: Channel bit clock of DATA which being reproduced.
$\frac{V_{COI}}{2}$ at the normal mode.
4. FSDW : Unprotected frame sync.
5. ULKFS : FRAME sync protection condition.
6. $\overline{\text{JIT}}$: Display of either RAM overflow or underflow for ± 4 frame jitter margin.
7. 2WDCK : Strobe signal
Digital filter On = 352.8 KHz
Off = 176.4 KHz
8. BLCK : BIT CLOCK Output signal. Digital filter On = 4.2336 MHz
Off = 2.1168 MHz

4

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 ~ +7	V
Input Voltage	V_I	−0.3 ~ +7	V
Output Voltage	V_O	−0.3 ~ +7	V
Operating Temperature	T_{OPR}	−20 ~ +75	°c
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input High Voltage	V_{IH1}	Note 1	0.7V_{DD}		V_{DD}	V
Input Low Voltage	V_{LH1}	Note 1	0		0.3V_{DD}	V
Input High Voltage	V_{IH2}	Note 2	0.8V_{DD}			V
Input Low Voltage	V_{LH2}	Note 2			0.2V_{DD}	V
Output High Voltage	V_{OH}	I_{OH} = −1mA	V_{DD} − 0.5		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 1mA	0		0.4	V
Input Leakage Current	I_{LKG}	V_{IN} = 0 ~ 5.5V			±5	μA
Three State Pin Output Leakage Current	I_{LKG}	V_{OUT} = 0 ~ 5.5V			±5	μA

Note 1. Related Pins – EFMI, RESET, TEST, MUTE, SEL 2 – 5, MLT, MDAT, SQEN. SQCK.
Note 2. Related Pins – TRCK, MCK, SRAM

2. AC Characteristics

A. X_{IN} and V_{COI} terminal

(V_{DD} = 5V ± 10%, V_{SS} = 0V, T_{OPR} = 0 ~ +70°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillation Frequency	f_{OSC}				18	MHz

B. Pins MCK, MDAT, MLT, TRCK, SQCK
(V_{DD} = 5.0V ± 10%, V_{SS} = 0V, T_{OPR} = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Clock Frequency	f_{CK1}			1	MHz
Clock Pulse Width	t_{WCK1}	300			nS
Set Up Time	t_{SU}	300			nS
Hold Time	t_H	300			nS
Delay Time	t_D	300			nS
Latch Pulse Width	t_W	300			nS
TRCK, SQCK frequency	t_{CK2}			1	MHz
TRCK, SQCK Frequency, Pulse Width	t_{WCK2}	300			nS

C. D/Ā Converter Interface Terminal
(Pins CHCK, WDCK, APTR, APTL, C1F1, C1F2, C2FL, DAFL, XTFR, 2WDCK, DATA)

Item	Symbol	DF OFF			DF ON			Unit
		Min	Typ	Max	Min	Typ	Max	
Clock Pulse Width	t_{WCK}		236			118		nS
Clock Skew (FAST)	t_{FCK}			40			40	nS
DATA Skew (FAST)	$t_{F\,(SK)}$			0			0	nS
DATA Skew (Delay)	$t_{D\,(SK)}$			8			80	nS

APPLICATION INFORMATION

1. MODE SELECTOR

SEL1	SEL2	SEL3	SEL4	SRAM	XIN	BO	DF	DAC		AUDIO /ROM	16KSRAM
								P/S	2S/OB		
O	O	O	O	O	16M	ON	ON	S	2S	AUDIO	internal
O	O	O	I	O	↓	↓	↓	P	OB	↓	↓
O	O	I	O	O	↓	↓	OFF	S	2S	↓	↓
O	I	O	O	O	↓	OFF	ON	↓	↓	↓	↓
O	I	O	I	O	↓	↓	↓	P	OB	↓	↓
O	I	I	O	O	↓	↓	OFF	S	2S	↓	↓
O	I	I	I	O	↓	↓	↓	P	OB	↓	↓
I	O	O	O	O	8M	↓	ON	S	2S	↓	↓
I	O	O	I	O	↓	↓	↓	P	OB	↓	↓
I	O	I	O	O	↓	↓	OFF	S	2S	↓	↓
I	O	I	I	O	↓	↓	↓	P	OB	↓	↓
I	I	I	O	O	16M	ON	↓	S	2S	↓	↓
I	I	I	I	O	8M	OFF	↓	↓	↓	ROM	↓

1) X_{IN} is the input terminal of crystal oscillator.
   16M = 16.9344 MHz, 8M = 8.4672 MHz
2) DF is internal digital filter
   On condition: Output the data after pass by filter
   Off condition: The opposite of ON condition
   DO shows digital audio out
3) S of DAC is outputed serially to PAD 78 and 2S is 2's complement.
   OB is OFFSET BINARY and shows inversed MSB.
4) When SRAM is 'L', use internal SRAM.
5) Audio use Audio Application and ROM use CD-ROM application in the Audio/ROM.

2. μ-Com Interface

The DATA inputed from μ-Com is inputed to MDAT and transfered by MCK.
The signal is inputed to MLT terminal in order that the data inputed is loaded to one of six control register.

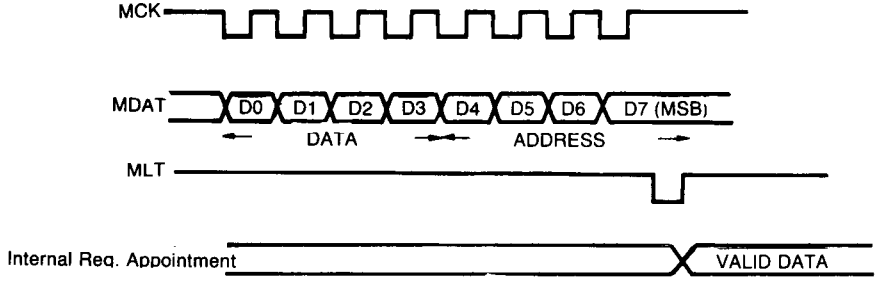


Fig. 3 μ-COM DATA INPUT TIMING CHART

CONTROL REGISTER	COMMENT	ADDRESS D7 ~ D4	DATA D3	DATA D2	DATA D1	DATA D0	JSTAT TERMINAL
CNTL-Z	DATA CONTROL	1001	ECMT	HIPD	NCLV	CRCD	Hi-Z
CNTL-S	FRAME SYNC PROTECTION ATTENUATION CONTROL	1010	FSEM	FSEL	WSEL	ATTM	Hi-Z
CNTL-L	TRACKING COUNTER LOWER 4 BIT	1011	TRC3	TRC2	TRC1	TRC0	$\overline{\text{COMPLETE}}$
CNTL-U	TRACKING COUNTER UPPER 4 BIT	1100	TRC7	TRC6	TRC5	TRC4	$\overline{\text{COUNT}}$
CNTL-W	CLV CONTROL	1101	COM	WB	WP	GAIN	Hi-Z
CNTL-C	CLV MODE	1110	CLV-MODE				$\overline{\text{PW}} \geqq 64$

Table 1. Control Register Selection μ-Com Data

1) CNTL-Z REGISTER

It is a register to control zero cross mute of audio data, phase terminal, control signal of phase servo, and have or not of CRCF DATA in SQDT.

		DATA = 0	DATA = 1
ZCMT	D3	Zero cross mute is off	ON
HIPD	D2	It operate PHAS normally	LKFS became "L" to "Hi-Z"
NCLV	D1	Phase servo being acted by frame sync	Phase servo being acted by base counter
CRCQ	D0	SQDT output except SQOK	SQDT is CRCF during rising time

2) CNTL-S Register

It is a register to control FRAME SYNC, PROTECTION, ATTENUATION.... etc.

FSEM	FSEL	FRAME
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	CLOCK
0	±3
1	±7

ATTM	MUTE	dB
0	0	0
0	1	$-\infty$
1	0	-12
1	1	-12

3) CNTL-L, U REGISTER

After the number of track that must be counted is inputed from μ-com, The Data is loaded to tracking counter by CNTL-L, U register

4) CNTL-W Register

		DATA = 0	DATA = 1	Comments
COM	D3	XTFR/4 & PDFR/4	XTFR/4 & PBFR/4	Phase comparative frequency control during phase-mode
WB	D2	XTFR/32	XTFR/16	Bottom hold period control during speed, or H speed-mode
WP	D1	XTFR/4	XTFR/2	PEAK hold period control during speed-mode
GAIN	D0	-12dB	0dB	SMPD gain control during speed, or H speed-mode

5) CNTL-C Register

MODE	D7 ~ D4	D3 ~ D0	SMDP	SMSD	SMEF	SMON
FORWARD		1000	H	Hi-Z	L	H
REVERSE		1010	L	Hi-Z	L	H
SPEED		1110	SPEED	Hi-Z	L	H
HSPEED	1110	1100	HSPEED	Hi-Z	L	H
PHASE		1111	PHASE	PHASE	Hi-Z	H
XPHSP		0110	SPEED, PHASE	Hi-Z, PHASE	L, Hi-Z	H
VPHSP		0101	SPEED	Hi-Z, PHASE	L, Hi-Z	H
STOP		0000	L	Hi-Z	L	L

3. Tracking Counter

This block used for track jump perform that the data, which must be jumped, inputed from μ-Com is loaded to CNTL-L, U at rising edge. Loaded Data is starting the count by tracking counter clock track, if CNTL-L is selected COMPLETE signal is outputed to $\overline{\text{ISTAT}}$ terminal, and if CNTL-U is selected, $\overline{\text{COUNT}}$ signal is outputed to.
When CNTL-L reg is selected, if the pulse width of bottom hold exceed 64T (T: a period of PBFS) 'L' is outputed to $\overline{\text{ISTAT}}$ terminal. The result is detected after reverse command is inputed from μ-com and is that the speed of spindle motor reduce.
The following is timing chart of tracking counter block.

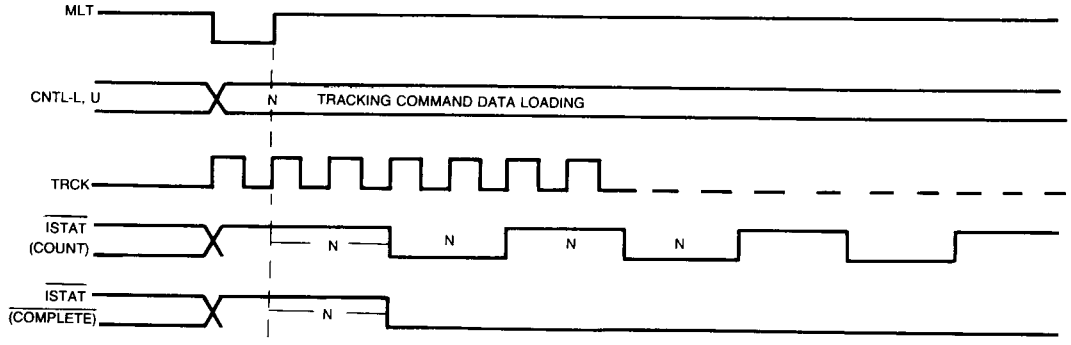


Fig. 4 Tracking Count Timing Chart

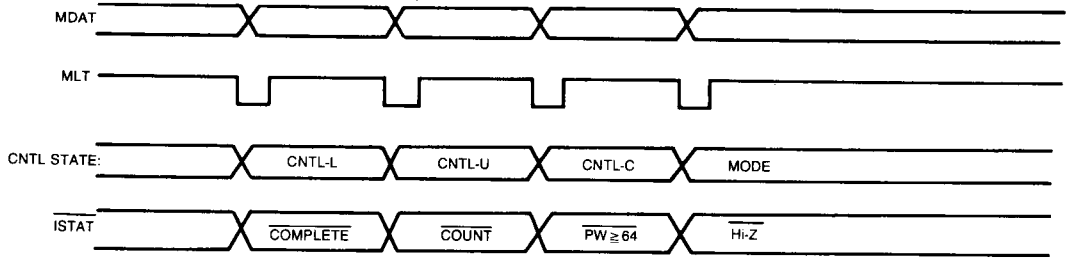


Fig. 5 CNTL Reg. According to Output Signal of $\overline{\text{ISTAT}}$

1) Block Diagram

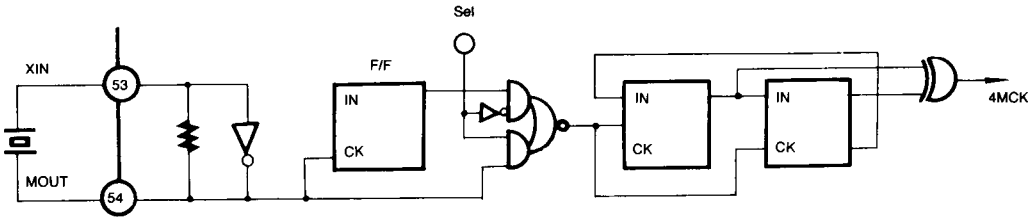
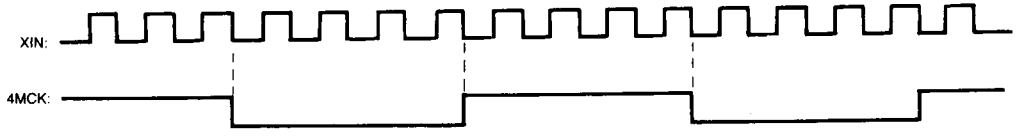
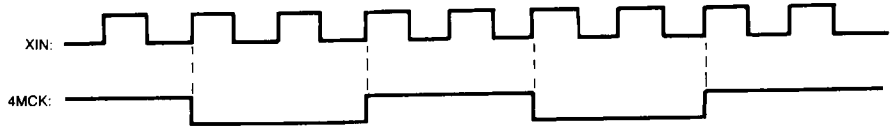


Fig. 6 X'tal OSC Block Diagram

2) Using the X'tal osc of 16.9344 MHz, Timing Chart (Sel = 0)



3) Using the X'tal osc of 8.4672 MHz, Timing Chart (Sel = 1)



5. EFM

EFM consist of EFM demodulator which demodulate EFM DATA inputed from the Disk, EFM phase detector, frame sync detector/protector/inserter, subcode sync detector, and controller which controls EFM block .... etc.

1) EFM Phase Detector

As EFM inputed from disk includes the component of 2.11 MHz, EFM Phase Detector generate the bit clock (PBCK) of 4.32 MHz to detect the phase of this signal.
This PBCK detects the phase at the edge of EFM signal and the result is outputed to phase terminal.

A. At normal operating

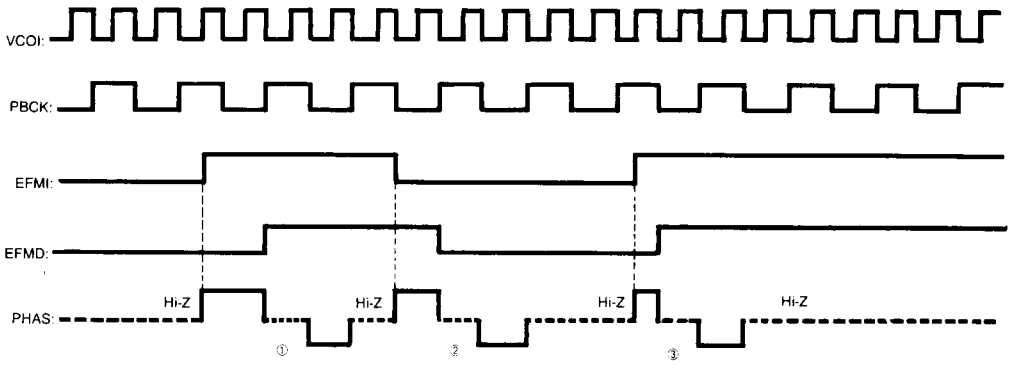


Fig. 7 EFM Phase Detection Timing Chart

In case of ①: when EFM signal is slow than VCO
In case of ②: when EFM signal is locked with VCO
In case of ③: when EFM signal is faster than VCO

B. At abnormal operation
If HIPD of CNTL-2 is selected "L" by μ-com EFM phase detector operates like (Figure 5)
If HIPD is 'H' and 'L' of LKFS is shorter than 3.5T (a period of PBFS is T)
Hi-Z is outputed to PHAS terminal as many as 'L' and be over 3.5T, Hi-Z is outputed as many as 3.5T

2) EFM Demodulator

Modulated 14 Bit DATA is inputed into NRE-I circuit in the DSP.
The 14 bit DATA through the circuit changes demodulated 8 bit DATA as NRE-I circuit convert 14 bit EFM data to 8 bit data. Demodulated DATA have two kind of signal, the one is subcode data and the other is PCM data, and that one is inputed into subcode block and this one is written in the 16K SRAM by CE and WE signal.

3) FRAME SYNC DETECTOR INSERTER/PROTECTOR

a. Frame sync detector

The Data consist of PRAME units, that is, it consist of frame sync, subcode data, PCM data, redundancy data..... etc.
The frame sync is detected by one per frame unit

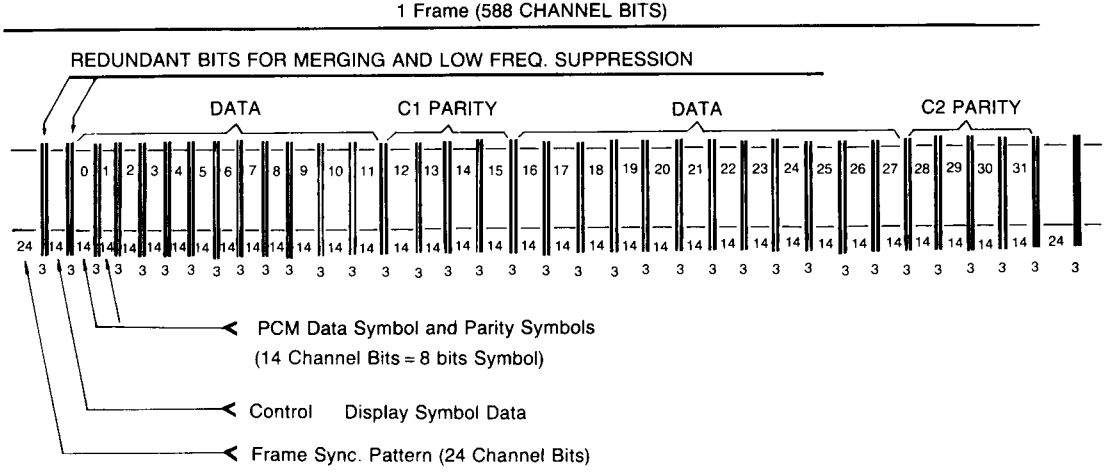


Fig. 8 (Frame Format)

B. Frame sync protector/inserter

Frame sync is omitted or detected in the place where it don't exist by the effect of ERROR or JITTER on the disk. In these cases, we need to insert or protect the signal.
The window is made by using the WSEL signal to protect the Frame Sync.
The frame sync inputed to window is ture data, and don't inputed is ignored.
A width of window is determined by WSEL of CNTL-S Reg.
If frame sync didn't be detected in the FRAME SYNC PROTECTION WINDOW, frame sync made by EFM Block is inserted in case of the sync is inserted sequencely. When the appointed number of FRAMEs is achieved by FSEM, FSEL of CNTL-S Reg, the ULKFS becomes "L" and FRAM SYNC PROTECTION WINDOW is ignored.
FRAME SYNC is received absolutely at that time. When Frame Sync is received, the ULKFS signal becomes "H" and FRAME sync detected in window is received.

LKFS	ULKFS	Explanations
I	I	Accordance with PLAYBACK FRAME SYNC and generated FRAME SYNC.
O	I	① Out of accordance with PLAYBACK FRAME SYNC and generated FRAME SYNC, but PBFR SYNC is detected in the window selected by WSEL. ② Out of accordance with PBFR SYNC and XTFR SYNC, and SYNC is inserted because it don't be detected in the window selected by WSEL.
O	O	① After insertion as many as the Frame decided by FSFM and FSEL of CNTL-S Reg. as frame sync don't be detected in the window. ② In case that PBFR SYNC don't be detected.

6. Subcode

14 bit Subcode Sync Signal (this is S0, S1) is detected in the Subcode Sync.
After S0 is detected, a frame of S1 is detected.
At that time S0 + S1 signal is outputed to S0S1 terminal, and S0, S1 signal is outputed to SDAT terminal when S0S1 signal is "H".
After 14 bit subcode data becomes EFM demodulation, the 8 BIT of subcode data (P, Q, R, S, T, U, V, W) is syncronized with PBFR signal and is outputed to SDAT by SBCK CLOCK.
Among the eight subcode DATA, Q1 data is selected and loaded to the eighty shift resister by PBFR signal. The result of checking the CRC (cycle redundancy check) of roading data is syncronized with S0S1 rising edge and outputed to SQOK terminal.
If the result of checking is error.
"L" is outputed to SQOK terminal and if it is true "H" is outputed to and if the CRCD of CNTL-Z Mode is "H", the result of CRC CHECK is outputed to SQDT terminal during from S0S1, 'H' to SQCK FALLING EDGE.
The following is the timing chart of subcode block.

1) at SQEN = 'L', SDAT, SQDT, S0S1, SQOK, VCOI Timing Chart

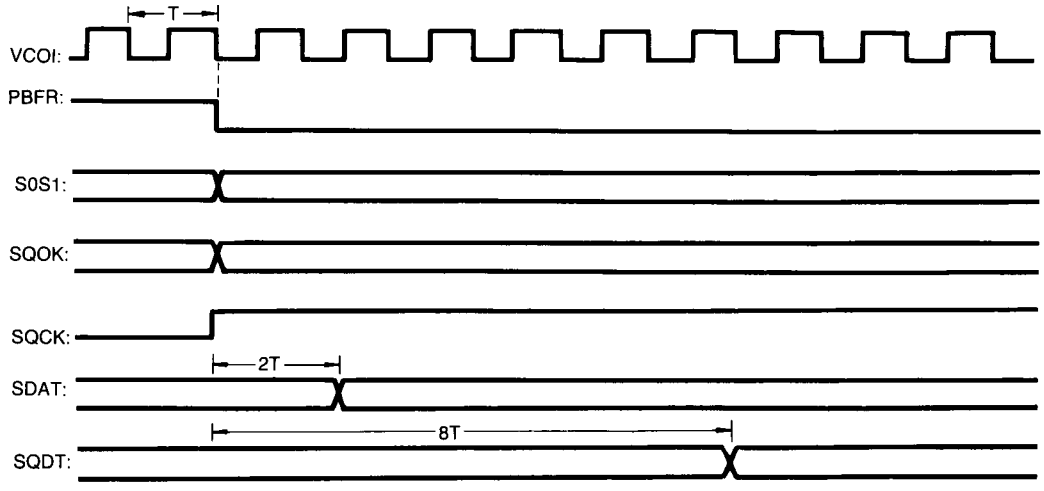


Fig. 9

2) at SQEN = 'L', SQOK, SQDT, S0S1 Timing Chart

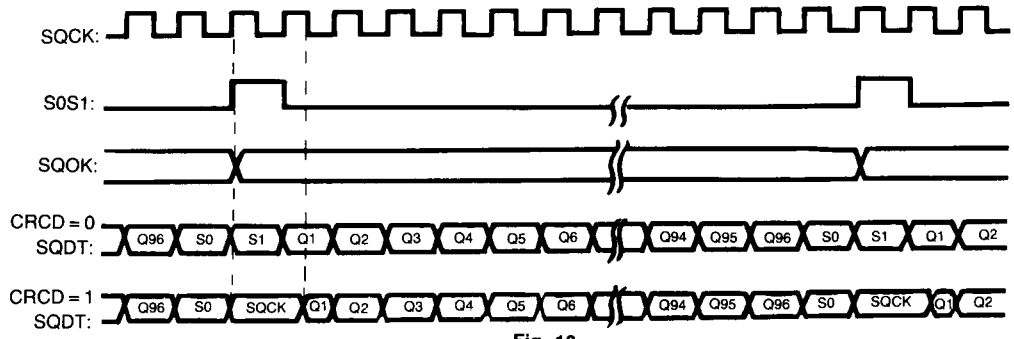


Fig. 10

3) at SQEN = 'H', SQOK, SQDT, S0S1, SQCK Timing Chart

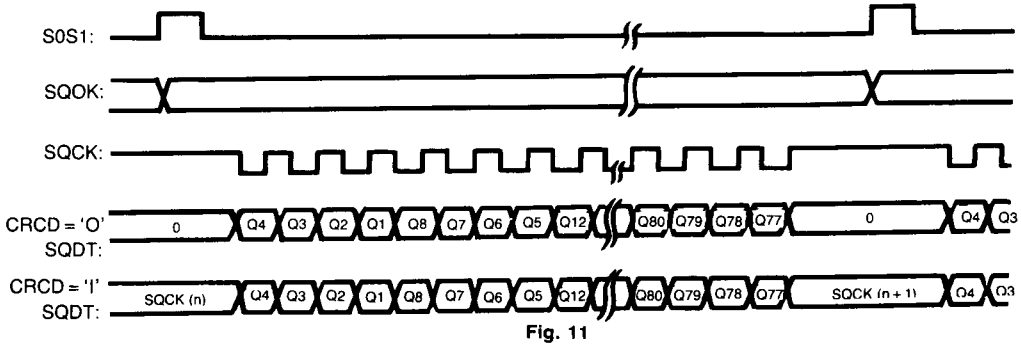


Fig. 11

Comment: If the SQOK of the subcode Q data is "H", subcode data is outputed to SQDT according to subcode, and it is "L" is outputed.

4) VCOI, SDAT, SBCK Timing Chart

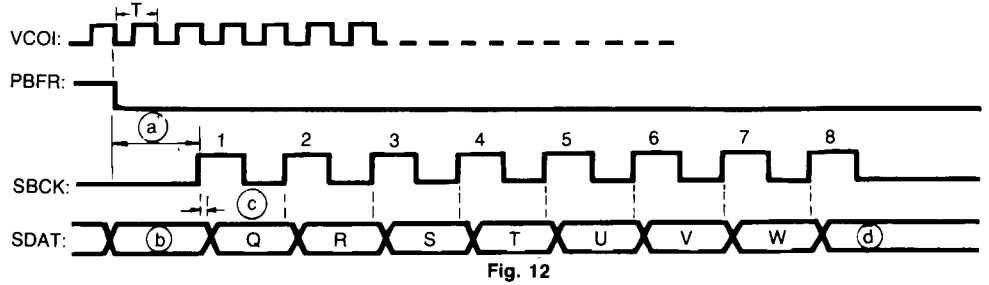


Fig. 12

a) after PBFR becomes falling edge
SBCK become "L" during about 10 sec.
b) If S0S1 is "L", subcode P is outputed and "H", S0, S1 is outputed.
c) If a period of VCOI is "T", the width of ⓒ is 4T ~ 6T.
d) If the pulse inputed to SBCK terminal be over seven, subcode data (P, Q, R, S, T, U, V, W) is repeated.

7. ECC

In case the data on the disk is damaged, ECC block corrects the damaged data.
C1 (32,28) and C2 (28,24) error is corrected by CIRC.
ECC is performed by the unit of one symbol of eight bit.
C1 pointer is generated for C1 correction, and C2 pointer is generated for C2 correction. C1, C2 send the error information of the DATA which ECC is performed.
The data which don't be corrected is showed the error data by outputing C2 FIAG.
The C2FL signal is handled in the interpolator by using the signal of C2F1 and C2F2.

C1F1	C1F2	C1C2 Error Condition	C2F1	C2F2	C2FL
O	O	No error	O	O	O
O	I	Single error correction	O	I	O
I	O	Double error correction	I	O	O
I	I	Irretrievable error	I	I	I

C1F1, C1F2: the error correct condition is outputed by C1 decoder.
C2F1, C2F2: the error correct condition is outputed by C2 decoder.
C2FL : In case that error can't be corrected by C2 decoder becomes 'H' and the reverse case becomes 'L'

8. 16K SRAM

SRAM Adress Generator and 16KSAM is built in DSP to write the data in the RAM, to read/write the data at the ECC processing, and to output the data to D/A converter after the EFM data from the disk is demodulated.
The SRAM (PAD 59) must be 'L' when the 16KSRAM is operating.

1) Address Generation Priority Control

These are processed at the same time that write when EFM is demodulated, R/W at the ECC processing at D/A converter read, the priority must be controlled. When these signals are required simultainiously the processing priority is that the first is D/A converter read, the second is EFM write, the third is ECC R/W.

2) EFM demodulation data write

When write requirement signal is send to SRAM ADDRESS GENERATOR, as the demodulated EFM DATA must be written in the SRAM, the priority is controlled and the enable signal is inputed to EFM block and the generated address is send to SRAM INTERFACE circuit.
The generated adress is a data considering deinterleave thirty-two addresses are generated in the one frame.

A. At the time being used 16K SRAM (EFM & ECC write)
- DB1 ~ DB8 is 'H'
- AD1 ~ AD11 is Hi-Z
- CE, WE don't care

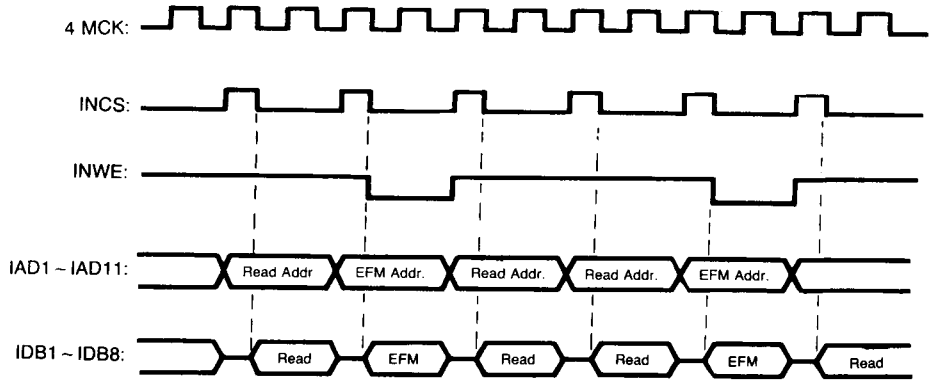
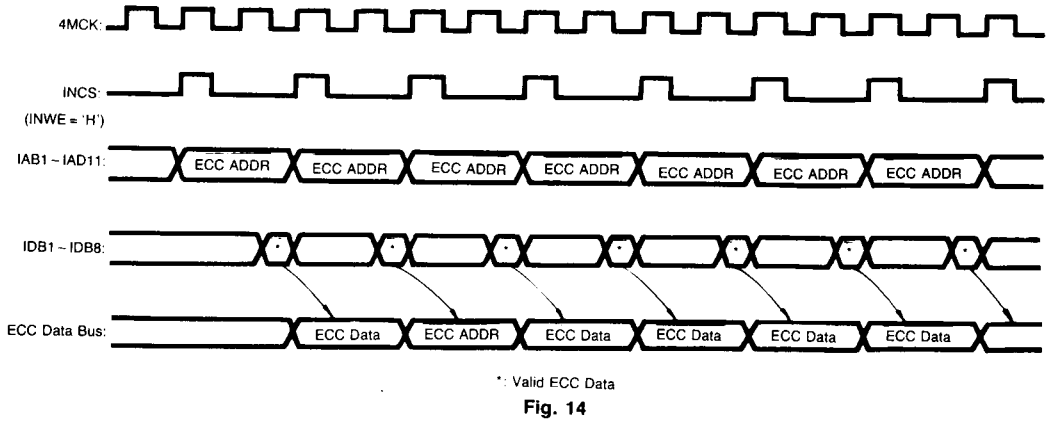


Fig. 13

3) ECC DATA R/W

At C1, C2 ECC processing, one hundred and twinty-nine address signal is generated during one frame processing as sixty-four PCM Datas and sixty-five pointer must be R/W, at ECC processing, write function is equal to 2). The following is at READ.

A. The reading time at 16K SRAM



*: Valid ECC Data

Fig. 14

4) D/A Converter Read

Thirty-six read enable signals are generated during one frame as six sampling data and twelve C2 pointer data must be read in each L, R-CH. The timing chart is equal to R/W block of ECC data for D/A converter read.
In conclusion, one hundred and seventy-nine of R/W processing action are requerd.

5) Address Generator

The Data interleaved at encode is deinterleaved at decode.
One hundred and eight frame data is needed for getting one frame of PCM data in CDP format.
Two counter is used to get data mached to CDP Format. That is, write base counter is used to write the EFM demodulated data in the SRAM, and read base counter is used to read the data in RAM.

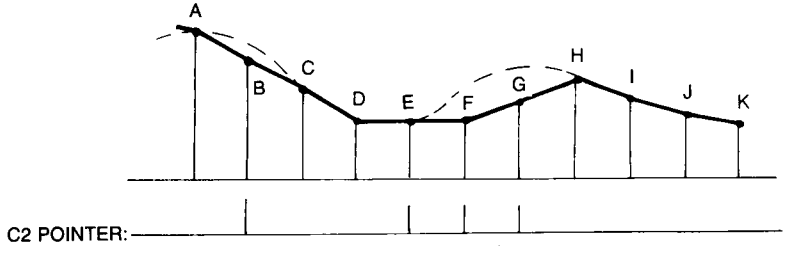
6) JITTER MARGIN

The EFM demodulated DATA is disturbed by rolling of the disk, or instability of servo system when the data is written in the SRAM. The data is distructed by time limit when the value of R/W base counter exceed ± 5 FRAME because of SRAM SIZE.
The JITTER MARGIN became less than ± 4 frame when the value of R/W base counter exceed ± 5 FRAME be due to the value of READ BASE COUNTER is loaded to the value of WRITE BASE COUNTER compulsorily.
The value of READ BASE COUNTER is loaded to the value of WRITE BASE COUNTER compulsarily when the difference of READ/WRITE BASE COUNTER exceed ± 4 frame, 'H' signal is outputed to JIT during a period of PBER.

9. Interpolator Mute

1) Interpolator

If the BURST ERROR occur on the disk although ECC process is performed, THE data can't be corrected, according to circumstance. The data is corrected by using C2 pointer of ECC in the interpolator block.
The PCM data is inputed to DATA BUS and the priority is that the first is 8 BIT C2 pointer the second is lower 8 bit, the third is upper 8 bit against each L. R-CH. When DA FLAG is 'H' takes pre hold, and in case that single error occur the average compensation method is performed with the value of PCM DATA, against a period of CHCK, when CHCK is 'L', R-CH DATA is outputed and when CHCK is 'H', L-CH DATA is outputed the timing chart of interpolator block refer to (Figure 16)



$B = \frac{A+C}{2}$: average compensation

$F = E = D$: Pre hold compensation

$G = \frac{F+H}{2}$: average compensation

Fig. 15

2) Mute, Attenuation

The audio data is muted or reduced by the ATTN signal is muting terminal and CNTL-S Reg.
The mute have two kind of muting, one is ZERO cross muting, the other is muting.

a) Zero cross muting
The audio data is muted, after ZCMT of CNTL-Z reg goes to 'H', and in case that mute is 'H' and the upper 6 bit of audio data became all 'L' or 'H'.

b) Muting
The audio data is muted in case that the ECMT of CNTL-Z Reg. is 'L' and mute terminal is 'H'.

c) Attenuation
The signal reduction is occured by ATTM of CNTL-S reg and mute signal as following.

ATTM	MUTE	
O	O	0dB
O	I	$-\infty$dB
I	O	-12dB
I	I	-12dB

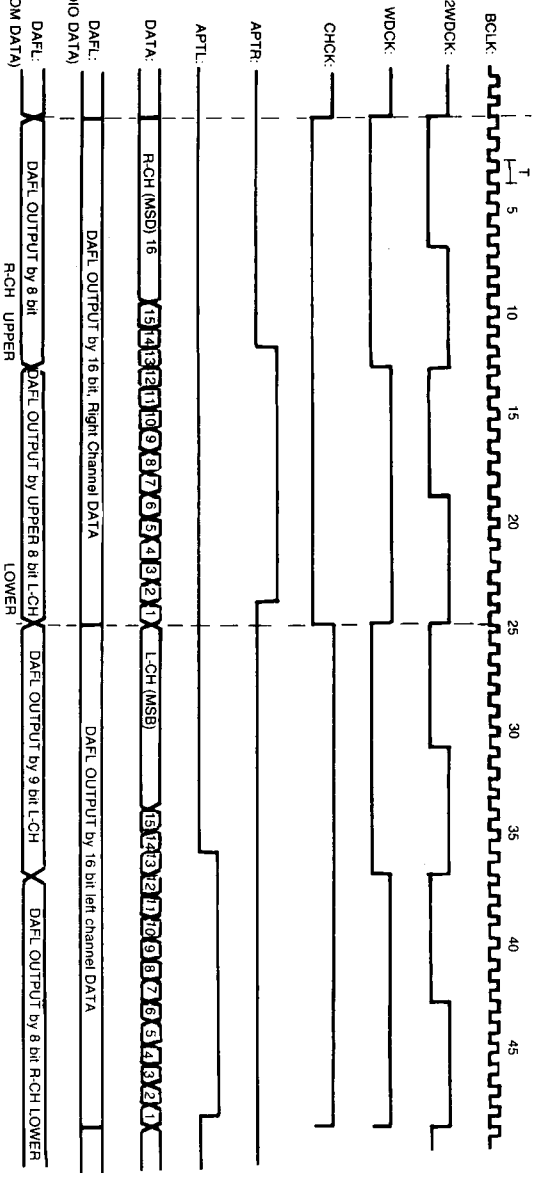


Fig. 16 The timing chart of PCM data output in case that sel 5 is 'L' and DF is off.

10. Digital Filter

The FIR (finite impulse response) digital filter is build in KS9210.
This block consist of register multiplier, S/P & P/S converter, controller.....etc.

1) Block diagram

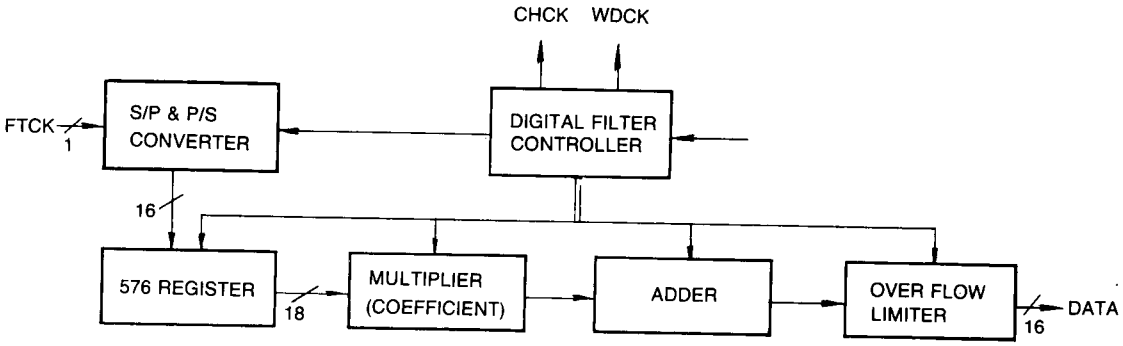
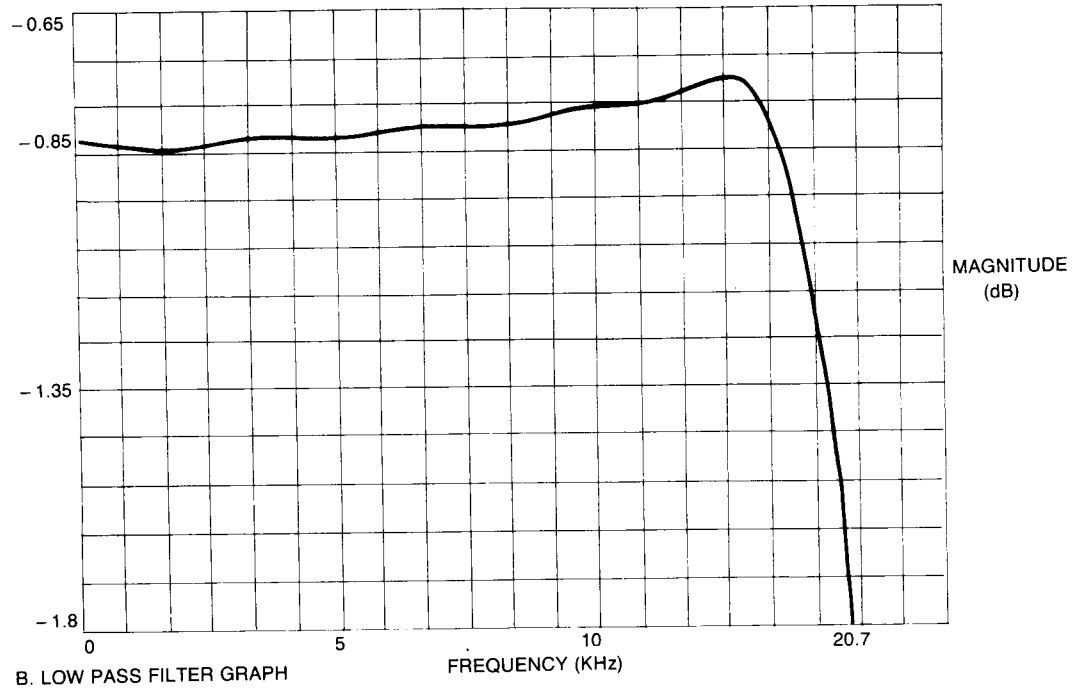


Fig. 17

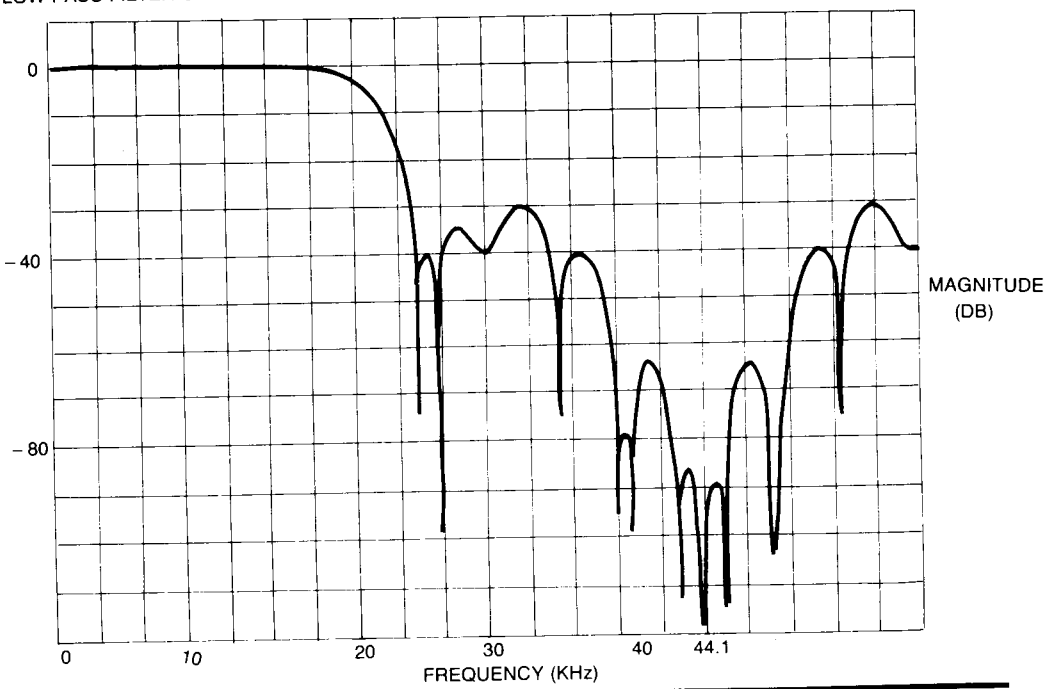
2) Specification

PASS BAND	• Ripple up to 18 KHz band • Reduction of 1 KHz in 20 KHz	±0.07 Max 0.55 Max
FILTER BAND	• Reduction of 1 KHz in 44.1±1 KHz • Reduction of 1 KHz in 44.1±5 KHz • Reduction of 1 KHz in 44.1±10 KHz • Reduction of 1 KHz in 44.1±20 KHz • −30dB frequency range of 1 KHz • −60dB frequency range of 1 KHz	91 dB Min 60 dB Min 44 dB Min 24 dB Min 44.1±20 KHz 44.1±6 KHz

A. RIPPLE GRAPH



B. LOW PASS FILTER GRAPH



11. CLV Servo

The CNTL-C Reg. is selected to control the CLV servo by Data inputed μ-Com.
The CLV servo action mode is appointed by the data inputed from μ-com to control spindle motor in CNTL-C Reg.

1) Forward
The terminal condition of output mode is that SMDP is "H", SMSD is "Hi-Z", SMEF is "L", and SMON is "H".

2) Reverse
The condition of reverse mode is that SMOP is 'L', SMSD is 'Hi-Z', SMEF is 'L', and SMOD is 'H'.

3) Speed-Mode
The spindle motor is controlled roughly by the mode when track jumping or EFM phase is unlocked.
If a period of VCO is 'T', the pulse width of frame sync is '22T'.
In case that the signal detected from EFM signal exceed '22T' by noise on the disk, ... etc., it must be removed, if not, the right frame sync can't be detected. In these case, the pulse width of EFM signal is detected by the period of XTFR/2 or XTFR/4 and the pulse width of EFM signal is detected by the period of XTFR/16 or XTFR/32.

* Peak hold clock is XTFR/2 or XTFR/4, and bottom hold clock is XTFR/16 or XTFR/32.

The detected value is used for syncronized frame signal.
If syncronized frame signal is less than 24T, the SMPD terminal outputs 'L', equal to 22T, outputs 'Hi-Z', and more than 23T, outputs 'H'.
If the gain signal of CNTL-W Reg. is 'L' the output of SMPD terminal is reduced up to – 12 dB. If it is 'H', there is no reduction. (refer to figure 7)
Output conditions SMSD = Hi-Z, SMEF = 'L', SMON = 'H'

4) Hi-Speed-Mode
The mirror do main of track which havn't pit is duplicated with 20KHz signal to EFM.
In this case, servo action be to unstable because the peak value of mirror signal which is longer than original frame sync signal is detected. In Hi-speed mode, by using the 8.4672/256 MHz signal against peak hold and XTFR/16 or XTFR/32 signal against bottom hold, the mirror is removed, and hi-speed servo action be to stable. Output is that SMSD is 'Hi-Z', SMEF is 'L' SMON is 'H'.

5) Phase-Mode

The mode for controls EFM phase. Phase difference between PBFR/r and XTFR/4 is detected when NCLV of CNTL-Z is 'L' and phase difference between Read Base Counter/4 and Write Base Counter/4 is detected when NCLV is 'H', and the difference is outputed to SMPD.
(refer to figure 8)
'H' is outputed from falling edge of PBFR during (WPO-278T) x 32 to SMSD terminal and 'L' is outputed up to falling edge of next PBFR.
(refer to figure 9)

6) XPHSD-Mode
The mode for using normal action.
The LKFS signal made from frame sync block is to sampling which period is PBFR. If sampling is 'H', Phase Mode is performed, and if the sampling is eight of 'L' continuously, speed mode is performed automatically. Selecting Peak hold period of speed mode, and bottom hold period and gain of speed/hi-speed mode is determined by CNTL-W Reg.

7) VPMSP-Mode
The mode to controls rough servo. Instead of X'tal VCO is used to test EFM pattern.
If the center value of VCO is varid the rotation of spindle motor is varied to same direction and VCO is locked easily.

8) STOP
The mode for stop spindle motor. Output is that SMDP is 'L', SMSD = 'Hi-Z' SMEF is 'L', and SMON is 'L'.

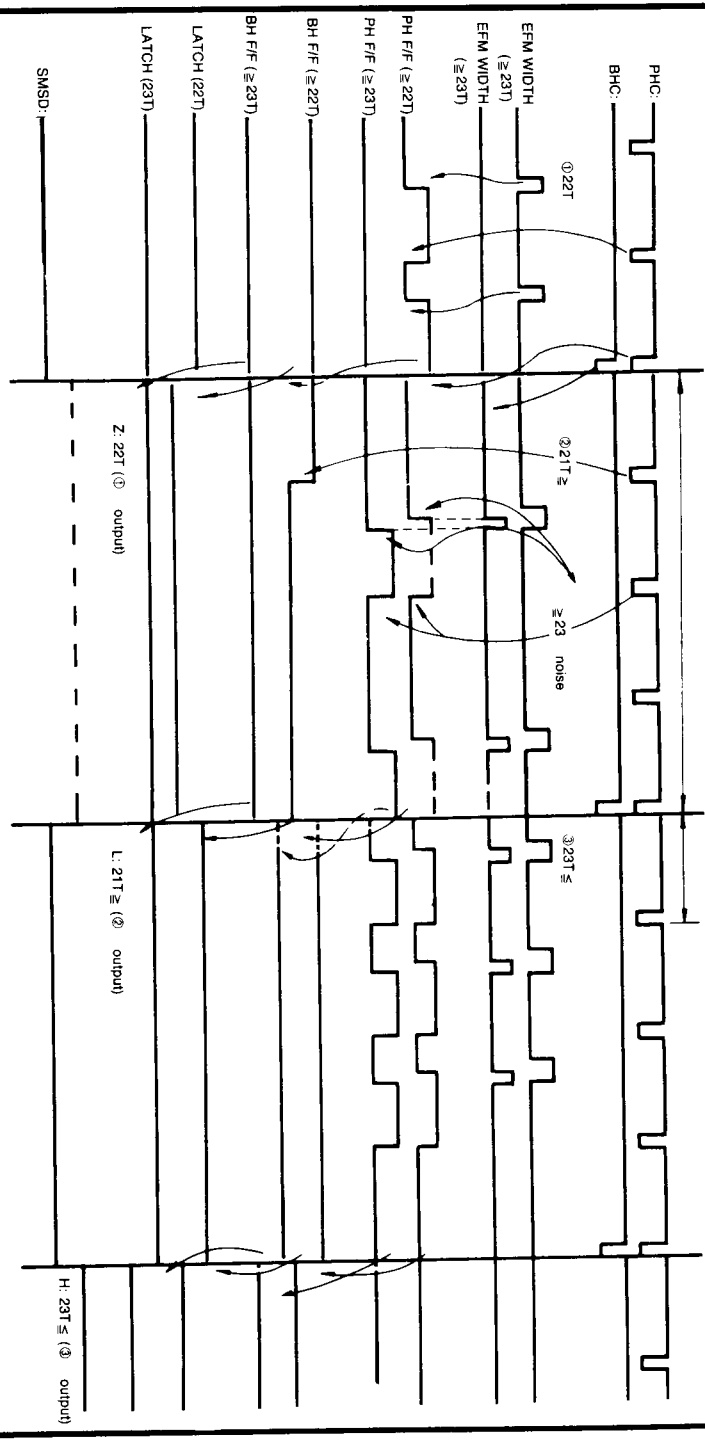


Fig. 18 The timing chart of SMSD output when gain is 'H'

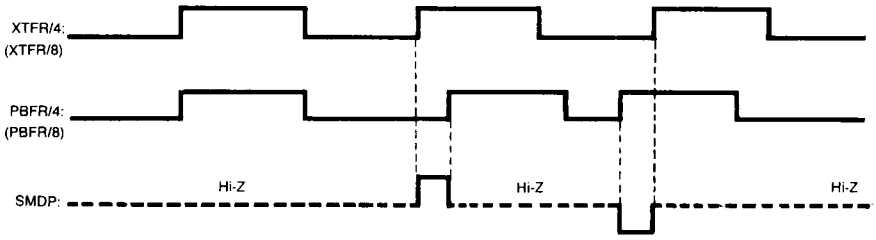
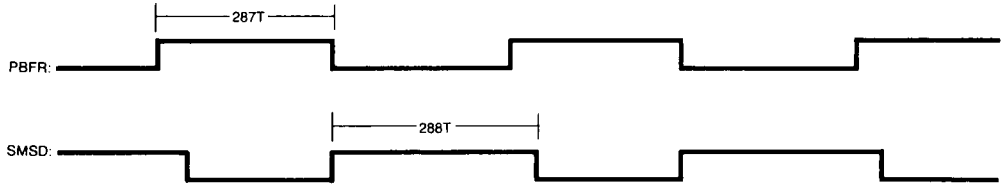
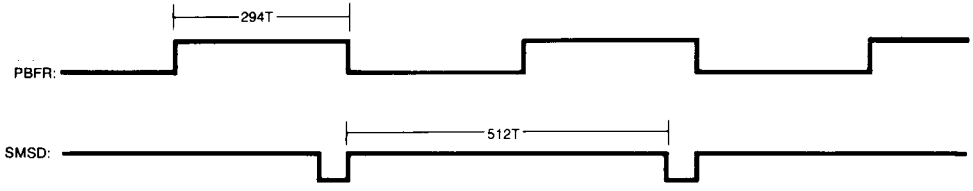


Fig. 19 The timing chart of SMDP output



(a) The timing chart of SMSD output when PBFR is '287T'



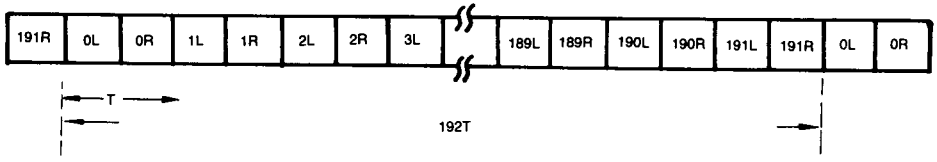
(b) The timing chart of SMDP output when PBFR is '294T'

Fig. 20 The timing chart of SMDP output at phase mode

12. Digital Audio Out

The data is outputed serially by audio interface format to other digital set.

1) Digital Audio Interface Format for CDP



0L: L-CH Format included block sync preamble
1L-191L: L-CH Format included L-CH sync preamble
0R ~ 191R: R-CH format included R-CH sync preamble

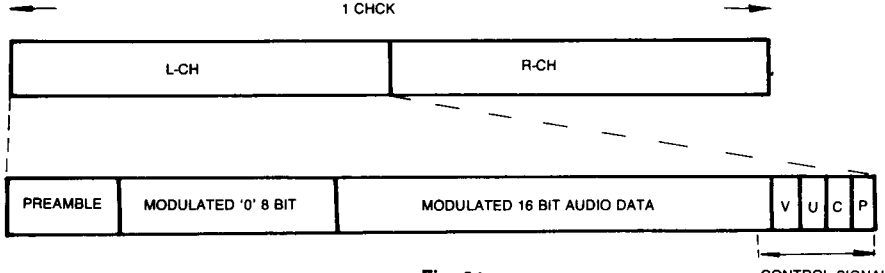


Fig. 21

a) PREAMBLE

Use for discrimate the block of data, L and R-CH DATA

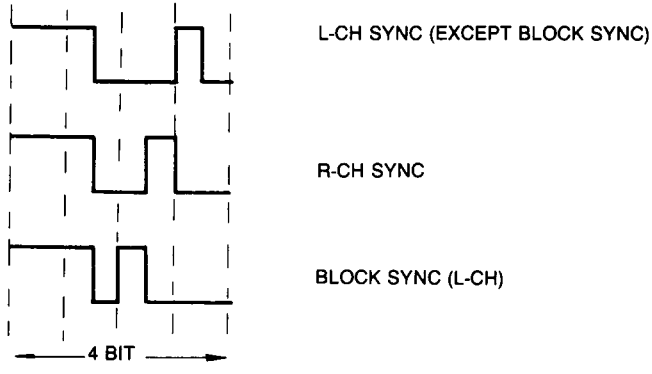


Fig. 22

b) Control Signal

① Validity bit: it is indicated that the error of 16 bit audio data exists, or don't
② User definable bit: subcode data output

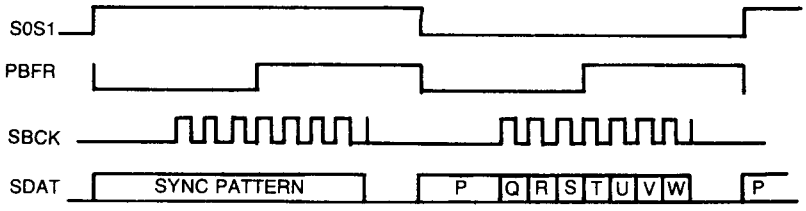
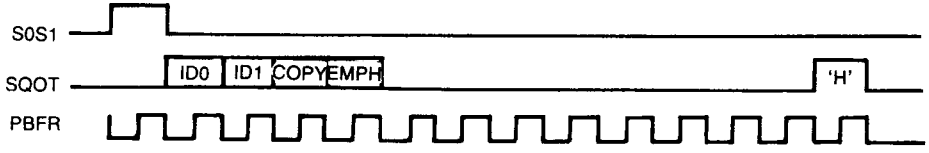


Fig. 23

③ Channel status bit:
Output a high position information of 4 bit of subcode Q indicate the number of channel, pre-emphasis and copy.... etc.
Indicate CDP-category.



④ Parity Bit: Make even parity.

Fig. 24