KS0794

160 COM / 160 SEG DRIVER FOR STN LCD

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Ver. 1.1

Prepared by: Gyeong-Nam, Kim

kgn@samsung.co.kr

KS0794 Specification Revision History		
Version	**Content**	**Date**
0.0	● Original	Apr.1999
1.0	● Including application note.	Jul.1999
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CONTENTS

INTRODUCTION

The KS0794 is a 160-output segment / common driver LSI suitable for driving large scale dot matrix LC panels using as personal computers / work stations. Through the use of SST (Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LC module.

The KS0794 is good both segment driver and common driver, and a low power consuming, high-precision LC panel display can be assembled.
In case of segment mode, the data input is selected 4bit parallel input mode and 8bit parallel input mode by a mode (MD) pin.

In case of common mode, data input/output pins are bi-directional, four data shift directions are pin-selectable.

FEATURES

BOTH SEGMENT MODE AND COMMON MODE

- Supply voltage for LC driver: +15.0 to +32.0V
- Number of LC driver outputs: 160
- Low output impedance
- Low power consumption
- Supply voltage for the logic system: +2.4V to +5.5V
- CMOS silicon gate process (P-type silicon substrate)
- Package: 190-pin TCP (Tape Carrier Package) & Au bump chip

Segment Mode

- Shift clock frequency: 14MHz (Max.) (Vdd = +5V ± 10%)
  8MHz (Max.) (Vdd = +2.4V to +4.5V)
- Adopts a data bus system
- 4-bit / 8-bit parallel input modes are selectable with a mode (MD) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip select, causes the internal clock to be stopped by automatically counting 160 of input data
- Line latch circuit reset function when DISPOFFB active

Common Mode

- Shift clock frequency: 4.0MHz (Max.) (Vdd = +2.4V to +5.5V)
- Built-in 160 bits bi-directional shift register (divisible into 80-bits ×2)
- Available in a single mode (160 bits shift register) or in a dual mode (80 bits shift register ×2)
- Shift register circuit reset function when DISPOFFB active

BLOCK DIAGRAM

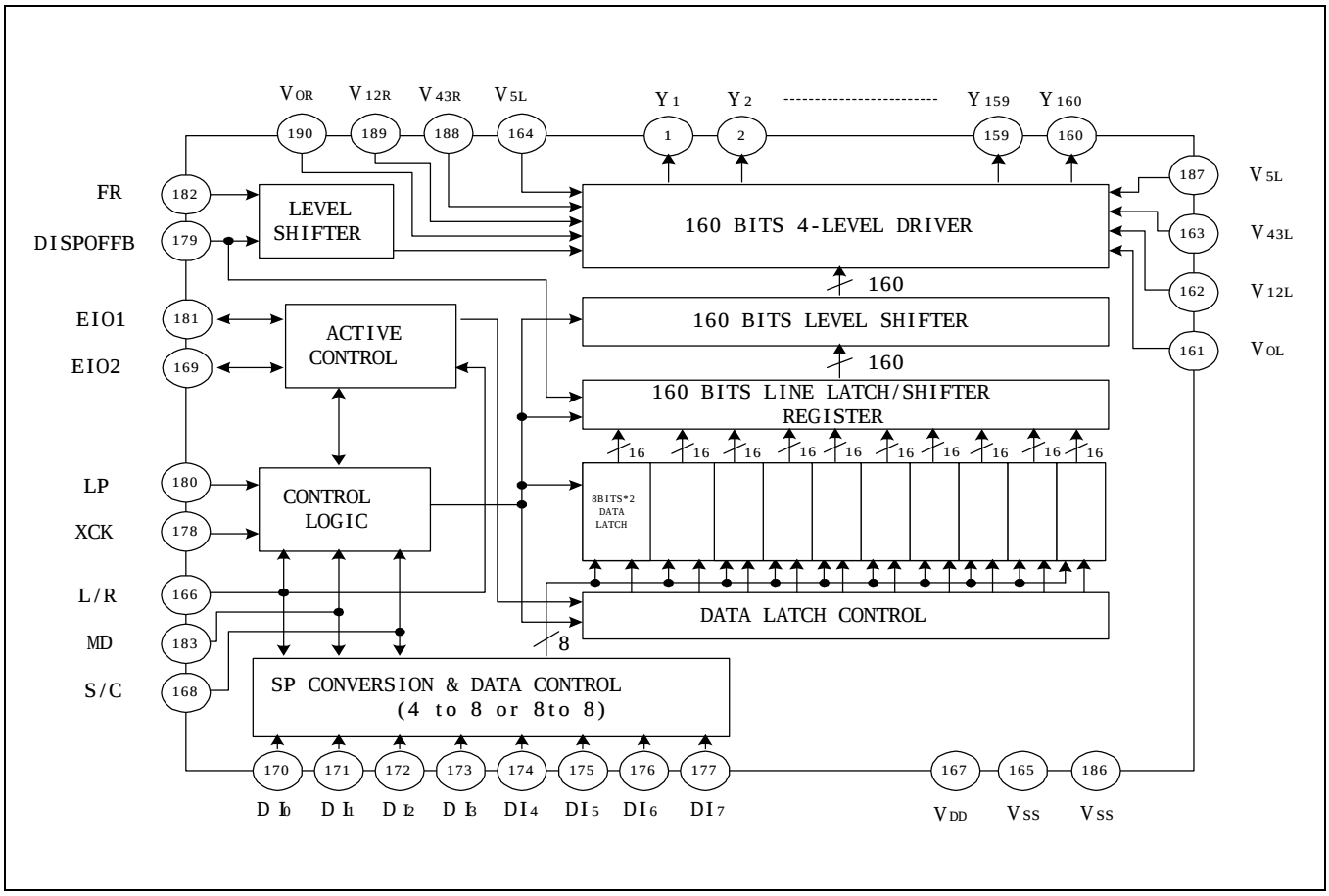

Figure 1. Block Diagram

PAD CONFIGURATION

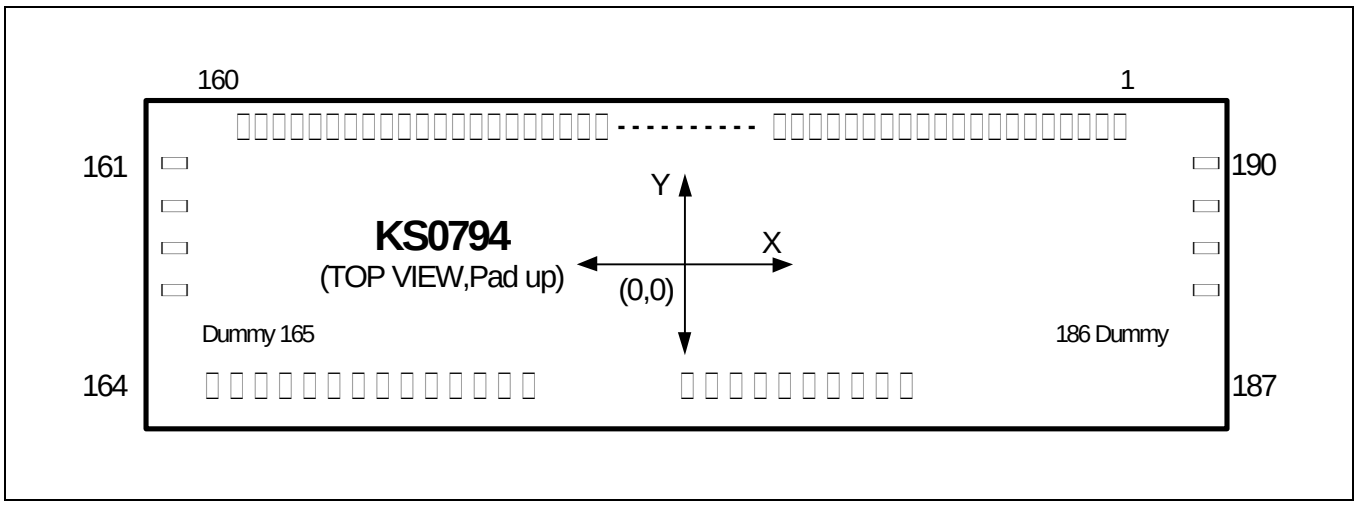

Figure 2. KS0794 Chip Configuration

Table 1. KS0794 Pad Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	11000	1100	mm
Pad pitch	1 to 160	65 (Min.)		
	161 to 190	260 (Min.)		
Bumped pad size	1 to 160	43	108	
	161 to 164 187 to 190	76	58	
	165 to 186	58	76	
Bumped pad height	1 to 190	14 (Typ.)		

PAD CENTER COORDINATES

Table 2. Pad Location

[Unit: mm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
1	Y1	5167.5	395	51	Y51	1917.5	395	101	Y101	-1332.5	395
2	Y2	5102.5	395	52	Y52	1852.5	395	102	Y102	-1397.5	395
3	Y3	5037.5	395	53	Y53	1787.5	395	103	Y103	-1462.5	395
4	Y4	4972.5	395	54	Y54	1722.5	395	104	Y104	-1527.5	395
5	Y5	4907.5	395	55	Y55	1657.5	395	105	Y105	-1592.5	395
6	Y6	4842.5	395	56	Y56	1592.5	395	106	Y106	-1657.5	395
7	Y7	4777.5	395	57	Y57	1527.5	395	107	Y107	-1722.5	395
8	Y8	4712.5	395	58	Y58	1462.5	395	108	Y108	-1787.5	395
9	Y9	4647.5	395	59	Y59	1397.5	395	109	Y109	-1852.5	395
10	Y10	4582.5	395	60	Y60	1332.5	395	110	Y110	-1917.5	395
11	Y11	4517.5	395	61	Y61	1267.5	395	111	Y111	-1982.5	395
12	Y12	4452.5	395	62	Y62	1202.5	395	112	Y112	-2047.5	395
13	Y13	4387.5	395	63	Y63	1137.5	395	113	Y113	-2112.5	395
14	Y14	4322.5	395	64	Y64	1072.5	395	114	Y114	-2177.5	395
15	Y15	4257.5	395	65	Y65	1007.5	395	115	Y115	-2242.5	395
16	Y16	4192.5	395	66	Y66	942.5	395	116	Y116	-2307.5	395
17	Y17	4127.5	395	67	Y67	877.5	395	117	Y117	-2372.5	395
18	Y18	4062.5	395	68	Y68	812.5	395	118	Y118	-2437.5	395
19	Y19	3997.5	395	69	Y69	747.5	395	119	Y119	-2502.5	395
20	Y20	3932.5	395	70	Y70	682.5	395	120	Y120	-2567.5	395
21	Y21	3867.5	395	71	Y71	617.5	395	121	Y121	-2632.5	395
22	Y22	3802.5	395	72	Y72	552.5	395	122	Y122	-2697.5	395
23	Y23	3737.5	395	73	Y73	487.5	395	123	Y123	-2762.5	395
24	Y24	3672.5	395	74	Y74	422.5	395	124	Y124	-2827.5	395
25	Y25	3607.5	395	75	Y75	357.5	395	125	Y125	-2892.5	395
26	Y26	3542.5	395	76	Y76	292.5	395	126	Y126	-2957.5	395
27	Y27	3477.5	395	77	Y77	227.5	395	127	Y127	-3022.5	395
28	Y28	3412.5	395	78	Y78	162.5	395	128	Y128	-3087.5	395
29	Y29	3347.5	395	79	Y79	97.5	395	129	Y129	-3152.5	395
30	Y30	3282.5	395	80	Y80	32.5	395	130	Y130	-3217.5	395
31	Y31	3217.5	395	81	Y81	-32.5	395	131	Y131	-3282.5	395
32	Y32	3152.5	395	82	Y82	-97.5	395	132	Y132	-3347.5	395
33	Y33	3087.5	395	83	Y83	-162.5	395	133	Y133	-3412.5	395
34	Y34	3022.5	395	84	Y84	-227.5	395	134	Y134	-3477.5	395
35	Y35	2957.5	395	85	Y85	-292.5	395	135	Y135	-3542.5	395
36	Y36	2892.5	395	86	Y86	-357.5	395	136	Y136	-3607.5	395
37	Y37	2827.5	395	87	Y87	-422.5	395	137	Y137	-3672.5	395
38	Y38	2762.5	395	88	Y88	-487.5	395	138	Y138	-3737.5	395
39	Y39	2697.5	395	89	Y89	-552.5	395	139	Y139	-3802.5	395
40	Y40	2632.5	395	90	Y90	-617.5	395	140	Y140	-3867.5	395
41	Y41	2567.5	395	91	Y91	-682.5	395	141	Y141	-3932.5	395
42	Y42	2502.5	395	92	Y92	-747.5	395	142	Y142	-3997.5	395
43	Y43	2437.5	395	93	Y93	-812.5	395	143	Y143	-4062.5	395
44	Y44	2372.5	395	94	Y94	-877.5	395	144	Y144	-4127.5	395
45	Y45	2307.5	395	95	Y95	-942.5	395	145	Y145	-4192.5	395
46	Y46	2242.5	395	96	Y96	-1007.5	395	146	Y146	-4257.5	395
47	Y47	2177.5	395	97	Y97	-1072.5	395	147	Y147	-4322.5	395
48	Y48	2112.5	395	98	Y98	-1137.5	395	148	Y148	-4387.5	395
49	Y49	2047.5	395	99	Y99	-1202.5	395	149	Y149	-4452.5	395
50	Y50	1982.5	395	100	Y100	-1267.5	395	150	Y150	-4517.5	395

Table 2. Pad Location (Continued)

[Unit: mm]

NO	NAME	X	Y
151	Y151	-4582.5	395
152	Y152	-4647.5	395
153	Y153	-4712.5	395
154	Y154	-4777.5	395
155	Y155	-4842.5	395
156	Y156	-4907.5	395
157	Y157	-4972.5	395
158	Y158	-5037.5	395
159	Y159	-5102.5	395
160	Y160	-5167.5	395
161	VOL	-5369	330
162	V12L	-5369	90
163	V43L	-5369	-120
164	V5L	-5369	-330
	DUMMY1	-4860	-419
165	VSS	-4600	-419
166	LR	-4340	-419
167	VDD	-4080	-419
168	SC	-3820	-419
169	EIO2	-3560	-419
170	DI0	-3300	-419
171	DI1	-3040	-419
172	DI2	-2780	-419
173	DI3	-2520	-419
174	DI4	-2260	-419
175	DI5	-2000	-419
176	DI6	-1740	-419
177	DI7	-1480	-419
178	XCK	2290	-419
179	DISPOFFB	2550	-419
180	LP	2810	-419
181	EIO1	3070	-419
182	FR	3330	-419
183	MD	3590	-419
184	NC	3850	-419
185	NC	4110	-419
186	VSS	4370	-419
	DUMMY2	4630	-419
187	V5R	5369	-330
188	V43R	5369	-120
189	V12R	5369	90
190	V0R	5369	330

PIN DESCRIPTION

Table 3. Pin Description

Pin No.	Symbol	I/O	Description
1 to 160	Y_1 – Y_{160}	O	LC driver output
161, 190	V_{0L}, V_{0R}	-	Power supply for LC driver
162, 189	V_{12L}, V_{12R}	-	Power supply for LC driver
163, 188	V_{43L}, V_{43R}	-	Power supply for LC driver
164, 187	V_{5L}, V_{5R}	-	Power supply for LC driver
166	L/R	I	Display data shift direction selection
167	V_{DD}	-	Power supply for logic system (+2.4 to +5.5V)
168	S/C	I	Segment mode/common mode selection
169	EIO_2	I/O	Input / output for chip select or data of shift register
170 to 176	DI_0 – DI_6	I	Display data input for segment mode
177	DI_7	I	Display data input for segment mode / dual mode data input
178	XCK	I	Display data shift clock input for segment mode
179	DISPOFFB	I	Control input for deselect output level
180	LP	I	Latch pulse input / shift clock input for shift register
181	EIO_1	I/O	Input/output for chip select or data of shift register
182	FR	I	AC-converting signal input for LC driver waveform
183	MD	I	Mode selection input
165, 186	V_{SS}	-	Ground (0V)

FUNCTIONAL DESCRIPTION

BLOCK FUNCTION

. Active Control
In case of segment mode, controls the selection or deselection of the chip. Following a LP signal, and after the chip select signal is input, a select signal is generated internally until 160 bits of data have been read in.
Once data input has been completed, a select signal for cascade connection is output, and the chip is deselected.
In case of common mode, controls the input/output data of bidirectional pins.

. SP Conversion & Data Control
In case of segment mode, keep input data which are 2 clocks of XCK at 4-bit parallel mode into latch circuit, or keep input data which are 1 clock of XCK at 8-bits parallel mode into latch circuit, after that they are put on the internal data bus 8 bits at a time.

. Data Latch Control
In case of segment mode, selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic, for every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.

. Data Latch
In case of segment mode, latches the data on the data bus. The latched state of each LC driver output pin is controlled by the control logic and the data latch control, 160 bits of data are read in 20 sets of 8 bits.

. Line Latch / Shift Register
In case of segment mode, all 160 bits which have been read into the data latch are simultaneously latched on the falling edge of the LP signal, and output to the level shifter block.
In case of common mode, shifts data from the data input pin on the falling edge of the LP signal.

. Level Shifter
The logic voltage signal is level-shifted to the LC driver voltage level, and output to the driver block.

. 4-level Driver
Driver the LC driver output pins from the line latch/shift register data, selecting one of 4 levels (V_0, V_{12}, V_{43}, V_5) based on the S/C, FR and DISPOFFB signals.

. Control Logic
Controls the operation of each block. In case of segment mode, when a LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block.
Once the selection signal has been output, operation of the data latch and data transmission are controlled, 160 bits of data are read in, and the chip is deselected. In case of common mode, controls the direction of data shift.

PIN FUNCTION

Segment Mode

Symbol	Function
V_{DD}	Logic system power supply pin connects to +2.4 to +5.5V
V_{SS}	Ground pin connects to 0 V
V_{0R}, V_{0L} V_{12R} , V_{12L} V_{43R} , V_{43L}	Power supply pin for LC driver voltage bias. . Normally, the bias voltage used is set by a resistor divider. . Ensure that voltage are set such that $V_{SS}<V_{43}<V_{12}<V_0$. . To further reduce the difference between the output waveforms of LC driver output pins Y_1 and Y_{160}, externally connect V_{iR} and V_{iL} (I = 0, 12, 43)
DI_0 – DI_7	Input pin for display data . In 4-bit parallel input mode, input data into the 4 pins DI_0 - DI_3. Connect DI_4 - DI_7 to V_{SS} or V_{DD}. . In 8-bit parallel input mode, input data into the 8 pins DI_0 - DI_7.
XCK	Clock input pin for taking display data . Data is read on the falling edge of the clock pulse.
LP	Latch pulse input pin for display data . Data is latched on the falling edge of the clock pulse.
L/R	Direction selection pin for reading display data . When set to V_{SS} level “L”, data is read sequentially from Y_{160} to Y_1. . When set to V_{DD} level H”, data is read sequentially from Y_1 to Y_{160}.
DISPOFFB	Control input pin for output deselect level . The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit. . When set to V_{SS} level “L”, the LC drive output pins (Y_1 - Y_{160}) are set to level V_{SS}. . While set to “L”, the contents of the line latch are reset, but read the display data in the data latch regardless of condition of DISPOFFB. When the DISPOFFB function is canceled, the driver outputs deselect level (V_{12} or V_{43}), then outputs the contents of the data latch on the next falling edge of the LP. That time, if DISPOFFB removal time can not keep regulation what is shown AC characteristics (page 21), can not output the reading data correctly.

Segment Mode (Continued)

FR	AC signal input for LC driving waveform . The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit. . Normally, inputs a frame inversion signal. . The LC driver output pin's output voltage level can be set using the line latch output signal and the FR signal. Table of truth values is shown in table 4.
MD	Mode selection pin . When set to V_{SS} level "L", 4-bit parallel input mode is set. . When set to V_{DD} level "H", 8-bit parallel input mode is set. . The relationship between the display data and driver output pins is shown in table 5.
S/C	Segment mode / common mode selection pin . When set to V_{DD} level 'H", segment mode is set.
EIO_1 **EIO_2**	Input / output pin for chip selection . When L/R input is at V_{SS} level 'L", EIO_1 is set for output, and EIO_2 is set for input. . When L/R input is at V_{DD} level 'H", EIO_1 is set for input, and EIO_2 is set for output. . During output. set to "H" while LP*XCLKB is 'H" and after 160-bits of data have been read, set to "L" for one cycle (from falling edge to falling edge of XCK), after which it returns to "H". . During input, after the LP signal is input, the chip is selected while EI is set to "L". After 160-bits of data have been read, the chip is deselected.
$Y_1 – Y_{160}$	LC driver output pins . Corresponding directly to each bit of the data latch, one level (V_0, V_{12}, V_{43}, or V_{SS}) is selected and output. Table of truth values are shown in table 4.

Common Mode

Symbol	Function
V_{DD}	Logic system power supply pin connects to +2.4 to +5.5V
V_{SS}	Ground pin connects to 0 V
V_{0R}, V_{0L} V_{12R} , V_{12L} V_{43R} , V_{43L}	Power supply pin for LC driver voltage bias. . Normally, the bias voltage used is set by a resistor divider. . Ensure that voltage are set such that $V_{SS}<V_{43}<V_{12}<V_0$. . To further reduce the difference between the output waveforms of LC driver output pins Y_1 and Y_{160}, externally connect V_{iR} and V_{iL} (I = 0, 12, 43)
EIO_1	Bidirectional shift register shift data input/output pin . Output pin when L/R is at V_{SS} level “L”, input pin when L/R is at V_{DD} level “H”. . When EIO1 is used as input pin, it will be pull-down. . When EIO1 is used as output pin, it won’t be pull-down.
EIO_2	Bidirectional shift register shift data input / output pin . Input pin when L/R is at V_{SS} level “L”, output pin when L/R is at V_{DD} level “H”. . When EIO_2 is used as input pin, it will be pull-down. . When EIO_2 is used as output pin, it won’t be pull-down.
LP	Bidirectional shift register shift clock pulse input pin . Data is shifted on the falling edge of the clock pulse.
L/R	Bidirectional shift register shift direction selection pin . Data is shifted from Y_{160} to Y_1 when set to V_{SS} to level “L”, and data is shifted from Y_1 to Y_{160} when set to V_{DD} level “H”.

Common Mode (Continued)

DISPOFFB	Control input pin for output deselect level . The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit. . When set to V_{SS} level "L", the LC drive output pins (Y_1 - Y_{160}) are set to level V_{SS}. . While set to "L", the contents of the shift resister are reset not reading data. When the DISPOFFB function is canceled, the driver outputs deselect Level (V_{12} or V_{43}), and the shift data is reading on the falling edge of the LP. That time, if DISPOFFB removal time can not keep regulation what is shown AC characteristics (page 25), the shift data is not reading correctly.
FR	AC signal input for LC driving waveform . The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit. . Normally, input a frame inversion signal. . The LC driver output pin's output voltage level can be set using the shift register output signal and the FR signal. Table of truth values are shown in table 4.
MD	Mode selection pin . When set to V_{SS} level "L", Single mode operation is selected, when set to V_{DD} level "H", Dual mode operation is selected.
DI_7	Dual Mode data input pin . According to the data shift direction of the data shift register, data can be input starting from the 81st bit. When the chip is used as Dual mode, DI_7 will be pull-down. When the chip is used as Single mode, DI_7 won't be pull-down.
S/C	Segment mode / Common mode selection pin . When set to V_{SS} level 'L", common mode is set.
DI_0 – DI_6	Not used . Connect DI_0 - DI_6 to V_{SS} or V_{DD}. Avoiding floating.
XCK	Not used . XCK is pull-down in common mode, so connect to V_{SS} or open.
Y_1 – Y_{160}	LC driver output pins . Corresponding directly to each bit of the shift register, one level (V0, V12, V43, or VSS) is selected and output. Table of truth values are shown in table 4.

FUNCTIONAL OPERATIONS

Segment Mode

Table 4-1. Truth Table

FR	Latch data	DISPOFFB	Driver output voltage level (Y_1 – Y_{160})
L	L	H	V_{43}
L	H	H	V_5
H	L	H	V_{12}
H	H	H	V_0
x	X	L	V_5

Here, $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$, H: V_{DD} (+2.4V to +5.5V), L: V_{SS} (0V), x: Don't care

Common Mode

Table 4-2. Truth Table

FR	Latch data	DISPOFFB	Driver output voltage level (Y_1 – Y_{160})
L	L	H	V_{43}
L	H	H	V_0
H	L	H	V_{12}
H	H	H	V_5
x	x	L	V_5

Here, $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$, H: V_{DD} (+2.4V to +5.5V), L: V_{SS} (0V), x: Don't care

Note: There are two kinds of power supply (logic level voltage, LC drive voltage) for LCD driver, please supply regular voltage which assigned by specification for each power pin. That time 'Don't care" should be fixed to 'H" or "L ", avoiding floating.

RELATIONSHIP BETWEEN THE DISPLAY DATA AND DRIVER OUTPUT PINS

Segment Mode

4-bit Parallel Mode

Table 5-1. 4-bit Parallel Mode

MD	L/R	EIO1	EIO2	Data Input	Figure of clock						
					1st	2nd	3rd	..	38th	39th	40th
L	L	Output	Input	DI0	Y157	Y153	Y149	..	Y9	Y5	Y1
				DI1	Y158	Y154	Y150	..	Y10	Y6	Y2
				DI2	Y159	Y155	Y151	..	Y11	Y7	Y3
				DI3	Y160	Y156	Y152	..	Y12	Y8	Y4
L	H	Input	Output	DI0	Y4	Y8	Y12	..	Y152	Y156	Y160
				DI1	Y3	Y7	Y11	..	Y151	Y155	Y159
				DI2	Y2	Y6	Y10	..	Y150	Y154	Y158
				DI3	Y1	Y5	Y9	..	Y149	Y153	Y157

8-bit Parallel Mode

Table 5-2. 5-bit Parallel Mode

MD	L/R	EIO1	EIO2	Data Input	Figure of clock						
					1st	2nd	3rd	..	18th	19th	20th
H	L	Output	Input	DI0	Y153	Y145	Y137	..	Y17	Y9	Y1
				DI1	Y154	Y146	Y138	..	Y18	Y10	Y2
				DI2	Y155	Y147	Y139	..	Y19	Y11	Y3
				DI3	Y156	Y148	Y140	..	Y20	Y12	Y4
				DI4	Y157	Y149	Y141	..	Y21	Y13	Y5
				DI5	Y158	Y150	Y142	..	Y22	Y14	Y6
				DI6	Y159	Y151	Y143	..	Y23	Y15	Y7
				DI7	Y160	Y152	Y144	..	Y24	Y16	Y8
H	H	Input	Output	DI0	Y8	Y16	Y24	..	Y144	Y152	Y160
				DI1	Y7	Y15	Y23	..	Y143	Y151	Y159
				DI2	Y6	Y14	Y22	..	Y142	Y150	Y158
				DI3	Y5	Y13	Y21	..	Y141	Y149	Y157
				DI4	Y4	Y12	Y20	..	Y140	Y148	Y156
				DI5	Y3	Y11	Y19	..	Y139	Y147	Y155
				DI6	Y2	Y10	Y18	..	Y138	Y146	Y154
				DI7	Y1	Y9	Y17	..	Y137	Y145	Y153

Common Mode

Table 5-3. Common Mode

MD	L/R	Data transfer direction	EIO1	EIO2	DI7
L (Single)	L(shift to left)	$Y_{160} \rightarrow Y_1$	Output	Input	X
	H(shift to right)	$Y_1 \rightarrow Y_{160}$	Input	Output	X
H (Dual)	L(shift to left)	$Y_{160} \rightarrow Y_{81}$ $Y_{80} \rightarrow Y_1$	Output	Input	Input
	H(shift to right)	$Y_1 \rightarrow Y_{80}$ $Y_{81} \rightarrow Y_{160}$	Input	Output	Input

Here, L: V_{SS}(0V), H: V_{DD}(+2.4V to +5.5V), X: Don't care

NOTE: "Don't care" should be fixed to "H" or "L", avoid floating.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 6. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Applicable pins	Ratings	Unit
Supply voltage (1)	V_{DD}	Ta=25 °C Referenced to V_{SS}(0V)	V_{DD}	-0.3 to +6.5	V
Supply voltage (2)	V_0		V_{0L}, V_{0R}	-0.3 to +35	V
	V_{12}		V_{12L}, V_{12R}	-0.3 to V_0+0.3	V
	V_{43}		V_{43L}, V_{43R}	-0.3 to V_0+0.3	V
	V_5		V_{5L}, V_{5R}	-0.3 to V_0+0.3	V
Input voltage	V_I		DI_0 –DI_7, XCK, LP, L/R, MD, S/C, EIO_1, EIO_2, DISPOFFB	-0.3 to V_{DD}+0.3	V
Storage temperature	T_{STG}	-	-	-45 to 125	°C

RECOMMENDED OPERATING CONDITIONS

Table 7. Recommended Operating Conditions

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Supply voltage (1)	V_{DD}	Referenced to V_{SS}(0V)	V_{DD}	+2.4		+5.5	V
Supply voltage (2)	V_0		V_{0L}, V_{0R}	+15		+32	V
Operating temperature	T_{OPR}	-	-	-20		+85	°C

NOTE: Ensure that voltage are set such that $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$

DC CHARACTERISTICS

Segment Mode

Table 8-1. DC Characteristics for Segment Mode

(V_{SS} = V_5 = 0V, V_{DD} = +2.4 to 5.5V, V_0 = +15 to +32V, Ta = -20~85°C)

Parameter	Symbol	Conditions		Applicable pins	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}			DI_0 -DI_7, XCK, LP, L/R, FR, MD, S/C,EIO_1, EIO_2, DISPOFFB	0.8V_{DD}			V
	V_{IL}						0.2V_{DD}	V
Output voltage	V_{OH}	I_{OH}=-0.4mA		EIO_1, EIO_2	V_{DD}-0.4			V
	V_{OL}	I_{OL}=+0.4mA					+0.4	V
Input leakage current	I_{LIH}	V_I=V_{DD}		DI_0 -DI_7, XCK, LP, L/R, FR, MD, S/C,EIO_1, EIO_2, DISPOFFB			+10	uA
	I_{LIL}	V_I=V_{SS}					-10	uA
Output resistance	R_{ON}	|ΔV_{ON}| =0.5V	V_0=+30V	Y_1- Y_{160}		1.0	1.5	kΩ
			V_0=+20V			1.5	2.0	
Stand-by current	I_{STB}	*1		V_{SS}			50.0	uA
Consumed current(1) (Deselection)	I_{DD1}	*2		V_{DD}			2.0	mA
Consumed current(2) (Selection)	I_{DD2}	*3		V_{DD}			8.0	mA
Consumed current	I_0	*4		V_0			1.0	mA

NOTE : 1. V_{DD} = +5V, V_0 = +32V, V_I = V_{SS}

2. V_{DD} = +5V, V_0 = +32V, f_{XCK} = 14MHz, No-load, EI = V_{DD}
   The input data is turned over by data taking clock (4-bit parallel input mode)
3. V_{DD} = +5V, V_0 = +32V, f_{XCK} = 14MHz, No-load, EI = V_{SS}
   The input data is turned over by data taking clock (4-bit parallel input mode)
4. V_{DD} = +5V, V_0 = +32V, f_{XCK} = 14MHz, f_{LP} = 41.6kHz, f_{FR} = 80Hz, No-load
   The input data is turned over by data taking clock (4-bit parallel input mode)

Common Mode

Table 8-2. DC Characteristics for Common Mode

(V_{SS} = V_5 = 0V, V_{DD} = +2.4 to 5.5V, V_0 = +15 to +32V, Ta = -20~85°C)

Parameter	Symbol	Conditions		Applicable pins	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}	-		DI_0 -DI_7, XCK, LP, L/R, FR, MD, S/C,EIO_1, EIO_2, DISPOFFB	0.8V_{DD}			V
	V_{IL}	-					0.2V_{DD}	V
Output voltage	V_{OH}	I_{OH} = -0.4mA		EIO_1, EIO_2	V_{DD}-0.4			V
	V_{OL}	I_{OL} = +0.4mA					+0.4	V
Input leakage current	I_{LIH}	V_I = V_{DD}		DI_0 -DI_7, XCK, LP, L/R, FR, MD, S/C,EIO_1, EIO_2, DISPOFFB			+10	uA
	I_{LIL}	V_I = V_{SS}					-10	uA
Output resistance	R_{ON}	|ΔV_{ON}| = 0.5V	V_0 = +30V	Y_1 - Y_{160}		1.0	1.5	kΩ
			V_0 = +20V			1.5	2.0	
Input pull-down current	I_{PD}	V_I = V_{DD}		XCK, EIO_1, EIO_2, DI_7			100.0	uA
Stand-by current	I_{STB}	*1		V_{SS}			50.0	uA
Consumed current(1)	I_{DD}	*2		V_{DD}			80.0	uA
Consumed current(2)	I_0	*2		V_0			160.0	uA

NOTE: 1. V_{DD} = +5V, V_0 = +32V, V_I = V_{SS}

2. V_{DD} = +5V, V_0 = +32V, f_{LP} = 41.6kHz, f_{FR} = 80Hz in case of 1/320 duty operation, No-load

AC CHARACTERISTICS

Segment Mode 1

Table 9-1. AC Characteristics for Segment Mode

(V_{SS} = V_5 = 0V, V_{DD} = +4.5 to +5.5V, V_0 = +15 to +32V, Ta = -20~85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift clock period *1	T_{WCK}	T_R, T_F≤10 ns	71			ns
Shift clock “H” pulse width	T_{WCKH}		23			ns
Shift clock “L” pulse width	T_{WCKL}		23			ns
Data setup time	T_{DS}		10			ns
Data hold time	T_{DH}		20			ns
Latch pulse “H” pulse width	T_{WLPH}		23			ns
Shift clock rise to latch pulse rise time	T_{LD}		0			ns
Shift clock fall to latch pulse fall time	T_{SL}		25			ns
Latch pulse rise to shift clock rise time	T_{LS}		25			ns
Latch pulse fall to shift clock fall time	T_{LH}		25			ns
Input signal rise time *2	T_R				50	ns
Input signal fall time *2	T_F				50	ns
Enable setup time	T_S		21			ns
DISPOFFB removal time	T_{SD}		100			ns
DISPOFFB “L” pulse width	T_{WDL}		1.2			us
Output delay time (1)	T_D	C_L = 15pF			40	ns
Output delay time (2)	T_{PD1}, T_{PD2}	C_L = 15pF			1.2	us
Output delay time (3)	T_{PD3}	C_L = 15pF			1.2	us

NOTES: 1. Take the cascade connection into consideration.

2. (T_{WCK} – T_{WCKH} – T_{WCKL}) / 2 is maximum in the case of high speed operation.

Segment Mode 2

Table 9-2. AC Characteristics for Segment Mode

(V_{SS} = V_5 = 0V, V_{DD} = +2.4V to +4.5V, V_0 = +15 to +32V, Ta = -20~85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift clock period *1	T_{WCK}	T_R, T_F≤10 ns	125			ns
Shift clock “H” pulse width	T_{WCKH}		51			ns
Shift clock “L” pulse width	T_{WCKL}		51			ns
Data setup time	T_{DS}		30			ns
Data hold time	T_{DH}		40			ns
Latch pulse “H” pulse width	T_{WLPH}		51			ns
Shift clock rise to latch pulse rise time	T_{LD}		0			ns
Shift clock fall to latch pulse fall time	T_{SL}		51			ns
Latch pulse rise to shift clock rise time	T_{LS}		51			ns
Latch pulse fall to shift clock fall time	T_{LH}		51			ns
Input signal rise time *2	T_R				50	ns
Input signal fall time *2	T_F				50	ns
Enable setup time	T_S		36			ns
DISPOFFB removal time	T_{SD}		100			ns
DISPOFFB “L” pulse width	T_{WDL}		1.2			us
Output delay time (1)	T_D	C_L = 15pF			78	ns
Output delay time (2)	T_{PD1}, T_{PD2}	C_L = 15pF			1.2	us
Output delay time (3)	T_{PD3}	C_L = 15pF			1.2	us

NOTES: 1. Take the cascade connection into consideration.

2. (T_{WCK} – T_{WCKH} – T_{WCKL}) / 2 is maximum in the case of high speed operation.

TIMING CHARACTERISTICS OF SEGMENT MODE

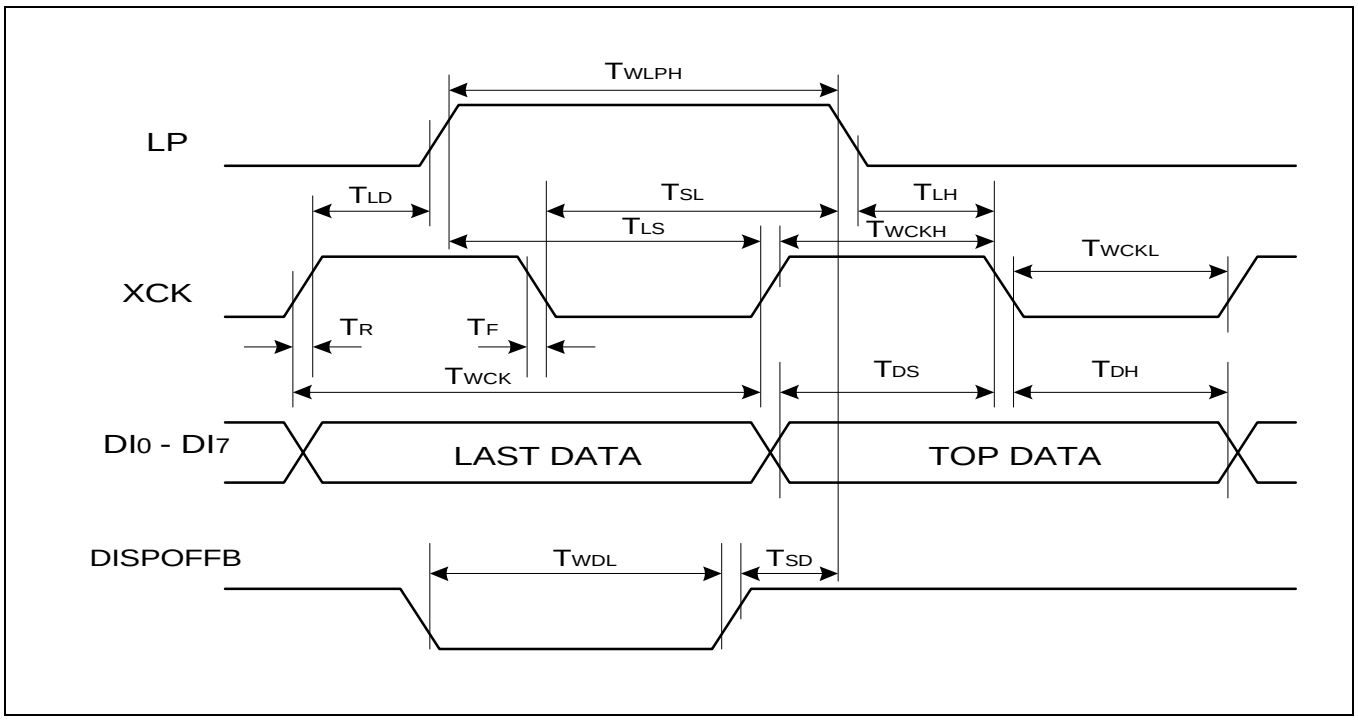

Figure 3-1. Timing Characteristics of Segment Mode

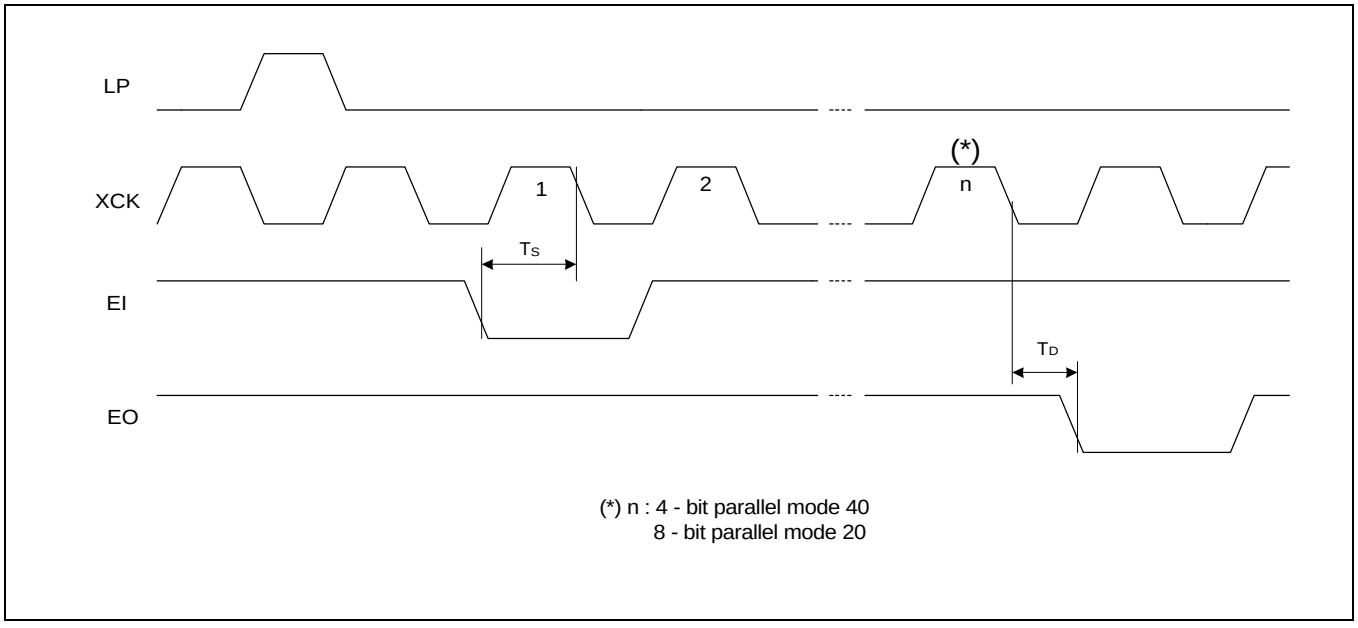

Figure 3-2. Timing Characteristics of Segment Mode

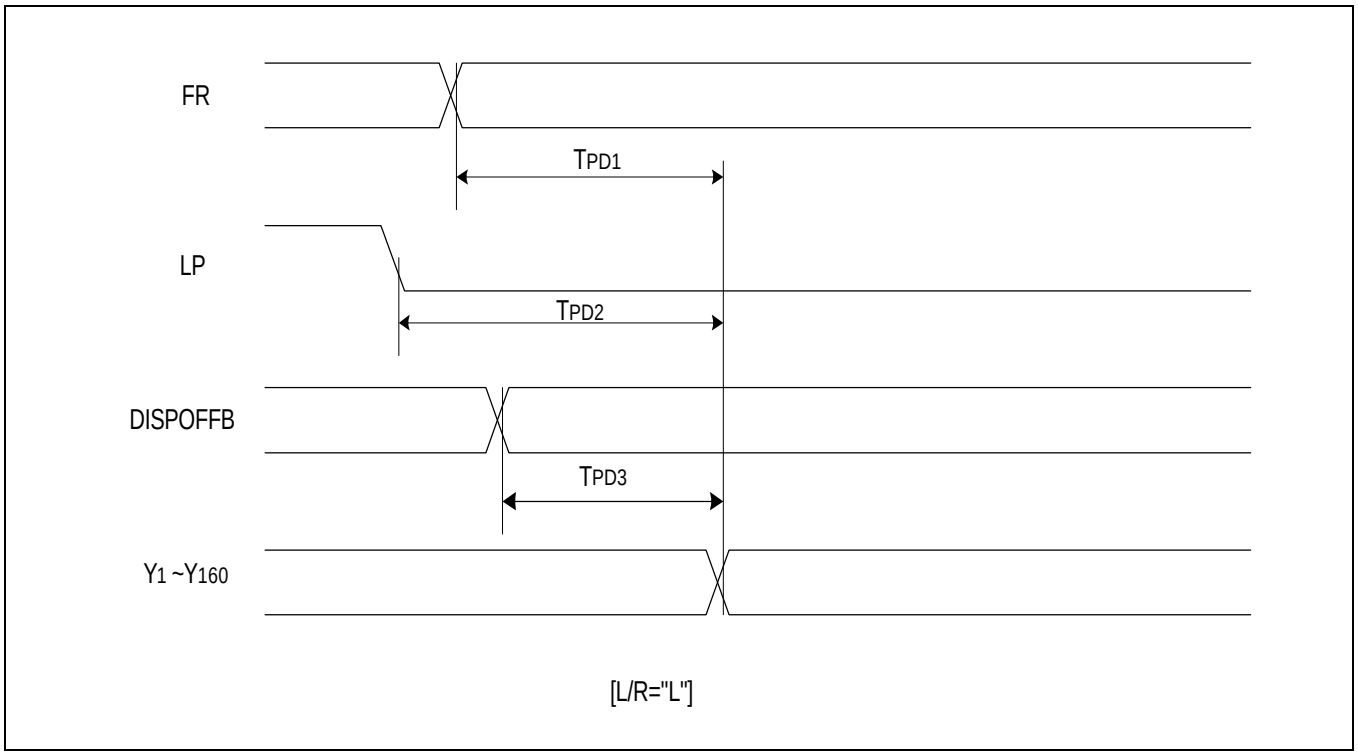

Figure 3-3. Timing Characteristics of Segment Mode

Common Mode

Table 10. AC Characteristics of Common Mode

(V_{SS} = V_5 = 0V, V_{DD} = +2.4V to +4.5V, V_0 = +15 to +32V, Ta = -20~85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period	T_{WLP}	T_R, T_F≤20ns	250			ns
Shift "H" pulse width	T_{WLPH}	V_{DD}=+5.0V±10%	15			ns
		V_{DD}=+2.5V~+4.5V	30			ns
Data setup time	T_{SU}		30			ns
Data hold time	T_H		50			ns
Input signal rise time	T_R				50	ns
Input signal fall time	T_F				50	ns
DISPOFFB removal time	T_{SD}		100			ns
DISPOFFB 'L" pulse width	T_{WDL}		1.2			us
Output delay time (1)	T_{DL}	CL=15pF			200	ns
Output delay time (2)	T_{PD1},T_{PD2}	CL=15pF			1.2	us
Output delay time (3)	T_{PD3}	CL=15pF			1.2	us

Timing Characteristics of Common Mode

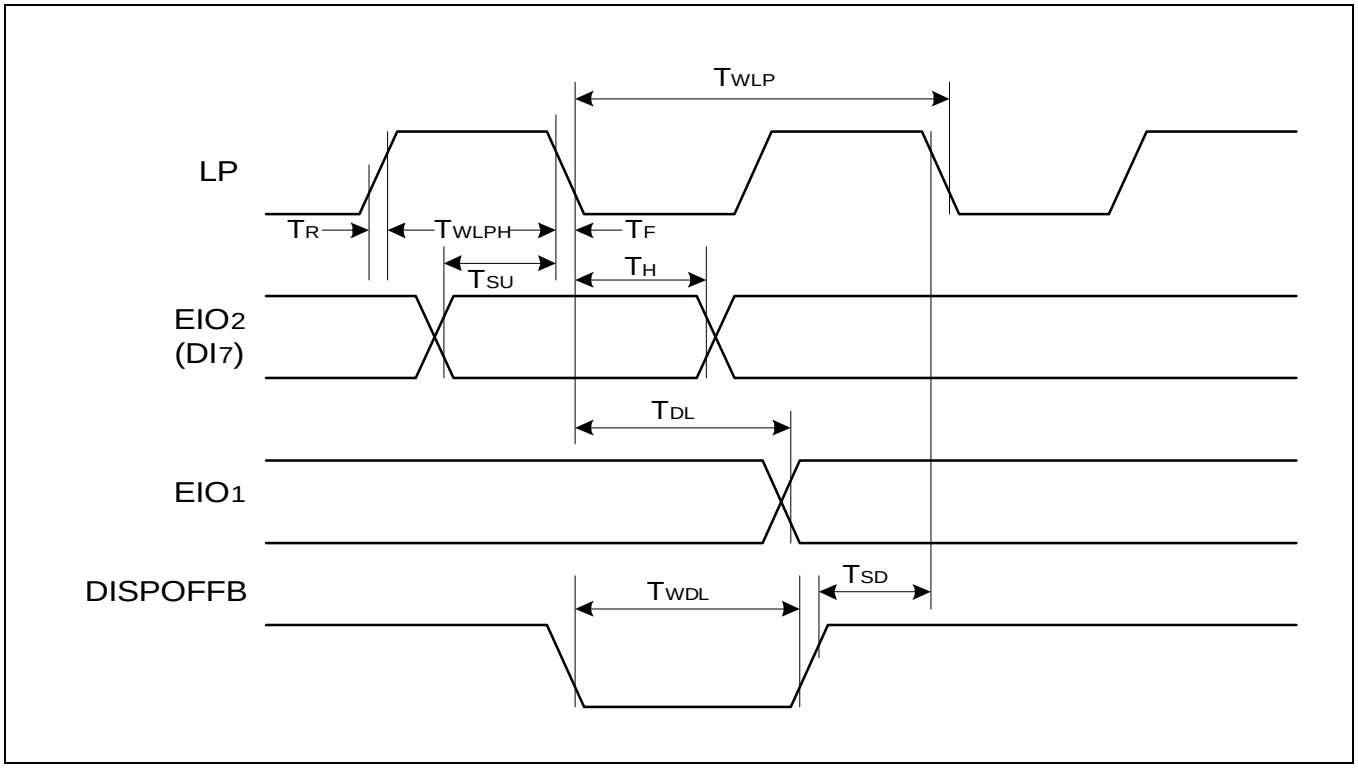

Figure 4-1. Timing Characteristics of Common Mode

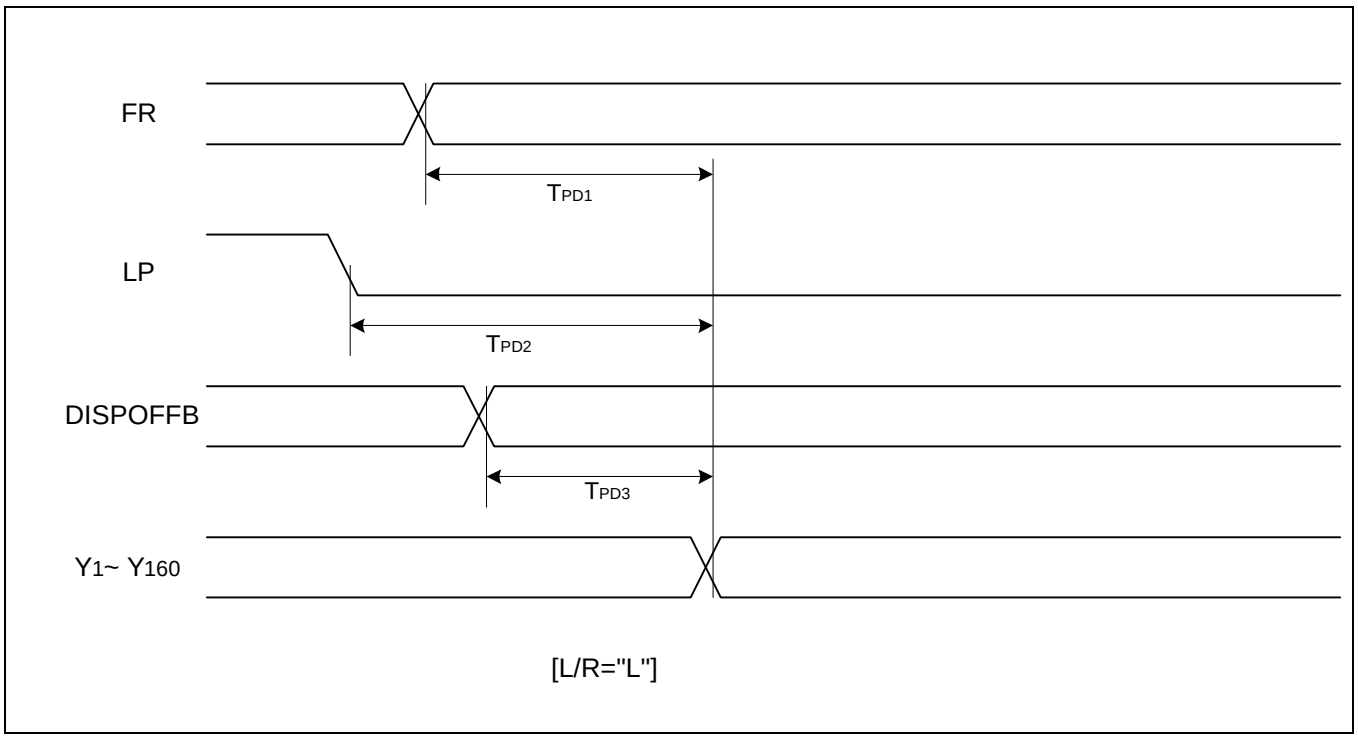

Figure 4-2. Timing Characteristics of Common Mode

PRECAUTION

. Precaution when Connecting or Disconnecting the Power

This LSI has a high-voltage LC driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LC driver power supply while the logic system power supply is floating.

The detail is as follows.

. When connecting the power supply, connect the LC drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LC driver power.

. We recommend you connecting the serial resistor (50~100Ω) or fuse to the LC drive power V_0 of the system as a current limiter. And set up the suitable of the resistor in consideration of LC display grade.

And when connecting the logic power supply, the logic condition of this LSI inside is insecurity. Therefore connect the LC driver power supply after resetting logic condition of this LSI inside on DISPOFFB function. After that, cancel the DISPOFFB function after the LC driver power supply has become stable. Furthermore, when disconnecting the power, set the LC drive output pins to level V_5 on DISPOFFB function. After that, disconnect the logic system power after disconnecting the LC drive power.
When connecting the power supply, show the following recommend sequence.

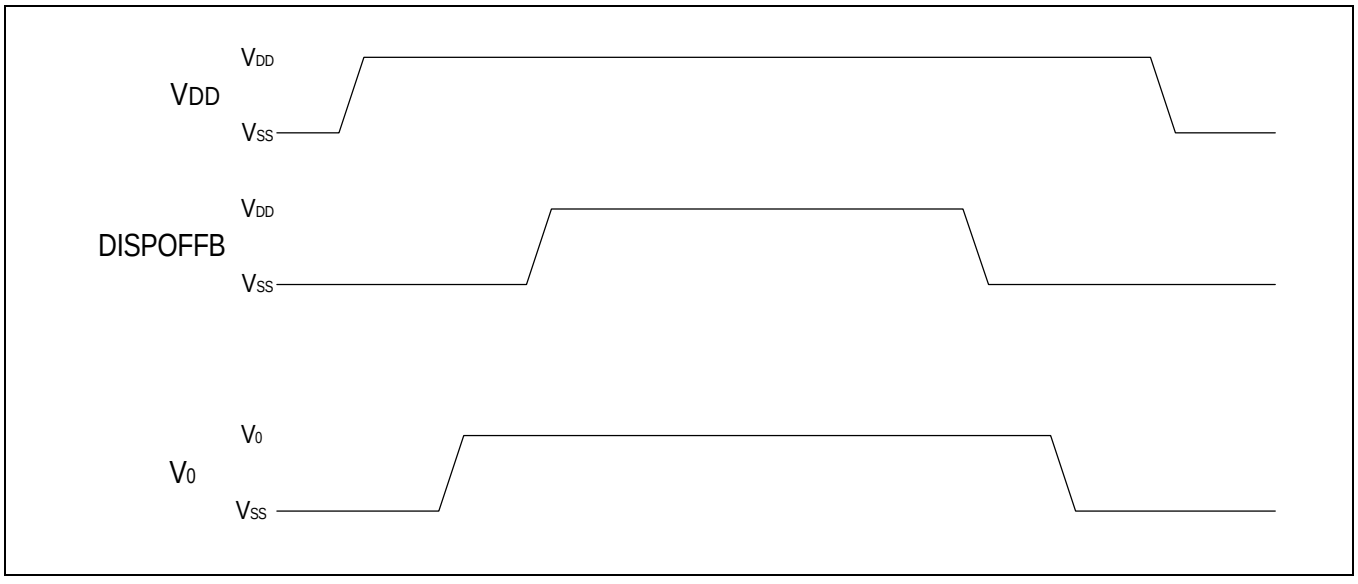

Figure 5. Connecting the Power Supply

CONNECTION EXAMPLES OF PLURAL SEGMENT DRIVERS

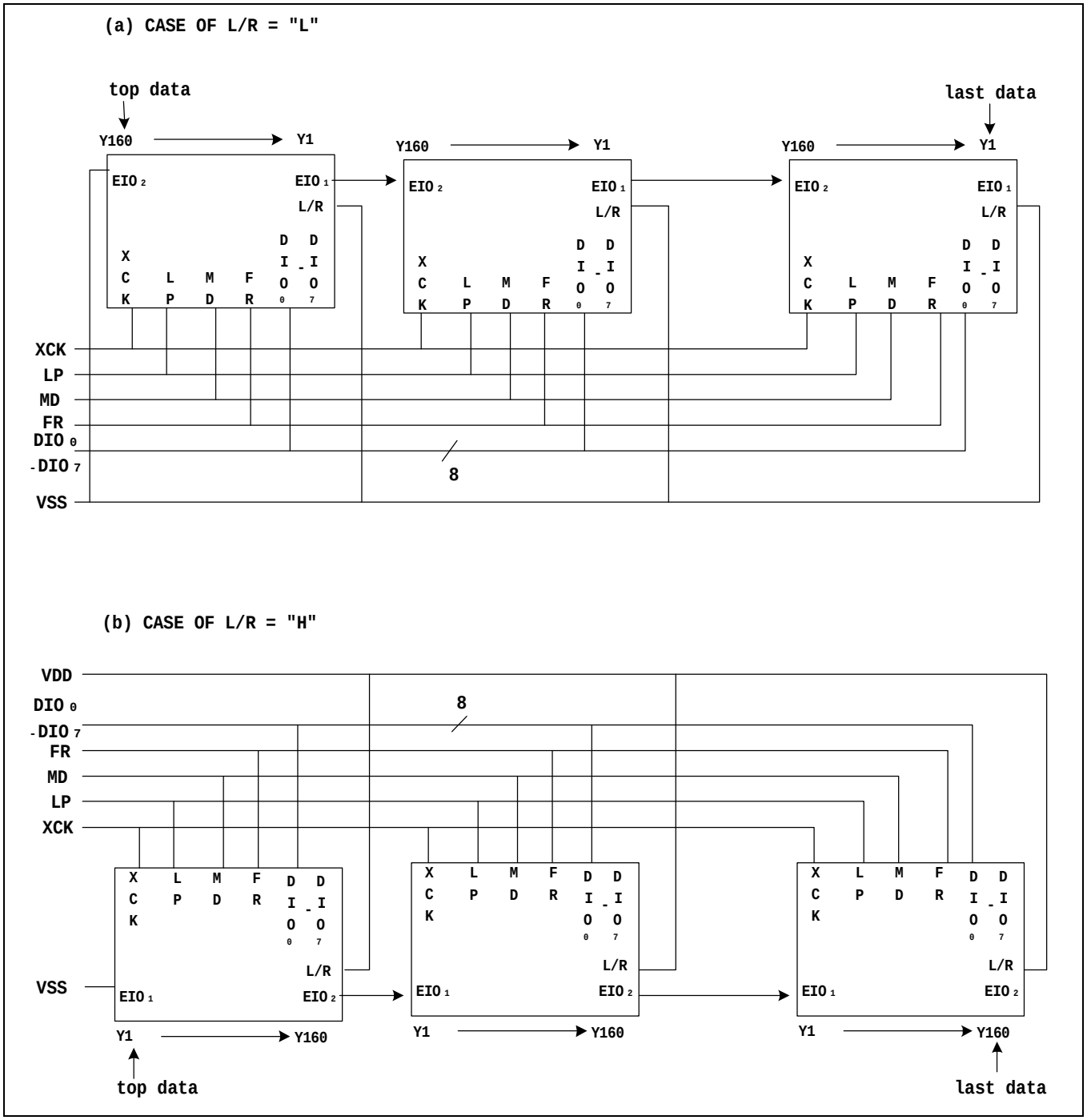

Figure 6

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TIMING CHART OF 4-DEVICE CASECADE CONNECTION OF SEGMENT DRIVERS

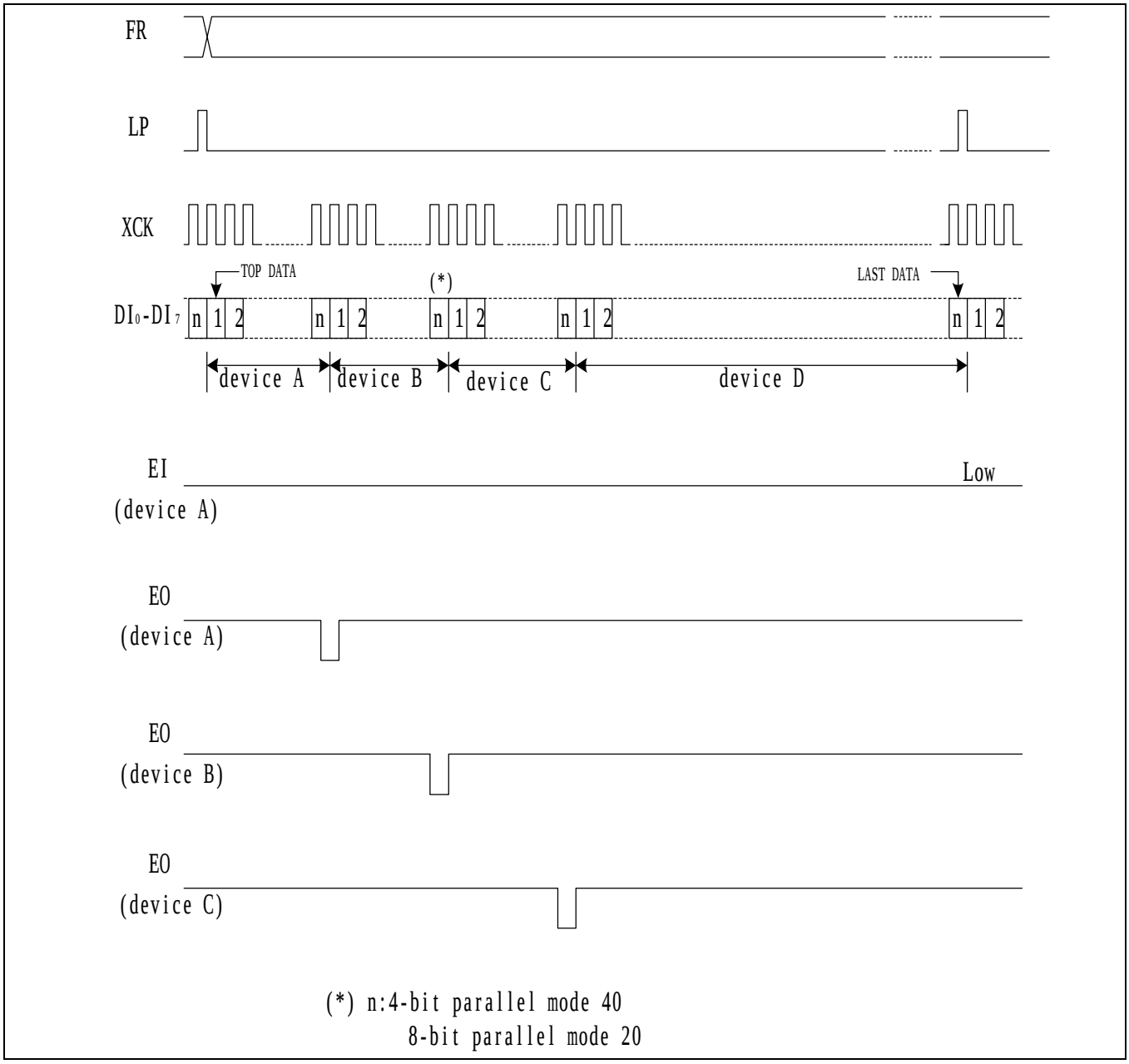
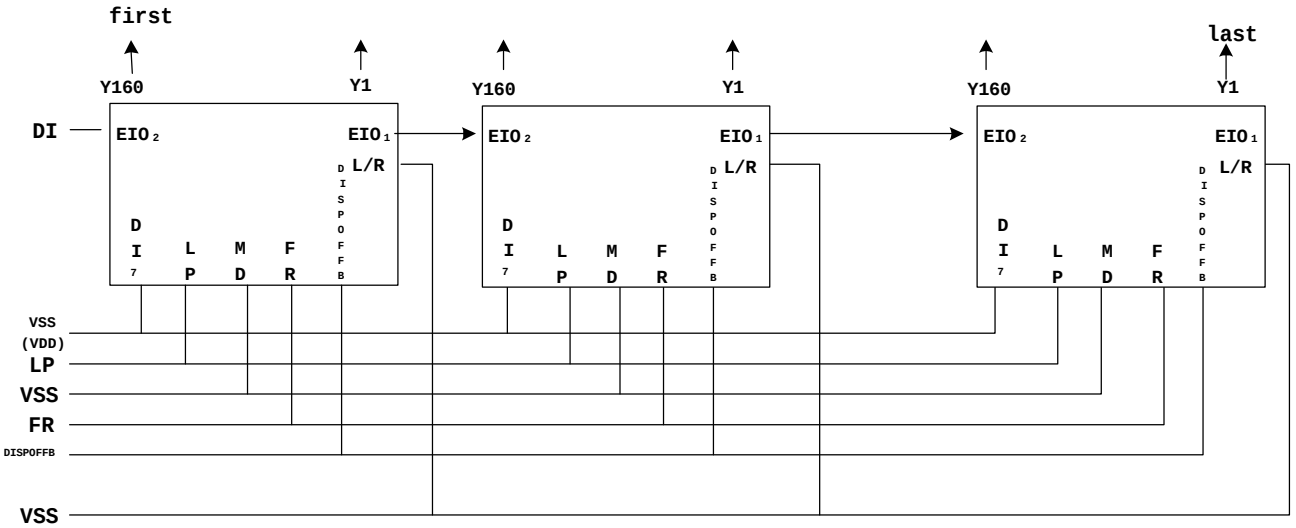


Figure 7

CONNECTION EXAMPLES OF PLURAL COMMON DRIVERS

(a) SINGLE MODE(SHIFTING TOWARD LEFT)



(b) SINGLE MODE(SHIFTING TOWARD RIGHT)

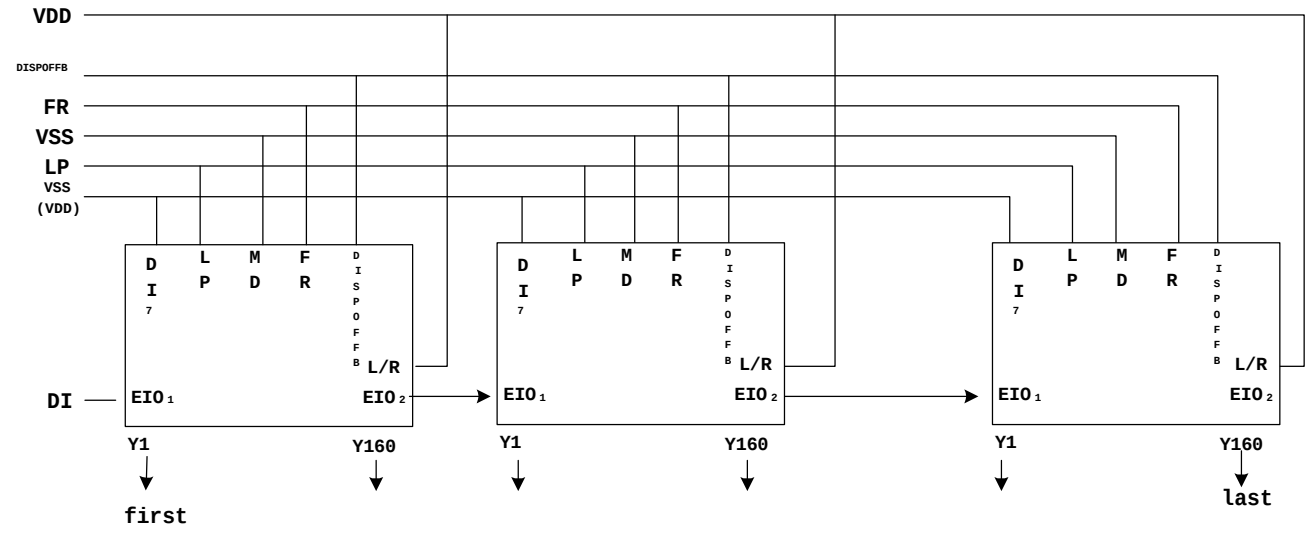
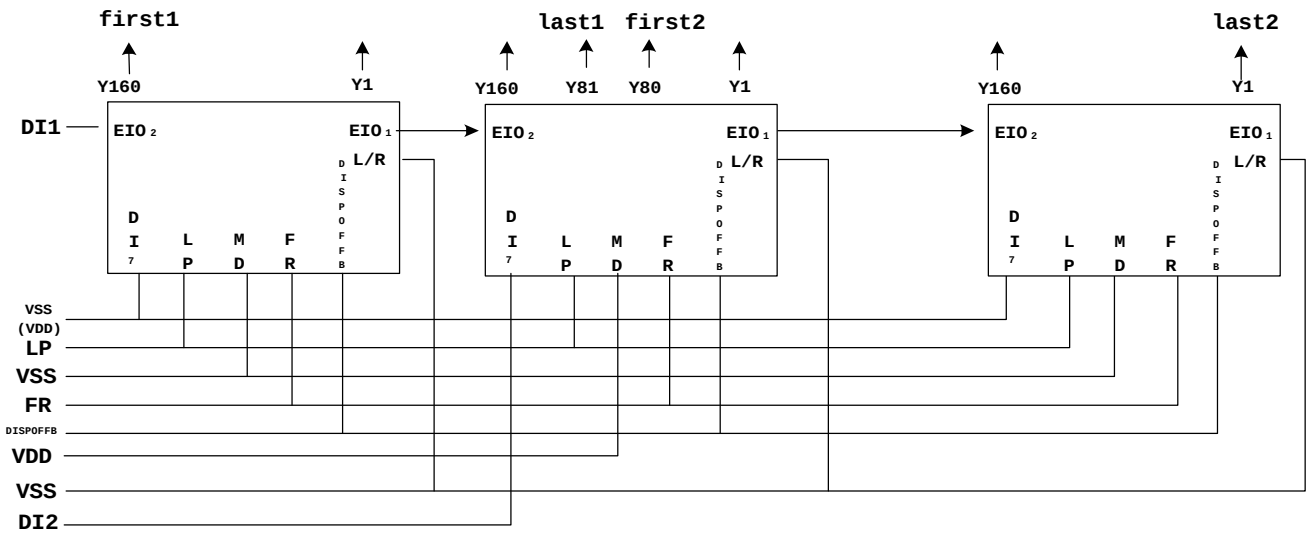


Figure 8

SAMSUNG ELECTRONICS

(c)DUAL MODE(SHIFTING TOWARD LEFT)



(d)DUAL MODE(SHIFTING TOWARD RIGHT)

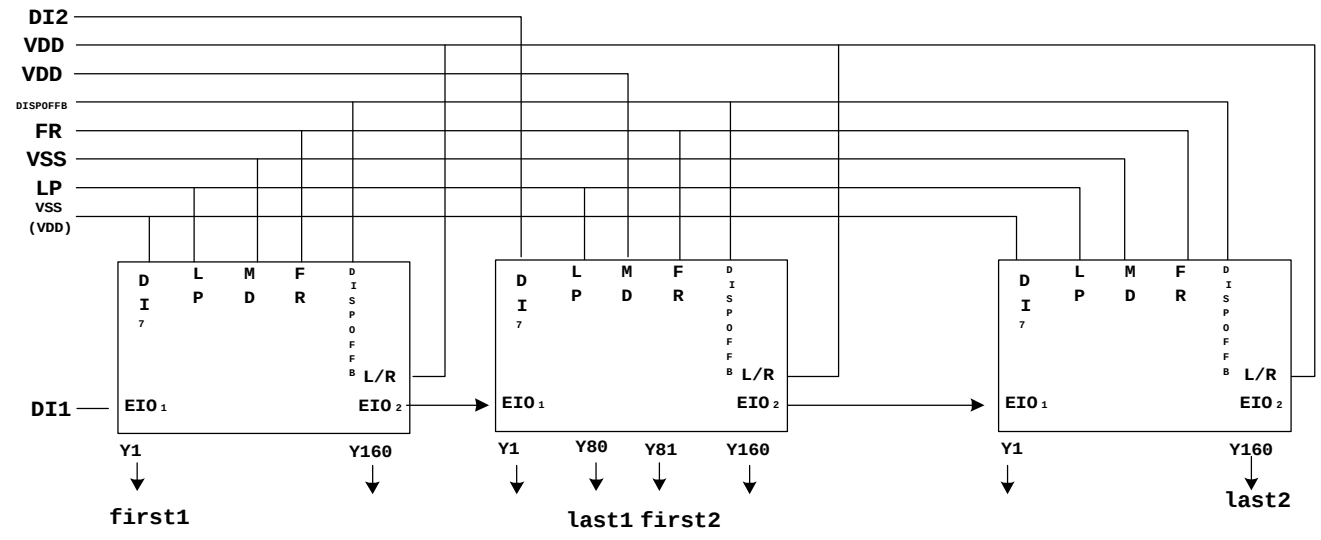


Figure 9