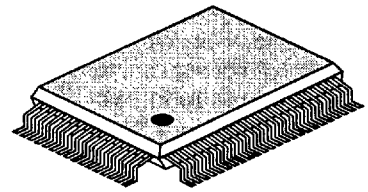
MULTISTANDARD VIDEO DECODER

The KS0122 converts analog NTSC or PAL video in composite or S-video format to digitized component video. Output data can be selected for CCIR 601 or square pixel sample rates in either YUV or RGB formats. All required clocks and video timing signals are generated. The KS0122 performs line lock tracking, AGC, ADC sampling, luma-chroma separation, luminance processing, color demodulation, chrominance processing, and format conversion. In addition, the ability to control the image's contrast, hue, saturation, brightness, and frequency response is provided.

100 PQFP



ORDERING INFORMATION

Device	Package	Temperature Range
KS0122	100 PQFP	0°~+70°C

FEATURES

- **Accepts NTSC-M and PAL-M/N/B/G/H formats with auto detection**
- **6 analog inputs: 3 S-video or 6 composite ports**
- **2 main AGC-clamp-ADC data paths**
- **Independent line and color burst synchronization**
- **Digital luma and chroma comb filters to achieve superior Y/C separation**
- **Full bandwidth decoding; horizontal resolution equivalent to 330 lines**
- **Programmable luma bandwidth, contrast, brightness, and edge enhancement**
- **Programmable chroma bandwidth, hue, and saturation**
- **Supports both square pixel and CCIR 601 output data rates**
- **Output in 8- or 16-bit YCbCr component, or 16-bit RGB 565 formats with dithering**
- **Power down mode**
- **3 or 2 wire serial interface**

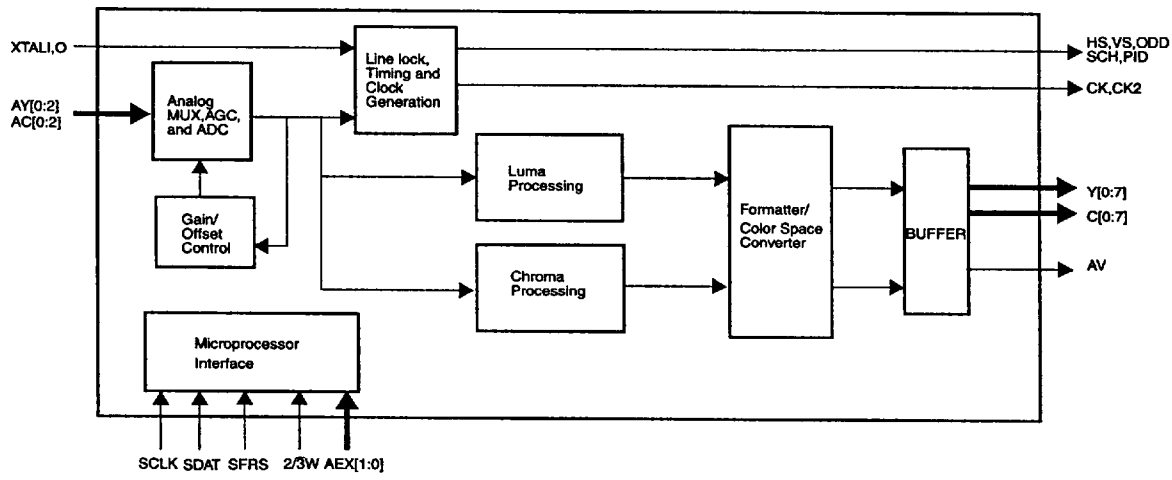
APPLICATIONS

- **Multimedia**
- **Digital Video**
- **Video Capture**
- **Video Editing**

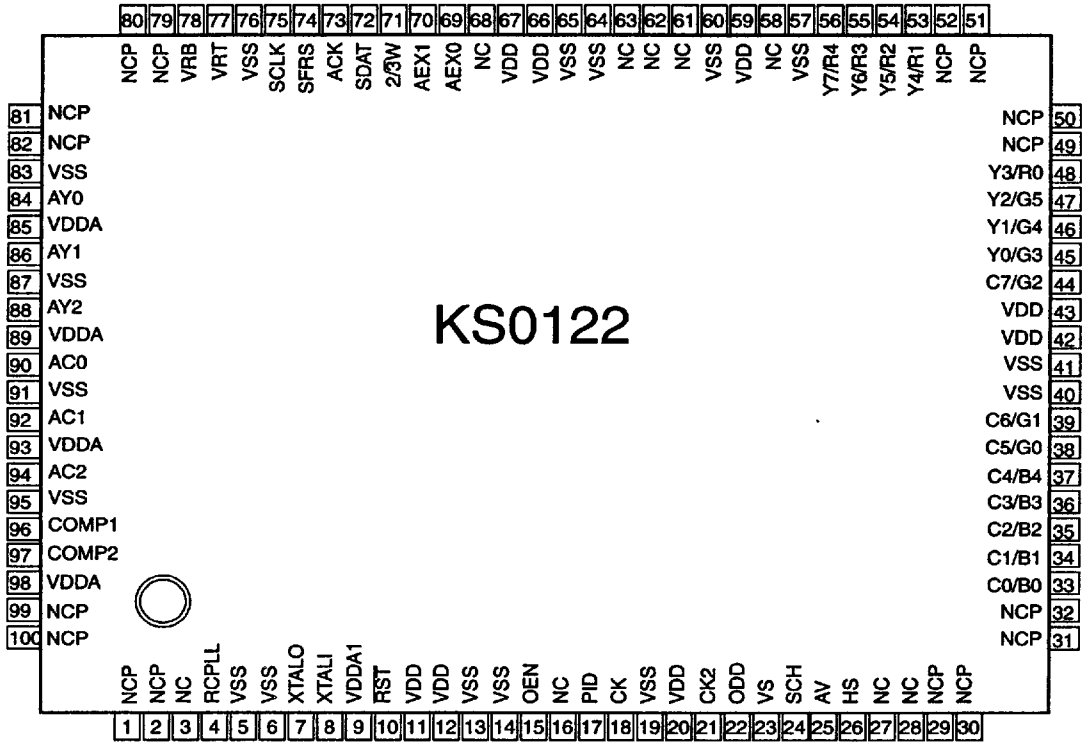
RELATED PRODUCT

- **KS0119 VIDEO ENCODER**

BLOCK DIAGRAM

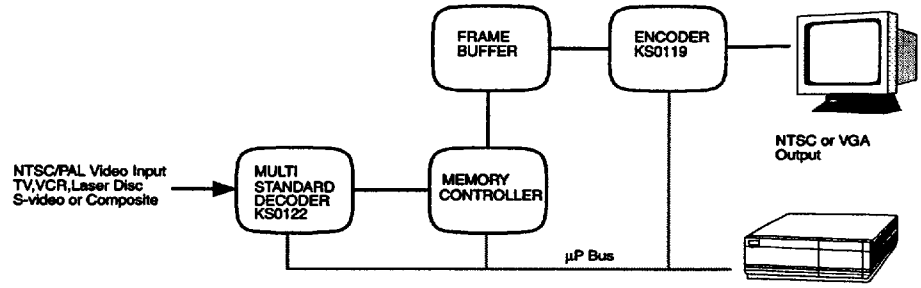


PIN ASSIGNMENT - 100 PQFP



TYPICAL APPLICATION

The KS0122 is shown in a typical application with the KS0119 NTSC Encoder.



PIN DESCRIPTION

Pin Name	Pin #	Type	Description
INPUT			
AY0 - AY2	84,86,88	I	Analog composite or luminance video input.
AC0 - AC2	90,92,94	I	Analog composite or chrominance video input.
XTALI	8	I	Pin1 for external crystal or TTL clock input.
XTALO	7	O	Pin 2 for external crystal.
RST	10	I	Chip reset. Active low signal.
OUTPUT (All output pins are three-statable)			
Y0/G3 - Y2/G5, Y3/R0 - Y7/R4	45-48,53-56	O	Digital video outputs for YCbCr or RGB data.
C0/B0 - C4/B4, C5/G0 - C7/G2	33-39,44	O	Digital video outputs for YCbCr or RGB data.
HS	26	O	User programmable horizontal timing signal. One pulse every video line.
VS	23	O	Vertical Sync.
ODD	22	O	Odd field flag. High for fields 1 and 3.
SCH	24	O	Color burst to sync phase (field 1or 3 detect, stable SCH data only).
PID	17	O	PAL ID flag. High for phase alternating line.
AV	25	O	Active video flag.
OEN	15	I	Digital video bus output enable. The video output signals can be 3-stated regardless the input on this pin if the **OENC[1:0]** bits in the **LUMA** register are set to 11 (binary).
CK	18	O	Pixel output clock.
CK2	21	O	Pixel output clock (rate is one half of CK) aligned to AV signal.
REFERENCE AND COMPENSATION			
VRT	77	I/O	ADC VRT compensation (requires an external 0.1 µF capacitor and a 1 kΩ resistor to VSSA).
VRB	78	I/O	ADC VRB compensation (requires an external 0.1 µF capacitor).
RCPLL	4	I/O	PLL filter (external RC filter is required).
COMP2	97	I/O	Internal 1.3 V reference decouple (requires an external 0.1 µF capacitor).
COMP1	96	I/O	Internal 1.5 V reference decouple (requires an external 0.1 µF capacitor).

PIN DESCRIPTION (Continued)

Pin Name	Pin #	Type	Description
HOST INTERFACE			
SFRS	74	I	Frame sync for 3-wire host interface.
SCLK	75	I	Serial clock.
SDAT	72	I/O	Serial data.
ACK	73	O	Write acknowledge for 2-wire serial mode.
2/3W	71	I	Selects 2 or 3 wire host interface.
AEX0 - AEX1	69 - 70	I	Device ID selection for host interface.
POWER AND GROUND			
VDD	11,12,20,42,43, 59,66,67	+5V	Digital power supply.
VDDA	85,89,93,98	+5V	Analog power supply.
VDDA1	9	+5V	Analog power supply.
VSS	5,6,13,14,19,40, 41,57,60,64,65, 76,83,87,91,95	GND	Common ground.
NC			
NC	3,16,27,28,58, 61-63,68	-	These pins are reserved and should not be connected.
NCP	1,2,29-32,49-52, 79-82,99,100	-	These pins are directly connected to the die substrate. They are intended as heat dissipation points. It is recommended that each corner set of 4 NCP pins be connected to as large as possible solid metal plane on the PCB component surface side. If electrical connect is desired (not required) only connection to VDDA is allowed.

PIN CROSS REFERENCE: NUMERICAL ORDER BY PIN NUMBER

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	NCP	26	HS	51	NCP	76	VSS
2	NCP	27	NC	52	NCP	77	VRT
3	NC	28	NC	53	Y4/R1	78	VRB
4	RCPLL	29	NCP	54	Y5/R2	79	NCP
5	VSS	30	NCP	55	Y6/R3	80	NCP
6	VSS	31	NCP	56	Y7/R4	81	NCP
7	XTALO	32	NCP	57	VSS	82	NCP
8	XTALI	33	C0/B0	58	NC	83	VSS
9	VDDA1	34	C1/B1	59	VDD	84	AY0
10	$\overline{RST}$	35	C2/B2	60	VSS	85	VDDA
11	VDD	36	C3/B3	61	NC	86	AY1
12	VDD	37	C4/B4	62	NC	87	VSS
13	VSS	38	C5/G0	63	NC	88	AY2
14	VSS	39	C6/G1	64	VSS	89	VDDA
15	OEN	40	VSS	65	VSS	90	AC0
16	NC	41	VSS	66	VDD	91	VSS
17	PID	42	VDD	67	VDD	92	AC1
18	CK	43	VDD	68	NC	93	VDDA
19	VSS	44	C7/G2	69	AEX0	94	AC2
20	VDD	45	Y0/G3	70	AEX1	95	VSS
21	CK2	46	Y1/G4	71	2/$\overline{3}$W	96	COMP1
22	ODD	47	Y2/G5	72	SDAT	97	COMP2
23	VS	48	Y3/R0	73	ACK	98	VDDA
24	SCH	49	NCP	74	SFRS	99	NCP
25	AV	50	NCP	75	SCLK	100	NCP

1. FUNCTIONAL DESCRIPTION

1.1. Analog Front End

The KS0122 has six analog video input pins. These inputs can be configured as six composite video sources, three S-video sources or a combination. The allowed pairings for the Y-C inputs are: AC0-AY0, AC1-AY1, and AC2-AY2. Inputs are selected using the **INSEL[3:0]** bits in the **CMDB** register. The input is ac coupled through a 0.1 µF external capacitor. Due to the high sampling rate of the ADCs inside the KS0122 most video sources will not require a LPF for alias reduction. For those video sources with data above 13 MHz, a low pass filter with a simple single pole at 6 MHz will provide sufficient high frequency signal reduction. This can be implemented with a 400 pF cap in parallel with the 75 Ω load. Timing mismatch in S-video mode can be compensated with the **YDEL[2:0]** bits in the **CMDE.** Unused video inputs can be connected to VSS, VDD, or left floating.

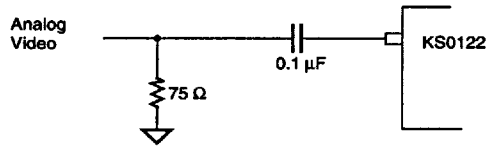


Figure 1. Typical Analog Video Input

As shown in Figure 2, the KS0122 has two complete internal analog paths, each including analog gain control, clamping control, and an 8-bit ADC. For composite video input, only the luma path is used. For S-video input, both the luma and chroma paths are utilized. Both ADCs operate at twice the output pixel rate to ease the requirement for the external analog anti-alias filter. The ADC digital data is used to calculate the correct gain and clamp values. The data is fed back to the analog clamping and gain control. This architecture eliminates any offset and gain mismatch in the analog front end.

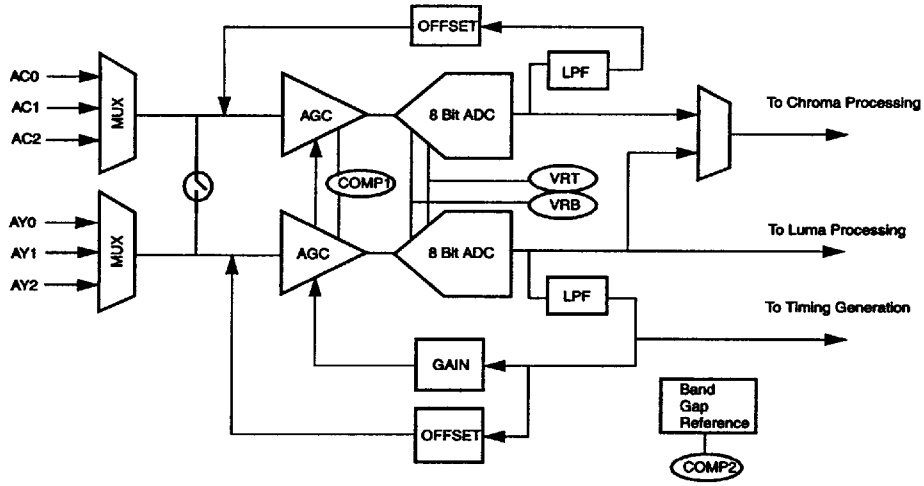


Figure 2. Analog Front End

The AGC normally references to sync tip, back porch delta. Video signal with abnormal sync tip or very bright saturated colors may cause the ADC to limit the maximum value. The user can enable the **AGCOVF** bit in the

CMDB register to force the gain tracking loop to reduce AGC when maximum limiting conditions occur. The AGC may also be programmed to freeze the AGC at the current value by setting the **AGCFRZ** bit in the **CMDB** register. Once the AGC is frozen, the gain can be manually adjusted with the **AGC** register.

The COMP1, COMP2, VRT, and VRB pins shown in Figure 2 are internal voltage reference nodes. Each needs to be decoupled with an external 0.1 µF capacitor placed as close as possible to the pin. VRT also requires a 1k resistor to VSS.

1.2. External Clock Reference

The KS0122 requires an external reference clock to track the analog video input. This reference (at 24.576 MHz or 26.8 MHz) can be supplied via a crystal using the on chip crystal interface or any TTL compatible source. These configurations are shown in Figure 3

The reference frequency selection should be based upon the intended operating modes of the KS0122. For CCIR 601 operation, the 24.576 MHz reference is recommended. For square pixel or dual mode operation, the 26.8 MHz reference is recommended. A reference of 50 ppm or better is required.

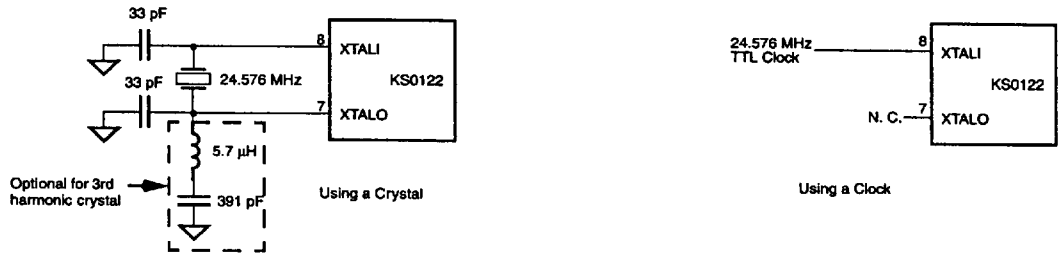


Figure 3. Standard Clock Configurations

The internal clock generation circuits require an external analog filter for the on-chip PLL as shown in Figure 4. These three components should be placed as close as possible to pin 4. The internal biasing circuits require a decoupling capacitor for pins COMP1 and COMP2 (pins 96 and 97).

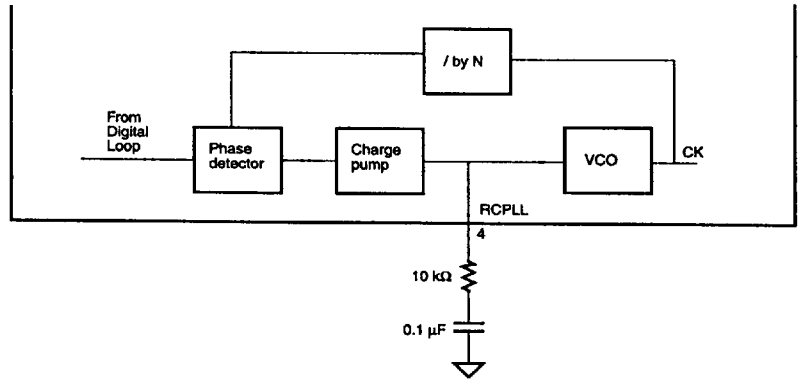


Figure 4. Analog PLL and RC Filter

1.3. Video Tracking

One of the critical functions of the KS0122 is to generate a time-base-corrected sampling clock. The KS0122 contains a sophisticated digital tracking system to support analog video sources with various signal conditions, such as VCR (with head switching), single field VCR, and noisy TV signals. The **HFSEL[1:0]** bits in the **CMDA** register are used to select different tracking algorithms. For all conditions except noisy broadcast, the **HFSEL** bit should be set to VCR mode (**HFSEL[1:0]**=01).

To ensure that samples are aligned horizontally, vertically in time, the sampling clock is generated by multiplying the line rate by N. The required N factor for the KS0122 is based upon the detected field rate (60 Hz or 50 Hz) and the desired sampling rates (CCIR 601 or square pixel). Field rate is automatically detected and can be monitored with the **FFRDET** bit in the **STAT** register. The **PIXSEL** bit in register **CMDD** selects CCIR 601 or square pixel. Table 1 shows the constants for the various combinations of input formats and output pixel rates.

Table 1: Timing for Different Pixel Rates

	CCIR 601 Data Rates				Square Pixel Data Rates				Units
	NTSC-M	PAL-B/G/H	PAL-M	PAL-N	NTSC-M	PAL-B/G/H	PAL-M	PAL-N	
Line Time	63.55	64.0	63.55	64.0	63.55	64.0	63.55	64.0	µS
Field Rate	60	50	60	50	60	50	60	50	Hz
Pixels/Line (N)	858	864	858	864	780	944	780	944	Pixels
Active Pixels/Line	720	720	720	720	640	768	640	768	Pixels
Active Lines/Frame	480	580	480	580	480	580	480	580	Lines
Pixel Rate	13.5	13.5	13.5	13.5	12.27	14.75	12.27	14.75	MHz
ADC Sampling Rate	27	27	27	27	24.54	29.5	24.54	29.5	MHz
Color Modulation Frequency	3.579	4.43	3.575	3.582	3.58	4.43	3.575	3.582	MHz

1.4. Luminance Processing Unit

The luminance path separates the luma from the CVBS for composite video input, provides digital filtering to reduce noise, enhances image quality, and adjusts contrast and brightness levels. Figure 5 shows the block diagram.

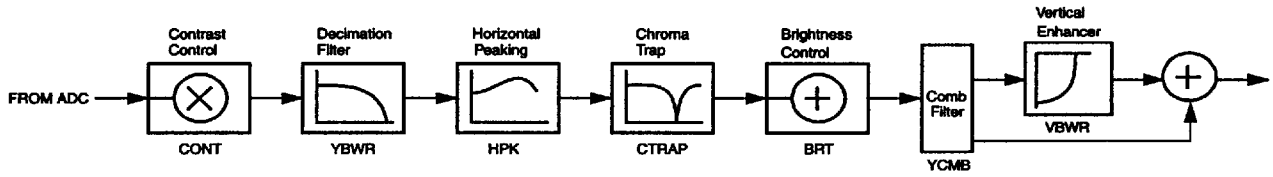


Figure 5. Luminance Processing Unit

1.4.1. Luminance Separation and Frequency Shaping

The CVBS or luma data is over-sampled at twice the output pixel rate. This high sampling rate, when combined with the decimation filter, reduces harmonic spurs folding into baseband and increases the luma resolution. The **YBWR** bit in the **LUMA** register allows the luminance bandwidth to be reduced when the video input contains high frequency noise. Video image edge sharpness can be adjusted via the **HPK[1:0]** bits in the **LUMA** register.

A programmable chroma trap can be disabled if the input is S-video format. The KS0122 also includes a programmable one or two line luminance comb filter to further separate the luminance from composite video. The filtering characteristics of the comb filter which control the luminance vertical bandwidth can be controlled with the **VBWR** bit in the **CMDC** register.

The luminance filter characteristics have been designed to be very similar for all combinations of 60/50 Hz video and CCIR 601/square pixel sampling rates. Figure 6 through Figure 13 show the output characteristics of the luminance path with different filter combinations for the supported input standards and output pixel rates.

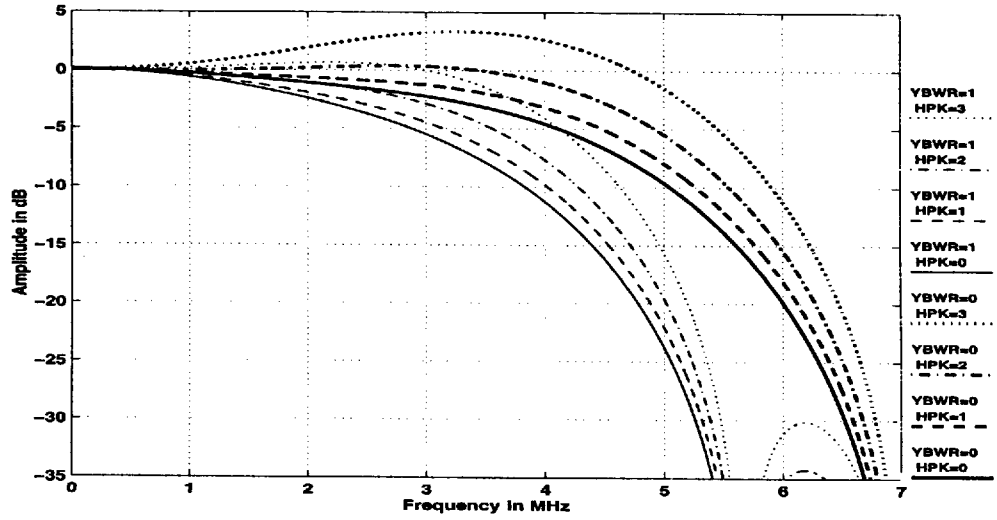


Figure 6. S-Video (CTRAP=0), CCIR 601, NTSC

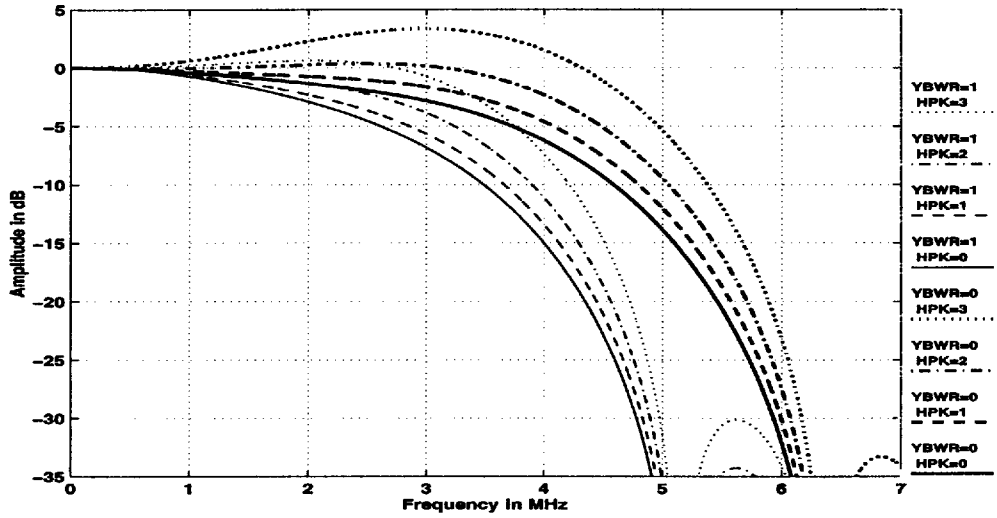


Figure 7. S-Video (CTRAP=0), Square Pixel, NTSC

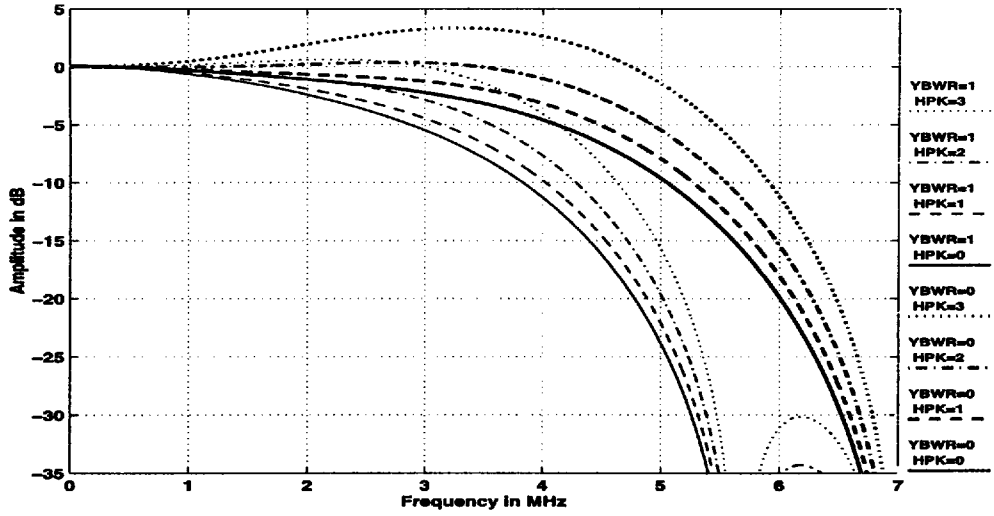


Figure 8. S-Video (CTRAP=0), CCIR 601, PAL

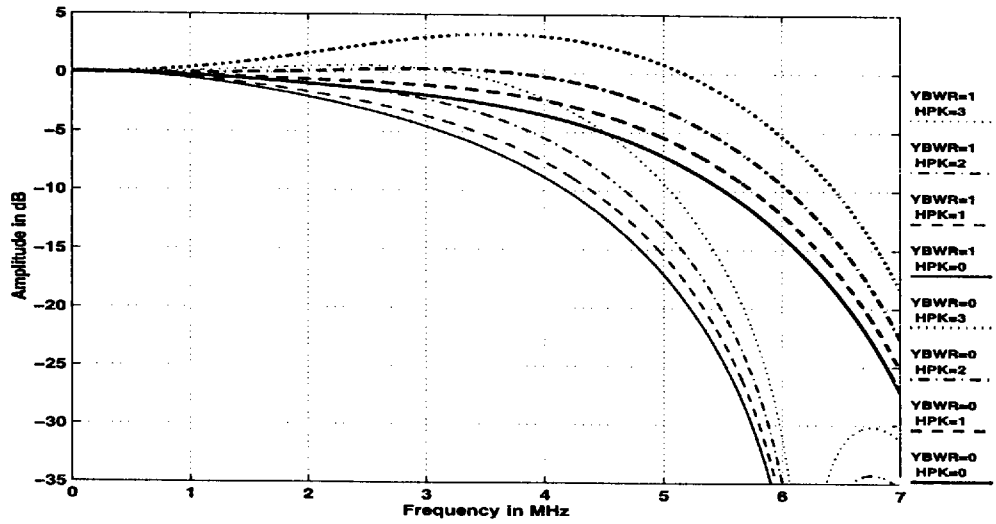


Figure 9. S-Video (CTRAP=0), Square Pixel, PAL

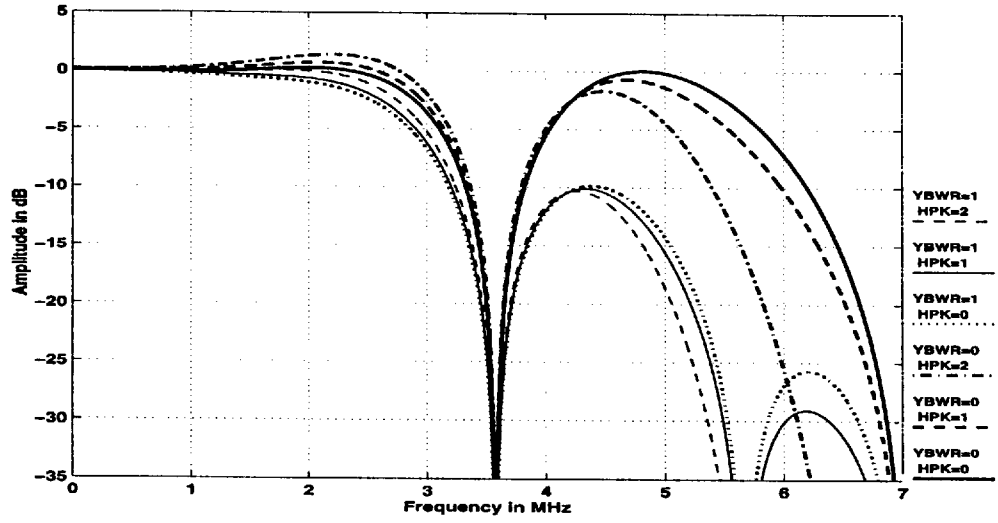


Figure 10. Composite Video (CTRAP=1), CCIR 601, NTSC

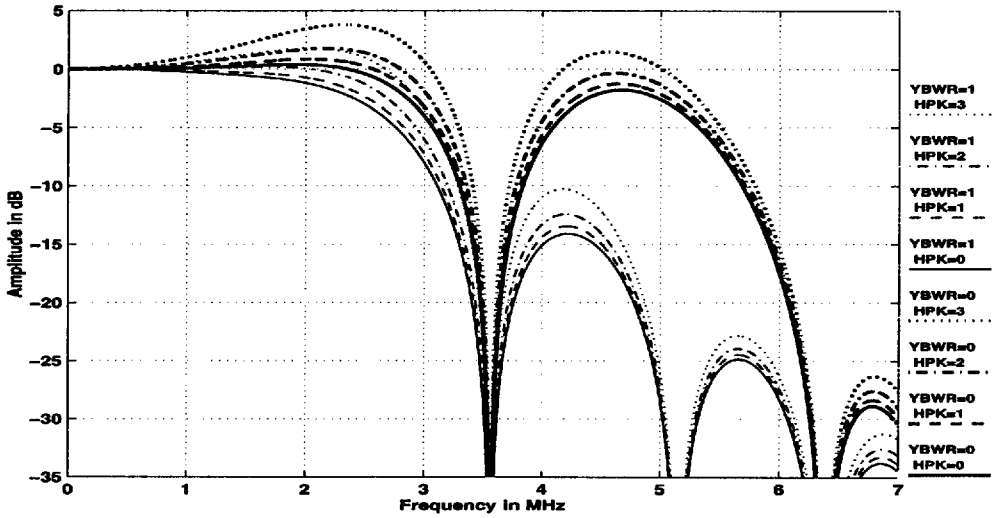


Figure 11. Composite Video (CTRAP=1), Square Pixel, NTSC

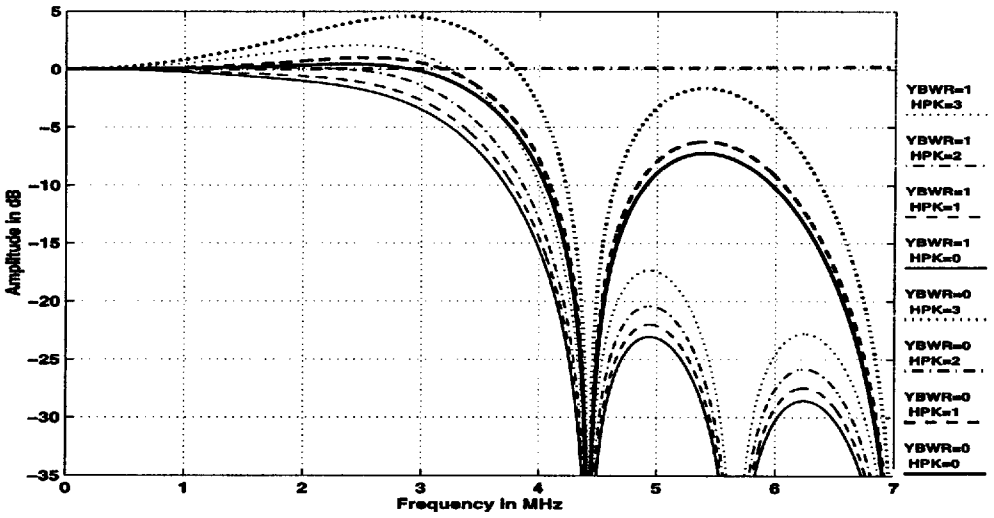


Figure 12. Composite Video (CTRAP=1), CCIR 601, PAL

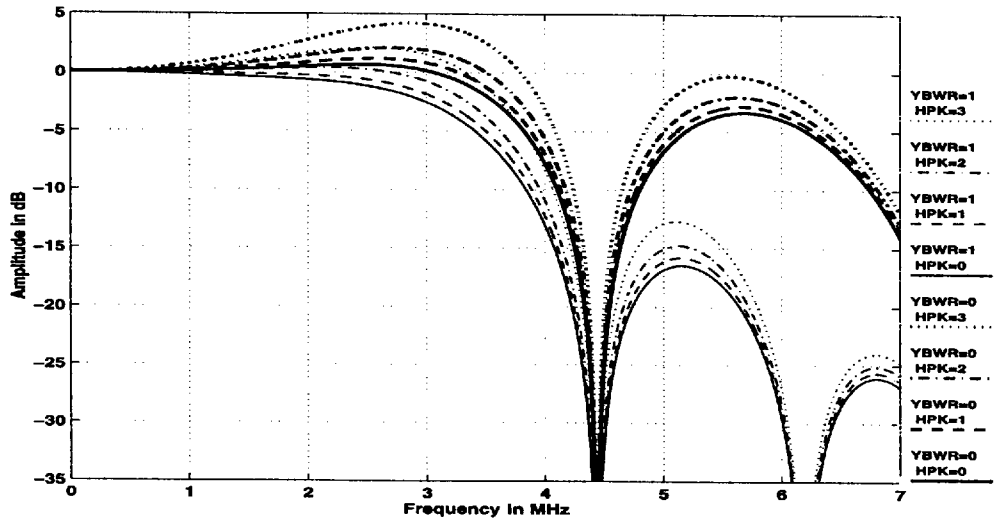


Figure 13. Composite Video (CTRAP=1), Square Pixel, PAL

1.4.2. Luminance DC Gain

The KS0122 can accommodate CCIR 624 M/N/H/G standards, which fall into categories of -40 or -43 sync tip and inclusion or exclusion of 7.5 IRE setup. The KS0122 can produce correct CCIR 601 luminance output levels by controlling the gain and offset in the luminance path via the **PED** bit in the **LUMA** register. This register should be set for the appropriate input standard. The programmable **CONT** and **BRT** registers provide the user with additional flexibility to create non-standard luminance gain and offset values.

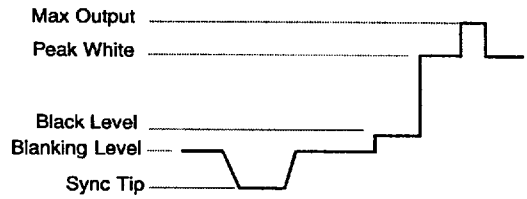


Figure 14. Luminance Signal

Luminance levels produced by the KS0122 for different broadcast standards (assuming **CONT**=0 and **BRT**=0) are summarized in Table 2.

Table 2: Luminance Digital Level Code

	NTSC/PAL- M/N (w/ Pedestal) - PED=1			NTSC/PAL- M/N (w/o Pedestal) - PED=0			PAL- B/G/H PED=1		
Signal	Level (IRE)	ADC (CVBS)	Y[7:0] Code	Level (IRE)	ADC (CVBS)	Y[7:0] Code	Level (IRE)	ADC (CVBS)	Y[7:0] Code
Max Input	109	255	255	109	255	255	117	255	255
Peak White	100	240	235	100	240	235	100	229	235
Black	7.5	83	16	0	70	16	0	70	16
Blank	0	70	1	0	70	16	0	70	16
Sync	-40	2	1	-40	2	1	-43	2	1
KS0122 data Path equation	$C_Y = 1.37CVBS-100$			$C_Y = 1.288CVBS-74$			$C_Y = 1.37CVBS-80$		

When digital component output is desired in RGB mode, the **RGBH** bit in the **LUMA** register can be programmed to increase the 0-100% values from standard CCIR 601 levels to full range levels.The gain variations are shown in Table 3.

Table 3: RGB Output Range

	RGB normal gain (RGBH=0)		RGB high gain (RGB=1)	
Signal	Cy	RGB (U,V=0)	Cy	RGB (U,V=0)
Peak White	235	235	255	255
Black	16	16	0	0

1.5. Chrominance Processing Unit

Data from the composite or chroma S-video ADC is routed to the chroma data path depending on the input type selection. This chroma data can be NTSC or PAL type color encoding. The KS0122 will automatically determine the color encoding method and adjust the tracking algorithm. Due to the limited frequency tracking range of any video chroma loop, some type of information as to chroma center frequency must be fed into the tracking loop. The KS0122 infers a NTSC-M 3.579 MHz chroma modulation frequency when a 60Hz video signal is detected. A 50 Hz video signal infers a 4.43 MHz chroma signal. These assumptions can be override with the **PALN** and **PALM** bits found in register **CMDB**.

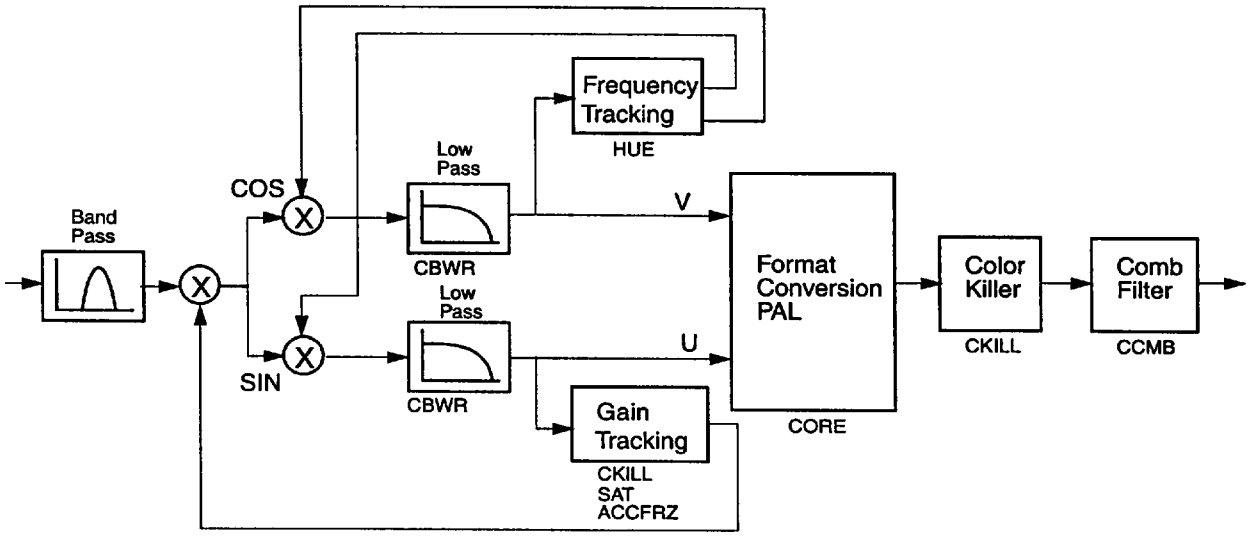


Figure 15. Chrominance Processing Unit

An optional 1 line chroma comb filter can be enabled to reduce luma leakage into the chroma path. The control is via the **CCMB** bit in the **CMDC** register. The comb filter offers the trade-off between chroma vertical resolution and luma cross interference. This comb filter can be disabled when the input is S-video.

The chroma horizontal bandwidth can be varied between 550 KHz and 850 KHz with the **CBWR** bit in the **CHRM** register. These selections offer the trade-off between chroma bandwidth and luminance interference. For S-video input, the **CBWR** bit should be set to maximum bandwidth. The frequency response of the chroma path is shown in Figure 16 for CCIR 601 output format data.

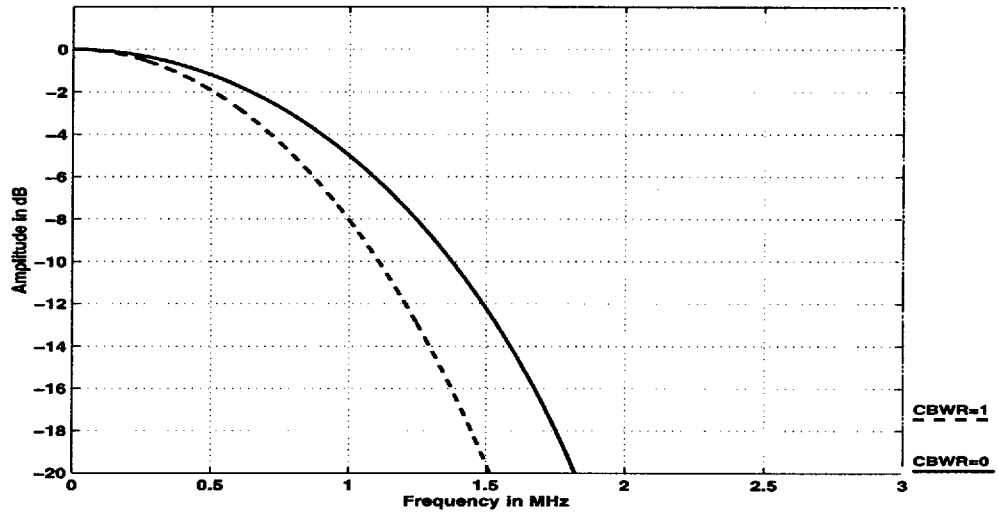


Figure 16. NTSC/PAL Input, CCIR 601 Output

The chroma channel can be programmed to automatically suppress the color burst if the amplitude is too small. This allows auto detection of black and white video. The chroma output can be manually disabled or forced on independent of color burst level. The **CKILL[1:0]** bits in the **CHRM** register are used to select the different color kill options.

The saturation of the color can be varied via the 8-bit **SAT** register. The **ACCFRZ** bit in the **CHRM** register can be set to 1 to freeze the saturation at its current value. Once the **ACCFRZ** bit is set to 1, the function of the **SAT** register is disabled. The phase reference for the frequency tracking loop may be adjusted using the 8-bit **HUE** register. This register provides an 8 bit reference dispersed across the 360° hue range.

The chrominance path offers a coring option to reduce low level noise to zero. Coring may be selected via the **CORE[1:0]** bits in the **CMDD** register. When coring is enabled, any chroma data within code levels 128±1 or 128±3 is forced to 128, depending on whether 1- or 2-lsb coring is selected.

1.6. Formatter and Color Space Converter

The formatter, color space converter receives the luma and chroma data and converts it to the selected output format. The KS0122 can output in various YUV and RGB digital formats selectable via the **OFMT[1:0]** bits in register **CMDC**. Table 4 shows the supported output formats.

Table 4: Digital Video Output Formats

Pin	Clock Alignment (CK2)							Clock Alignment (CK)			
	4:2:2 OFMT=0		4:1:1a OFMT=1				RGB 565 OFMT=2	CCIR 656 YC OFMT=3			
	2N	+1	4N	+1	+2	+3	N	4N	+1	+2	+3
C0/B0	Cb0	Cr0					B0				
C1/B1	Cb1	Cr1					B1				
C2/B2	Cb2	Cr2					B2				
C3/B3	Cb3	Cr3					B3				
C4/B4	Cb4	Cr4	Cr6	Cr4	Cr2	Cr0	B4				
C5/G0	Cb5	Cr5	Cr7	Cr5	Cr3	Cr1	G0				
C6/G1	Cb6	Cr6	Cb6	Cb4	Cb2	Cb0	G1				
C7/G2	Cb7	Cr7	Cb7	Cb5	Cb3	Cb1	G2				
Y0/G3	Y0	Y0	Y0	Y0	Y0	Y0	G3	Y0	Cb0	Y0	Cr0
Y1/G4	Y1	Y1	Y1	Y1	Y1	Y1	G4	Y1	Cb1	Y1	Cr1
Y2/G5	Y2	Y2	Y2	Y2	Y2	Y2	G5	Y2	Cb2	Y2	Cr2
Y3/R0	Y3	Y3	Y3	Y3	Y3	Y3	R0	Y3	Cb3	Y3	Cr3
Y4/R1	Y4	Y4	Y4	Y4	Y4	Y4	R1	Y4	Cb4	Y4	Cr4
Y5/R2	Y5	Y5	Y5	Y5	Y5	Y5	R2	Y5	Cb5	Y5	Cr5
Y6/R3	Y6	Y6	Y6	Y6	Y6	Y6	R3	Y6	Cb6	Y6	Cr6
Y7/R4	Y7	Y7	Y7	Y7	Y7	Y7	R4	Y7	Cb7	Y7	Cr7

The color space converter uses the following equations for conversions from YUV to RGB:

$$R = C_Y + 1.375C_R$$
$$G = C_Y + (-0.703)C_R + (-0.328)C_B$$
$$B = (C_Y + 1.734C_B)$$

1.7. Synchronization Signals

The KS0122 internal tracking loops create a sampling clock that is phase and frequency locked to the video sync tip. In addition to providing the pixel clock, the KS0122 also outputs necessary timing signals to locate the first and last pixels, to indicate the beginning of a line, a field, and to identify the field. All the timing and clock pins may be optionally put into high impedance state.

The KS0122 can also generate all the video timing without video input. This enables the KS0122 to be used as a video timing generator for a system that contains both the KS0122 for live video input and a MPEG decoder.

1.7.1. Horizontal Timing

The KS0122 creates many internal timing signals aligned to the horizontal sync tip. These include timing for locations of color burst used in chrominance processing, along with back porch, and sync tip timing signals used for AGC and clamp functions.

The KS0122 includes two external horizontal timing signals. The HS signal has no function inside the KS0122. It is provided as a user programmable signal that sends a pulse every video line. The start and stop locations of the pulse can be programmed via the 2's compliment **HSE** and **HSB** registers. Default values provide a pulse whose rising edge is aligned with the delayed video sync tip.

The AV is an active high signal indicating that active video is being output. When the signal is low, the output is forced to blank with no color. The two registers **AVB** and **AVE** are used to control the start and stop locations of the AV signal. Care must be taken to specify the correct number of active video pixels. As with the HS signal, the default value 0 for **AVB** and **AVE** defines an AV pulse at the correct default location with the correct number of active pixels (e.g. 720 pixels for CCIR 601 format). The approximate signal locations are shown in Figure 17.

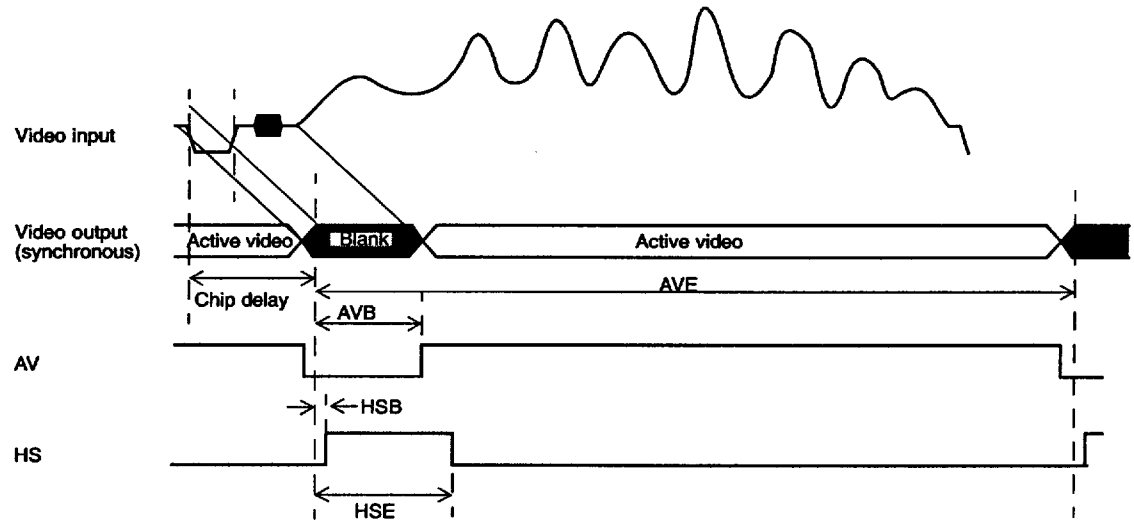


Figure 17. Timing for HS and AV

Table 5 shows the default edge locations relative to the video sync tip as it would appear at the Y[7:0] pins, as well

as the maximum and minimum programmable ranges for each of the possible operating mode. Note the numbers shown are in multiple of CK clocks relative to the delayed horizontal sync tip.

Table 5: Programmable Range for AV and HS (in Number of CK Clocks)

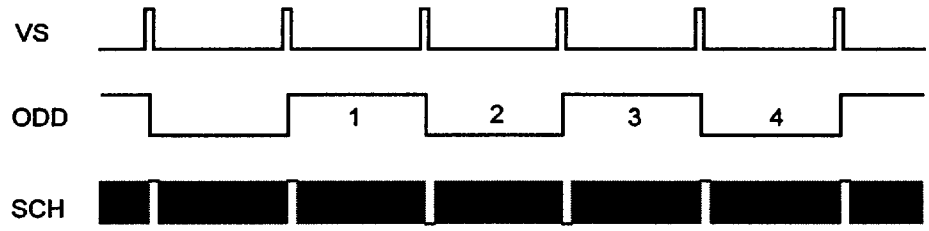
	NTSC (60 Hz)						PAL (50 Hz)					
	CCIR 601			Square Pixel			CCIR 601			Square Pixel		
	min	default	max	min	default	max	min	default	max	min	default	max
AVB	115	243	370	107	235	362	128	256	383	170	298	425
AVE	1555	1683	1810	1387	1515	1643	1568	1696	1823	1707	1834	1962
HSB	-128	0	127	-128	0	127	-128	0	127	-128	0	127
HSE	142	270	398	117	245	373	142	270	398	167	295	423

1.7.2. Vertical Timing

The vertical timing signals include VS, ODD, SCH, and PID. The VS is an active high signal which is used for identifying the first line of video in the vertical position. The VS signal's rising edge is based upon an internal low pass filter. Its rising location is dependent on the noise conditions of the video input. The falling edge of the vertical sync is locked to either the beginning of the video line or half way. The half way location relative to the beginning of the video line changes depending on current input standard and output format. The **VSE** bit in the **CMDA** register can be programmed to shorten the VS falling edge by one horizontal line.

The ODD signal signifies the current field number. When ODD is high, the current field is 1 or 3 (or 5 or 7 if in PAL mode). The signal may be used in conjunction with SCH and PID to exactly identify the current field. Although the ODD status can be determined by using the AV and VS signals with minimal external logic, it is recommended that the ODD signal be used. The KS0122 has extensive internal circuits that generate the correct ODD sense even when tracking single field video sources such as consumer VCR in trick mode.

To distinguish between fields 1, 2 verse fields 3, 4 (or fields 1, 2, 3, 4 verse fields 5, 6, 7, 8 for PAL) the phase of the color burst relative to the sync tip must be measured. That information is provided by the SCH pin. The KS0122 provides the output of a comparator that measures whether the current color burst phase is greater or less than a predetermined constant. This constant is controlled with the **SCHCMP[3:0]** bits in the **CMDE** register. The polarity of the SCH output pin depends on the current **SCHCMP[3:0]** value. The SCH signal changes every video line. The SCH for line 260 is held for the entire vertical blanking period. By using the SCH signal for the same line from each field, proper field identification can be determined. Figure 18 shows field identification values for **SCHCMP[3:0]**=0. It is important to note that the SCH value is only valid for video signals that have a constant sync tip to color burst relationship. This is not the case with consumer VCRs.



Truth Table

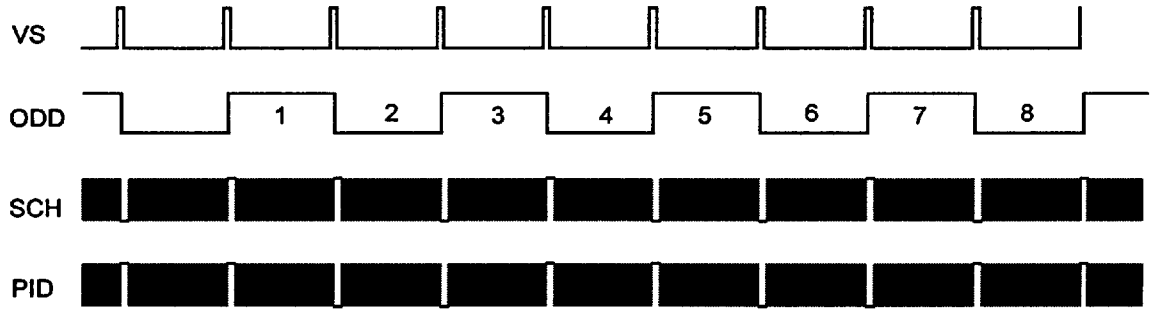
FIELD	1	2	3	4
ODD	H	L	H	L
SCH	H	L	L	H

Note:
ODD and SCH are measured at the falling edge of VS.

Figure 18. NTSC Vertical Timing Signals

The PID pin is used to identify whether the current V-axis is inverted in PAL mode. This signal changes at the color burst. By noting this value at the same line of each field, a determination of whether a field is from {1-4} or {5-8} can be made. As with the SCH pin, the KS0122 is designed to hold the line 260 PID measurement for the entire vertical blank period. This allows easy sampling of the PID or current field identification.

The ODD, SCH and PID signals change at different times and more than once within the video fields. Proper data for field identification is determined by latching all three signals at the falling edge of VS. Figure 19 shows the VS, ODD, SCH, and PID signals and their latched values for each of the 8 possible fields.

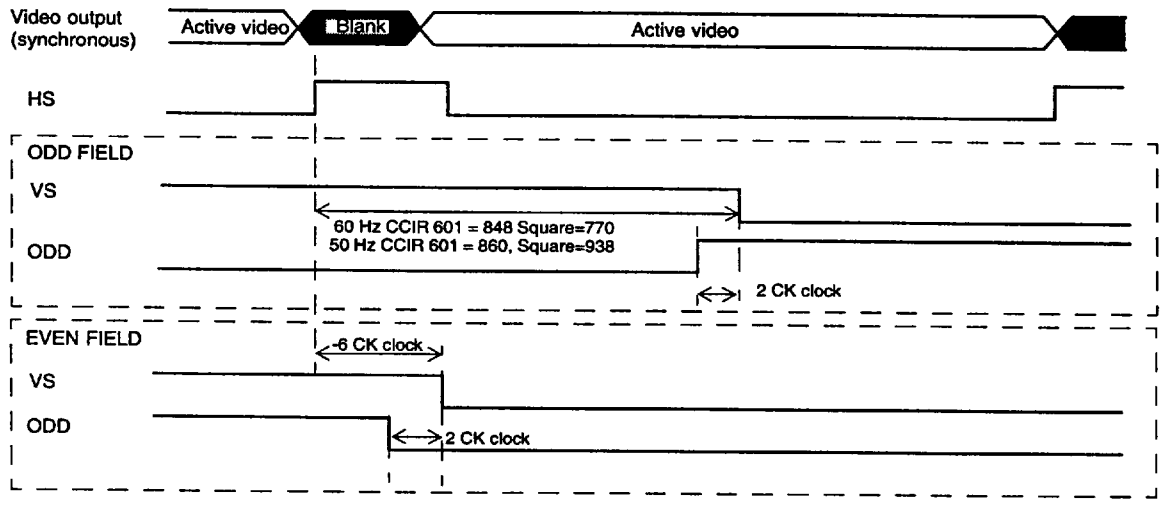


Truth Table

FIELD	1	2	3	4	5	6	7	8
ODD	H	L	H	L	H	L	H	L
SCH	H	H	L	H	L	L	H	L
PID	H	L	L	H	H	L	L	H

Note:
ODD, SCH and PID are measured at the falling edge of VS.

Figure 19. PAL Vertical Timing Signals



Note: Numbers shown are with default **HSB** and **HSE** register settings.

Figure 20. Short Term Vertical Timing

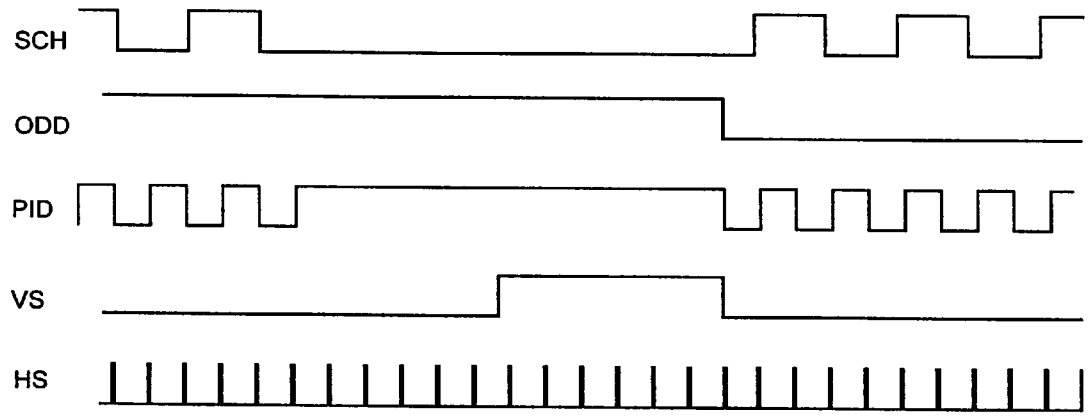


Figure 21. Line to Line VS,SCH and PID Timing (PAL input)

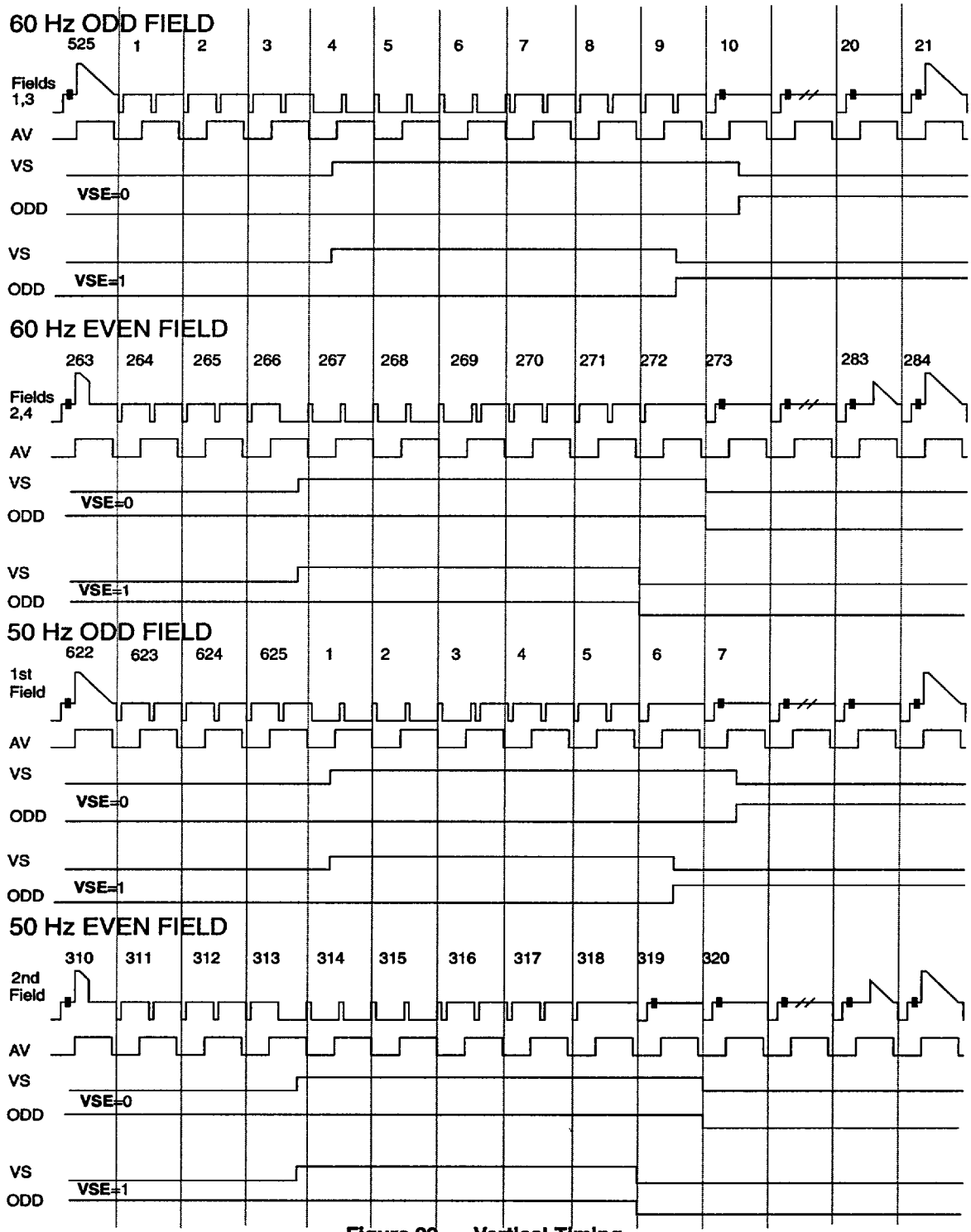


Figure 22. Vertical Timing

1.8. Digital Video Output

The KS0122 has a sixteen-bit wide, tri-statable digital video output bus. The video data is clocked out by the CK2 (CK if output is CCIR 656 YC format) pixel clock. The Y and C data is aligned with the AV signal as shown in Figure 23. To ease board design, up to three valid pixels are provided before the rise of AV and after the fall of AV, otherwise, the Y output is forced to 16 and the C output is forced to 128.

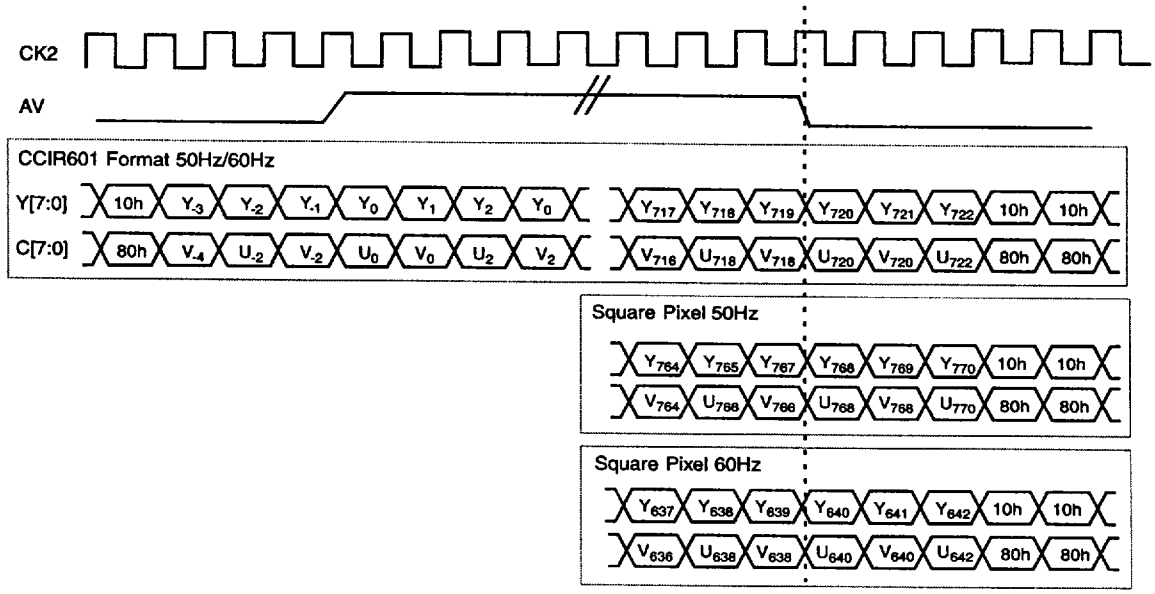


Figure 23. Data Output for 4:2:2 Format

2. HOST INTERFACE

The KS0122 provides two serial host interface protocols to communicate to the internal registers. The selection of the two interfaces is controlled through the 2/3W pin. The KS0122 always functions as a slave device. This means that the KS0122 will never initiate a data transfer.

The KS0122 contains two types of registers: an index register used for indirect data register access, and a set of data registers.

2.1. Three Wire Serial Interface

The three wire serial interface is selected by connecting the 2/3W to ground. This interface uses three signals: SFRS, SDAT, and SCLK. The SFRS indicates a valid data transfer. Serial data is carried through the SDAT and clocked in or out with the SCLK. The data protocol sends each byte as msb first.

2.1.1. Three Wire Write/Read to KS0122

Each data transfer cycle is called a frame. A valid frame is indicated by a HIGH on the SFRS signal. A frame consists at least three bytes: the first byte contains a 7-bit slave device ID and a R/W bit (bit assignment shown in Figure 24); the second byte indicates which type of register the data transfer is intended for (00h for index, 01 for data); and the third and consequent byte(s) are the data to be transferred to/from the register. If the data transfer is to/from the index register, three bytes are needed each frame. Since the KS0122 features an auto index increment function, consecutive data transfer to/from the data registers can be completed within the same frame.

The KS0122 may be configured with one of four slave device ID's using the AEX1 and AEX0 pins. Up to 4 KS0122's can be used in the same system by configuring each device with a unique device ID.

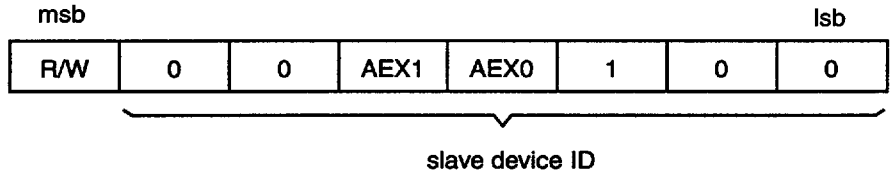


Figure 24. 3-wire Device ID and R/W

Figure 25 shows an example of a write to the index register. Each bit is latched into the device by the rising edge of the SCLK. A write to the data register is similar to a write to the index register except the second byte is 01h and the third and so on byte(s) are the data to be written (Figure 26). When the data is read from the device, the KS0122 outputs each bit is after the falling edge of the SCLK.

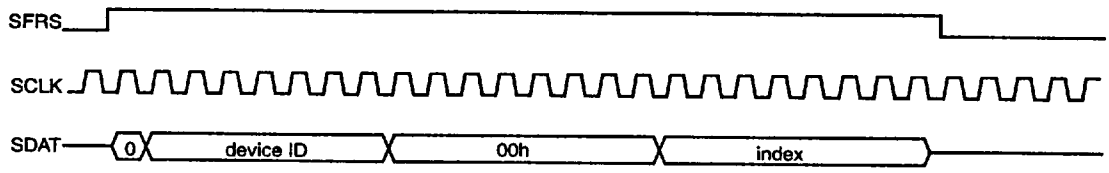


Figure 25. 3-wire Write to Index Register

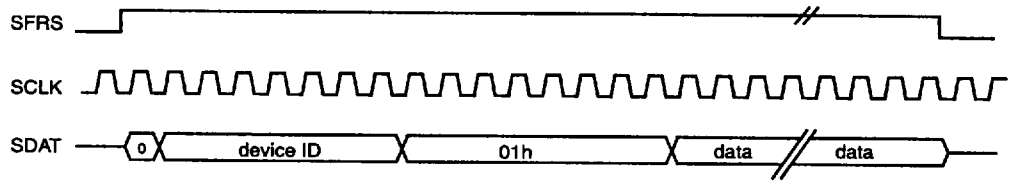


Figure 26. A Typical 3-wire Write to Data Register

2.2. Two Wire Serial Interface

The two wire interface consists of the SCLK and SDAT signals. There is no dedicated qualifying signal like the SFRS used in the three wire interface. Data can be written to or read from the KS0122. For both read and write, each byte is transferred msb first. For both read and write, the data bit is valid when the SCLK is high.

2.2.1. Two Wire Write to KS0122

The host initiates a transfer cycle with a START signal. The START signal is HIGH to LOW transition on the SDAT while the SCLK is high. The host then sends a byte consisting of the 7-bit slave device ID and a 0 in the R/W bit. The arrangement for the slave device ID and the R/W bit is depicted in Figure 27. AEX1 and AEX0 are configuration pins used to configure the KS0122 to use one of the four addresses. Up to four KS0122's can be used in one system each with a unique address.

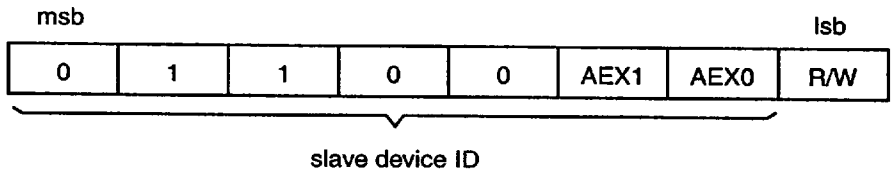


Figure 27. 2-wire Slave Device ID and R/W

The second byte the host sends is the base register index. The host then sends the data. The KS0122 increments

the index automatically after each byte of data is sent. Therefore, the host can write multiple bytes to the slave if they are in sequential order. The host completes the transfer cycle with a STOP signal which is a LOW to HIGH transition when the SCLK is high.

Each byte transfer consists of 9 clocks. When writing to the KS0122, the ACK pin can be wired to the SDAT pin so that an acknowledge signal is created during the 9th clock.

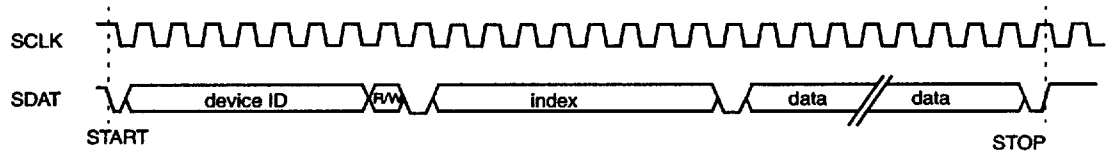


Figure 28. 2-wire Data Write

2.2.2. Two Wire Read from KS0122

The read cycle takes two START-STOP phases. The first phase is a write to the index. The second phase is the read from the data register.

The host initiates the first phase by sending the START signal. It then sends the slave device ID along with a 0 in the R/W position. The index is then sent followed by the STOP signal.

The second phase also starts with the START signal. It then sends the slave device ID but with a 1 in the R/W position to indicate data is to be read from the slave device. The host uses the SCLK to shift data out from the KS0122.

3. CONTROL REGISTER DESCRIPTION

This section contains information concerning the programmable control registers. Table 6 provides the default power up values for each index, the recommended values and a brief description of the function. The recommended values are for composite video at input AY0 assuming 24.576 MHz reference and CCIR 601 output data. The following pages describe each location in detail and the possible programing values (the * indicates the power-on default).

Table 6: Register Summary

Index	Mnemonic	Power Up Default	Recommended Values	Description
00h	STAT	-	-	Read Only Status Bits
01h	CMDA	00h	28h	Control Register A
02h	CMDB	00h	20h	Control Register B
03h	CMDC	00h	00h	Control Register C
04h	CMDD	00h	08h	Control Register D
05h	CHRM	44h	40h	Chroma Control Register
06h	LUMA	05h	05h	Luma Control Register
07h	CONT	00h	00h	Luma Contrast Control
08h	BRT	00h	00h	Luma Brightness Control
09h	SAT	00h	00h	Chroma Saturation Control
0Ah	HUE	00h	00h	Chroma Hue Control
0Bh	AGC	60h	60h	Video Y/C AGC Override Control
0Ch	AVB	00h	00h	AV Signal Begin
0Dh	AVE	00h	00h	AV Signal End
0Eh	HSB	00h	00h	HS Signal Begin
0Fh	HSE	00h	00h	HS Signal End
10h	TESTA	00h	00h	Test register.
11h	FRUN	00h	00h	Free Run Control
12h	TESTC	00h	00h	Test registers.
13h	TESTD	00h	00h	
14h	CMDE	00h	00h	Control Register E

Read Only Status Bits									
Index	Mnemonic	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00h	STAT	-	-	-	FFRDET	PALDET	CDET	-	-

CDET Status for detection of color. This can be used to poll existence of video
- 0 No color signal detected.
- 1 Color signal detected.

PALDET Status for current detected color format.
- 0 NTSC color format.
- 1 PAL color format.

FFRDET Status for current detected field frequency.
- 0 50 Hz field frequency, i.e. M system.
- 1 60 Hz field frequency, i.e. N/B/G/H system.

Control Register A									
Index	Mnemonic	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01h	CMDA	XT26	VBIE	1	HFSEL1	HFSEL0	VSE	0	0

VSE — Change the ending location for the VS.

- 0 Line 10/10.5.*
- 1 Line 9/9.5.

HFSEL[1:0] — Selects between standard algorithm and tracking algorithm optimized for VCR.

- 0 Extreme head switch VCR.
- 1 Standard VCR source - use for most video.
- 2 Good quality video - Laser Disc, test source.
- 3 Noisy broadcast source.

VBIE — Vertical Master Mode enable

- 0 Normal vertical sync operation.*
- 1 Vertical sync ignores input and free runs at 50 or 60 Hz (depending on settings of **MNFMT** and **IFMT**). The **FRUN** register must be set to 14 (hex) for this mode to work. This mode can be used to generate timing for a slave device.

XT26 — Select the external clock reference frequency.

- 0 External clock is 24.5 MHz.
- 1 External clock is 26.8 MHz.

Control Register B									
Index	Mnemonic	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
02h	CMDB	PALM	PALN	AGCOVF	AGCFRZ	INSEL3	INSEL2	INSEL1	INSEL0

INSEL[3:0] Analog input channel select.

- 0x0 Y0 is composite input.*
- 0x1 Y1 is composite input.
- 0x2 Y2 is composite input.
- 0x4 C0 is composite input.
- 0x5 C1 is composite input.
- 0x6 C2 is composite input.
- 0x8 Y0 is Luminance input, C0 Chrominance input.
- 0x9 Y1 is Luminance input, C1 Chrominance input.
- 0xA Y2 is Luminance input, C2 Chrominance input.

AGCFRZ Freeze the analog AGC for the Y and C paths at their current values. When high, the current gain value for the Y and C AGCs can be read or set using the AGC register.

- 0 AGC is running. Reading AGC register returns register setting not current AGC gain.*
- 1 AGC is frozen. Gain can be changed or read with AGC register.

AGCOVF AGC gain control mode.

- 0 AGC gain tracks to sync tip and back porch.*
- 1 If ADC overflows, AGC gain will be reduced (this has higher priority over normal sync tip - back porch tracking).

PALN Selection between PAL-N and PAL-B/G/H tracking algorithm in the chroma processing unit when 50 Hz field rate is detected.

- 0 Select PAL-B/G/H tracking algorithm.*
- 1 Select PAL-N tracking algorithm.

PALM Selection between PAL-M and NTSC-M tracking algorithm in the chroma processing unit when 60 Hz field rate detected.

- 0 Select NTSC-M tracking algorithm.*
- 1 Select PAL-M tracking algorithm.

Control register C									
Index	Mnemonic	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
03h	CMDC	VBWR	0	YCMB1	YCMB0	0	CCMB	OFMT1	OFMT0

OFMT[1:0] Digital video data output format select.
- 0 YUV 4:2:2 format.*
- 1 YUV 4:1:1a format.
- 2 CCIR 656 YC format.
- 3 RGB 565 format.

CCMB Chroma comb filter control.
- 0 Chroma comb filter is on.*
- 1 Chroma comb filter is disabled.

YCMB[1:0] Luma comb filter control.
- 0 Comb filter is on. Auto selection 1-2 line comb.*
- 1 1 line comb filter.
- 2 2 line comb filter.
- 3 No comb filter.

VBWR Reduce vertical bandwidth while increasing chroma rejection from comb filter.
- 0 Maximum vertical bandwidth.*
- 1 Vertical bandwidth reduced.

Control Register D									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
04h	**CMDD**	POWDN	0	0	CORE1	CORE0	MNFMT	PIXSEL	IFMT

IFMT — Manual input standard select. Format selection can be controlled automatically if **MNFMT**=0.
- 0 Input field rate is 60 Hz.*
- 1 Input field rate is 50 Hz.

PIXSEL — Select pixel sampling rate.
- 0 Output data is at CCIR 601 rate.*
- 1 Output data is at square pixel rate.

MNFMT — Manual input format control override. When this bit is 1 the **IFMT** bit is enabled.
- 0 Input video standard is detected automatically.*
- 1 Input video standard is selected with the **IFMT** bit.

CORE[1:0] — Chroma coring - forces chroma signals with small amplitude to zero (code 128).
- 0 No chroma coring.*
- 1 1 lsb chroma coring.
- 2 2 lsb chroma coring.

POWDN — Power down mode.
- 0 Normal operation.*
- 1 All chip functions except microprocessor interface and CK/CK2 generation are disabled. In power down mode the output frequency of the CK/CK2 pins is not locked but is within 5% of nominal frequency.

Chroma Control Register									
Index	Mnemonic	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
05h	CHRM	ACCFRZ	1	0	CBWR	0	0	CKILL1	CKILL0

CKILL[1:0] Chroma color killer.

- 0 Auto mode. If the color burst amplitude is low, then chroma data is suppressed.*
- 2 Chroma output is always enabled.
- 3 Chroma output is always suppressed (no color).

CBWR Chroma bandwidth reduction control.

- 0 Chroma 3 dB point at 850 kHz.*
- 1 Chroma 3 dB point at 550 kHz.

ACCFRZ Color gain freeze control.

- 0 Normal operation - on and tracking input.*
- 1 Frozen at current saturation value.

Luma Control Register									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
06h	**LUMA**	OENC1	OENC0	RGBH	PED	YBWR	CTRAP	HPK1	HPK0

HPK[1:0] Luminance 3 MHz peaking control.
- 0 Peaking less than nominal.
- 1 Nominal peaking.*
- 2 Increased peaking.
- 3 Even higher peaking.

CTRAP Luminance channel chroma notch filter. Location depends on **IFMT** and **PIXSEL**.
- 0 No chroma trap. Used for composite test signals or S-Video.
- 1 Chroma trap enabled. Used for most composite sources.*

YBWR Luminance bandwidth reduction.
- 0 Full bandwidth.*
- 1 Reduced bandwidth.

PED Enable gain correction for 7.5 IRE black level (pedestal).
- 0 No pedestal 0 IRE = CCIR 601 code 16.*
- 1 Pedestal enabled 7.5 IRE = CCIR 601 code 16.

RGBH Selects high gain mode for RGB output data.
- 0 RGB output data for input of 0%-100% are 4-56, 8-118, and 4-56, respectively.*
- 1 RGB output data for input of 0%-100% are 0-63, 0-127, and 0-63, respectively.

OENC[1:0] Video data and timing signal output 3-state control.
- 0 3-state video data output when OEN input is low.*
- 1 3-state video data output plus VS, HS, ODD, PID, SCH, and AV when OEN is low.
- 2 3-state everything above plus CK and CK2 when OEN is low.
- 3 3-state all the above outputs regardless what state OEN input is.

Luma Contrast Control									
Index	Mnemonic	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
07h	CONT	CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0

CONT[7:0] Contrast control register. The value contained in the register is in 2's compliment format. The default value of 0 provides standard CCIR 601 luminance gain.

Luma Brightness Control									
Index	Mnemonic	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
08h	BRT	BRT7	BRT6	BRT5	BRT4	BRT3	BRT2	BRT1	BRT0

BRT[7:0] Brightness control register. The value contained in the register is in 2's compliment format. The nominal value is 0. Each lsb change corresponds to 1 lsb change in the luminance code.

Chroma Saturation Control									
Index	Mnemonic	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
09h	SAT	SAT7	SAT6	SAT5	SAT4	SAT3	SAT2	SAT1	SAT0

SAT[7:0] Color saturation control register (2's compliment). The nominal saturation corresponds to the register value 0. The more positive the register value the more the saturation.

Chroma Hue Control									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0Ah	**HUE**	HUE7	HUE6	HUE5	HUE4	HUE3	HUE2	HUE1	HUE0

HUE[7:0] Hue control register. The value contained in this register is in 2's compliment format. It covers the range from -180° to +180° with a resolution of 1.41°/lsb.

Video Y/C AGC override control									
Index	**Mnemonic**	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
0Bh	**AGC**	AGC7	AGC6	AGC5	AGC4	AGC3	AGC2	AGC1	AGC0

AGC[7:0] If AGC is frozen (**FRZ0**=1) then this byte controls the AGC gain stage. The value contained in the register is unsigned.

AV Signal Begin									
Index	Mnemonic	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0Ch	AVB	AVB7	AVB6	AVB5	AVB4	AVB3	AVB2	AVB1	AVB0

AVB[7:0] This register is used to control the leading edge of the AV output signal. The leading edge location of the AV is relative to the start of the horizontal sync of the video in number of CK clocks. It is calculated by adding the register content (in 2's complement) to a nominal value (corresponding to the register content of 0x00). Some examples of the register values and their AV leading edge locations are shown below.

Register Content	CCIR 601		Square Pixel	
	NTSC	PAL	NTSC	PAL
0x80	115	128	107	170
0xFF	242	255	234	297
0x00*	243	256	235	298
0x01	244	257	236	299
0x7F	370	383	362	425

AV Signal End									
Index	Mnemonic	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0Dh	AVE	AVE7	AVE6	AVE5	AVE4	AVE3	AVE2	AVE1	AVE0

AVE[7:0] This register is used to control the trailing edge of the AV output signal, in very much the same way as the AVB. Some examples are shown below.

Register Content	CCIR 601		Square Pixel	
	NTSC	PAL	NTSC	PAL
0x80	1555	1568	1387	1706
0xFF	1682	1695	1514	1833
0x00*	1683	1696	1515	1834
0x01	1684	1697	1516	1835
0x7F	1810	1823	1643	1962

HS Signal Begin									
Index	Mnemonic	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0Eh	HSB	HSB7	HSB6	HSB5	HSB4	HSB3	HSB2	HSB1	HSB0

HSB[7:0] This register is used to control the leading edge of the HS output signal. The leading edge location of the HS is relative to the start of the horizontal sync of the video in number of CK2 clocks. It is calculated by adding the register content (in 2's complement) to the nominal value of 0. Some examples of the register values and their HS leading edge locations are shown below.

0x80 -128.

0xFF -1.

0x00 0.*

0x01 1.

0x7F 127.

HS Signal End									
Index	Mnemonic	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0Fh	HSE	HSE7	HSE6	HSE5	HSE4	HSE3	HSE2	HSE1	HSE0

HSE[7:0] This register is used to control the trailing edge of the HS output signal, in very much the same way as the HSB. Some examples are shown below.

Register Content	CCIR 601		Square Pixel	
	NTSC	PAL	NTSC	PAL
0x80	142	142	117	167
0xFF	269	269	244	294
0x00*	270	270	245	295
0x01	271	271	246	296
0x7F	398	398	373	423

Free Run Control									
Index	Mnemonic	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
11h	FRUN	FRUN7	FRUN6	FRUN5	FRUN4	FRUN4	FRUN3	FRUN2	FRUN1

FRUN[7:0] This register controls whether the KS0122 tracks the input video for timing generation or free runs without tracking the input.

0x00 Timing generation tracks input video.*

0x14 Free run. The **VBIE** bit in register **CMDA** must be set for the free run to work.

Control Register E									
Index	Mnemonic	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
14h	CMDE	YDEL2	YDEL1	YDEL0	0	SCHCMP3	SCHCMP2	SCHCMP1	SCHCMP0

YDEL[2:0] Y-C delay control. Group delay between Y and C can be adjusted as follows (in unit of CK2):

0 No delay.*

1 -2.0

2 -1.5

3 -1.0

4 -0.5

5 0.5

6 1.5

7 2.0

SCHCMP[3:0] Phase constant compare value for color burst phase relative to sync tip. Each step is 22.5 degrees with the value of 0 equal to 0 degree.

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Units
Supply voltage (measured to VSS)	V_{DD}	-0.5 to + 7.0	V
Voltage on any digital pin	V_{PIN}	-0.5 to (V_{DD}+0.5)	V
Ambient operating temperature (case)	T_A	-10 to + 100	°C
Storage temperature	T_S	-65 to + 150	°C
Junction temperature	T_J	150	°C
Vapor phase soldering (1 min.)	Tvsol	220	°C

Notes: 1.Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions.
2.Functional operation under any of these conditions is not implied.
3.Applied voltage must be current limited to a specified range.

OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Units
Supply voltage (measured to VSS)	V_{DD}	4.75	5.0	5.25	V
Ambient operating temperature, still air	T_A	0		70	°C

ELECTRICAL CHRACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Units
Supply					
Analog supply current	I_{DDA}		105	125	mA
Digital supply current	I_{DDD}		140	175	mA
Analog Characteristics					
Integral linearity error (AGC/ADC only)	$E_{I\text{-}ADC}$			1.5	lsb
Differential linearity error (AGC/ADC only)	$E_{D\text{-}ADC}$			0.75	lsb
Total harmonic distortion (4 MHz full scale)	THD		42		dB
Signal to noise ratio (4 MHz full scale)	SNR		42		d
Analog bandwidth (50 IRE to 3 dB point)	BW	4			MH
Input voltage range (peak-peak) 100 IRE input	$V_{I(PP)}$	0.5		1.5	V_{pp}
Input resistance AY0-AY2,AC0-AC2	R_{IN}	200			kΩ
Input capacitance for analog video inputs	C_{IN}		10		pF
Charge current for offset control	I_{OFF}		±4		μA
Cross talk between analog inputs	α			-50	dB
Video Performance					
Luminance frequency response (maximum variation to 4.2 MHz - multi burst)	F_{LUMA}		2		dB
Differential gain - complete chip (Modulated 40 IRE ramp)	D_G		1.5		%
Differential phase - complete chip (Modulated 40 IRE ramp)	D_P		1.0		degree
Chrominance frequency response (3 dB point) - CBWR=0/1	F_{CHROMA}		800/500		kHz
Chroma nonlinear gain distortion (NTC-7 Combination)	C_{NGD}		1		%
Chroma nonlinear phase distortion (NTC-7 Combination)	C_{NPD}		1.25		degree
Chroma to luma intermodulation (NTC-7 Combination)	C_{LI}		1		IRE
Chroma luma gain equality (NTC-7 Composite)	DEL_{CL}		±20		ns
Chroma luma delay equality (NTC-7 Composite)	AMP_{CL}		98-101		%
Noise level for unified weighting 10 kHz-5 MHz (100 IRE unmodulated ramp)	N_{LUMA}		58		dB
Chroma AM noise (red field)	N_{CAM}		60		dB
Chroma PM noise (red field)	N_{CPM}		54		dB
Digital I/O Characteristics					
Input low voltage	V_{IL}	VSS-0.5		0.8	V
Input high voltage	V_{IH}	2.0		VDD+0.5	V

Characteristics	Symbol	Min	Typ	Max	Units
Input low current (V_{IN} = 0.4 V)	I_{IL}			-1	µA
Input high current(VIN=2.4)	I_{IH}			-1	µA
Digital output low voltage (I_{OL}=3.2mA)	V_{OL}			0.4	V
Digital output high voltage (IOH=400µA)	V_{OH}	2.4			V
Digital three-state current	I_{OZ}			50	µA
Digital output capacitance	C_{OUT}			7	pF
Maximum capacitance load for digital data pins	$C_{L\text{-}DATA}$			30	pF
Maximum capacitance load for CK and CK2 outputs	$C_{L\text{-}CK}$			60	pF
Timing Characteristics - Digital Inputs					
XTALI input pulse width low	t_{pwlX}	15	20		ns
XTALI input pulse width high	t_{pwhX}	15	20		ns
Clock and Data Timing					
Total propagation delay from analog input to digital output	t_{dCHIP}		42ns + 28CK2		
Pulse width high for CK (KS0112 operates at frequencies from 24.5 MHz to 29 MHz)	t_{pwhCK}	15	18.5	22	ns
Pulse width high for CK2	t_{pwhCK2}	30	37	44	ns
Delay from rising edge of CK to CK2	t_{CK2}	3		7	ns
Delay from rising edge CK2 to data change (including pins Y0-Y7, C0-C7, AV, HS, VS, ODD, PID, SCH)	$t_{dD\text{-}CK2}$			25	ns
Delay from rising edge CK to data change (including pins Y0-Y7, C0-C7, AV, HS, VS, ODD, PID, SCH)	$t_{dD\text{-}CK}$			25	ns
Minimum hold time from rising edge of CK2 for data output)	t_{hD}	7			ns
Delay from falling edge of OEN to data bits in 3-state	t_{zD}			30	ns
Delay from rising edge OEN to data bits enabled	t_{enD}			35	ns
Timing Characteristics - 3-Wire Host Interface					
SCLK minimum pulse width low	$t_{pwlSCLK}$	50			ns
SCLK minimum pulse width high	$t_{pwhSCLK}$	115			ns
Read mode - delay from rising edge of SLCK to when data is in 3-state	$t_{3\text{-}stateD}$			40	ns
Write mode - SDAT setup time to rising edge of SCLK	t_{sD}	20			ns
Write mode -SDAT hold time from rising edge of SCLK	t_{hD}	20			ns
Read mode - delay from falling edge of SDAT to when data is valid	t_{validD}			40	ns

Characteristics	Symbol	Min	Typ	Max	Units
Read mode - delay from falling edge of SFRS to when data is in 3-state	$t_{3\text{-}stateD}$			50	ns
SFRS setup time to rising edge of SCLK	t_{sFRS}	20			ns
SFRS hold time from falling edge of SCLK	t_{hFRS}	20			ns
Timing Characteristics - 2-Wire Host Interface					
SCLK clock frequency	f_{SCLK}	0		400	kHz
Capacitive load for each bus line	C_b			400	pF
Rise and fall times for SCLK and SDAT	t_{RF}	20		300	ns
SCLK minimum pulse width low	$t_{pwlSCLK}$	1.3			µs
SCLK minimum pulse width high	$t_{pwhSCLK}$	0.6			µs
SDAT setup time to rising edge of SCLK	t_{sD}	100			ns
SDAT hold time from rising edge of SCLK	t_{hD}	0			ns

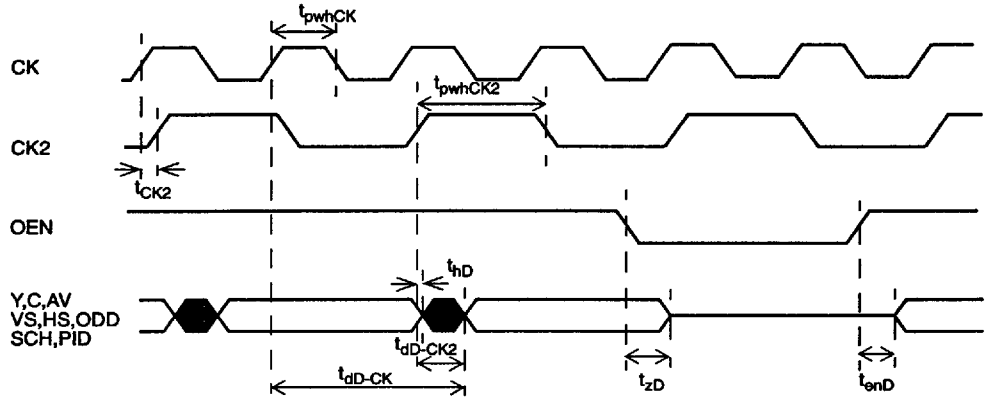


Figure 29. Data Output

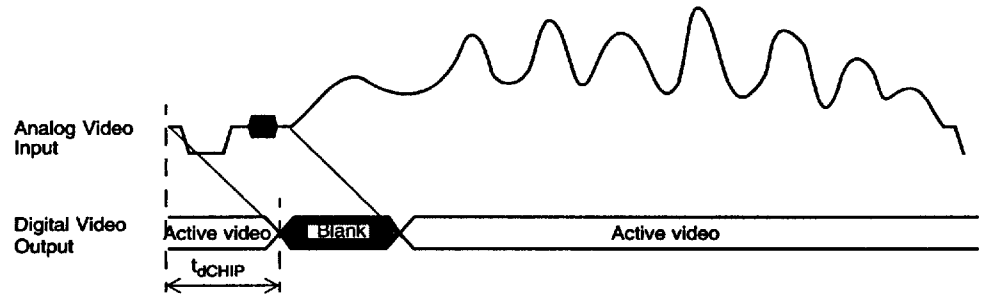


Figure 30. Analog Video Input to Digital Video Output Delay

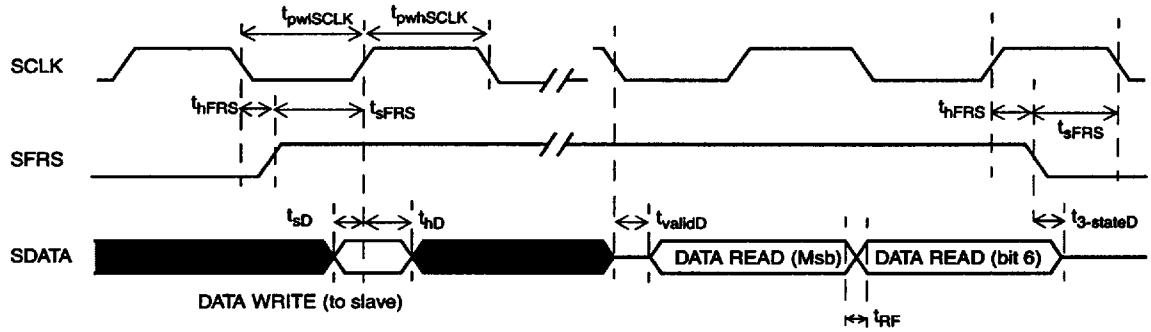


Figure 31. Host Interface Detailed Timing

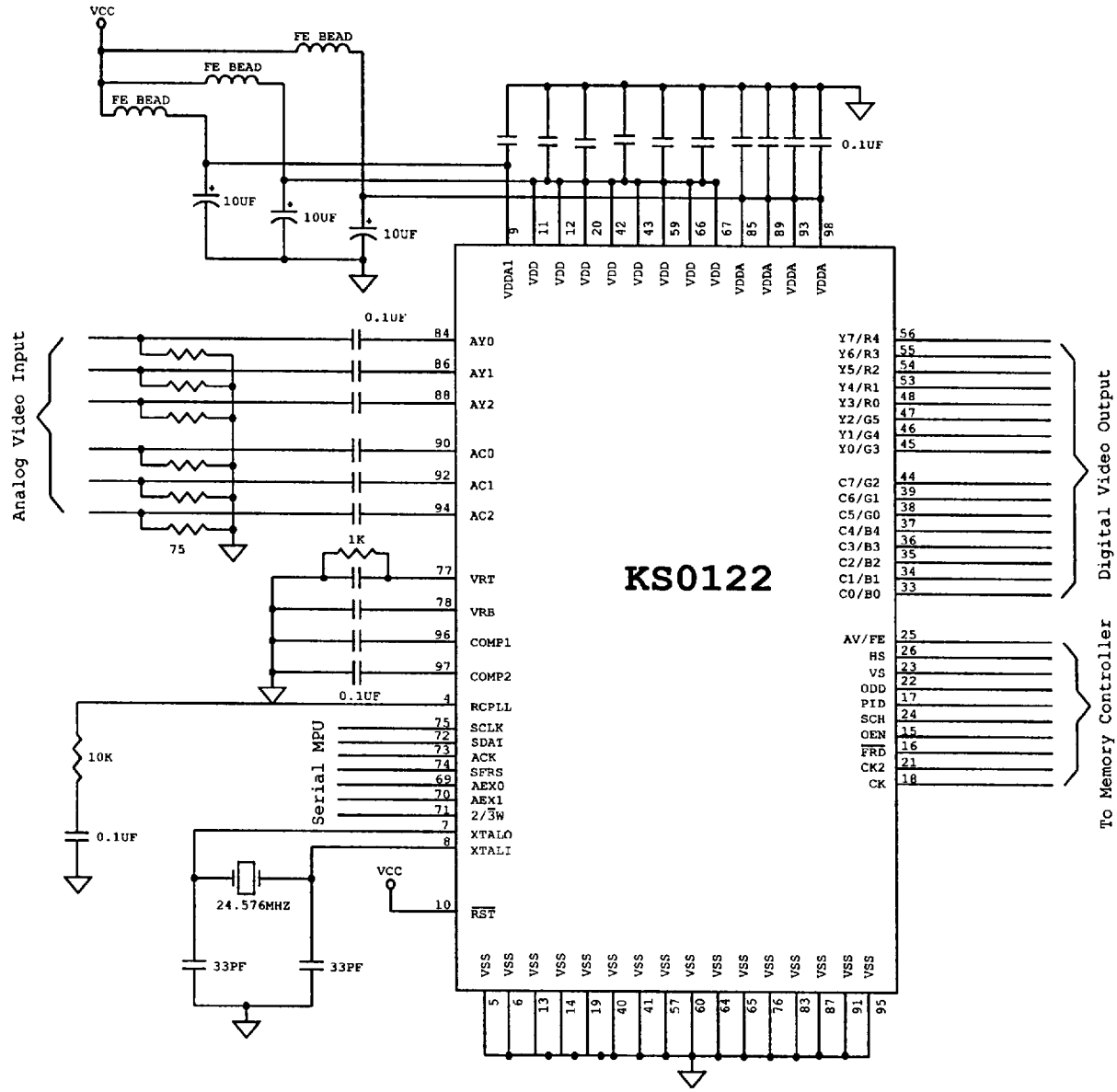
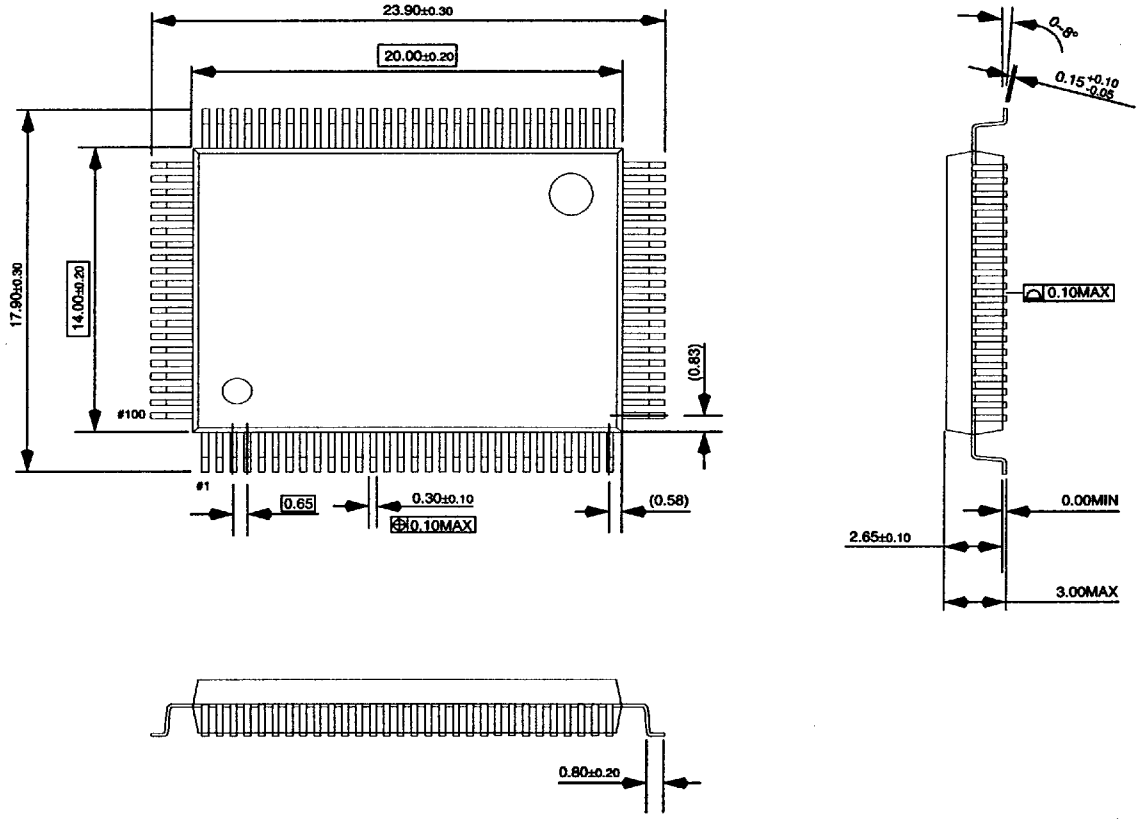


Figure 32. KS0122 Application Example

Package Dimension

100-QFP-1420C



Dimensions are in Millimeters