

KK74HC132A

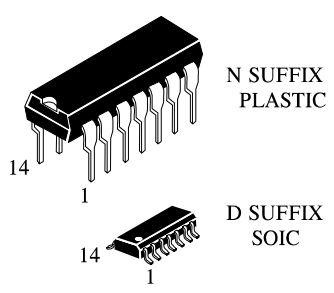
**Quad 2-Input NAND Gate
with Schmitt-Trigger Inputs**

High-Performance Silicon-Gate CMOS

The KK74HC132A is identical in pinout to the LS/ALS132. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

The KK74HC132A can be used to enhance noise immunity or to square up slowly changing waveforms.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices

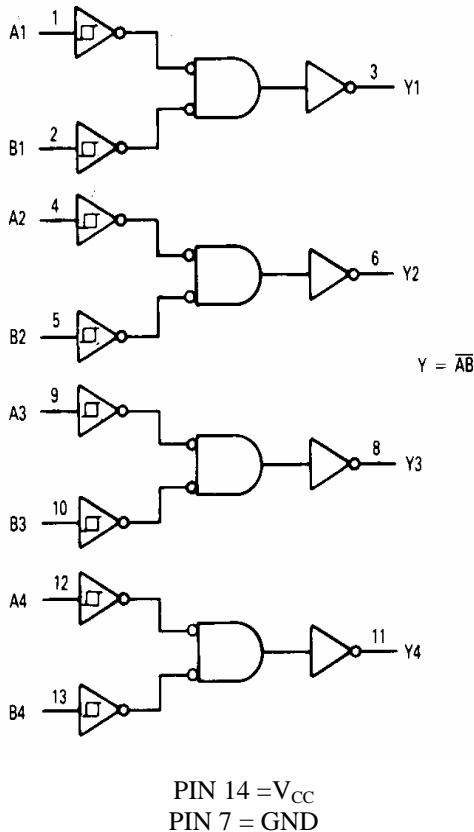


N SUFFIX
PLASTIC

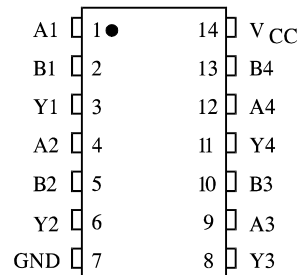
D SUFFIX
SOIC

ORDERING INFORMATION
 KK74HC132AN Plastic
 KK74HC132AD SOIC
 $T_A = -55^\circ$ to 125° C for all packages

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	-	no limit*	ns

*When $V_{IN} \approx 0.5V_{CC}$, $I_{CC} \gg$ quiescent current.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V _{T+} max	Maximum Positive-Going Input Threshold Voltage	V _{OUT} =0.1 V I _{OUT} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{T+} min	Minimum Positive-Going Input Threshold Voltage	V _{OUT} =0.1 V I _{OUT} ≤ 20 μA	2.0	1.0	0.95	0.95	V
			4.5	2.3	2.25	2.25	
			6.0	3.0	2.95	2.95	
V _{T-} max	Maximum Negative-Going Input Threshold Voltage	V _{OUT} =V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	0.9	0.95	0.95	V
			4.5	2.0	2.05	2.05	
			6.0	2.6	2.65	2.65	
V _{T-} min	Minimum Negative-Going Input Threshold Voltage	V _{OUT} =V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V _H max Note	Maximum Hysteresis Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	1.2	1.2	1.2	V
			4.5	2.25	2.25	2.25	
			6.0	3.0	3.0	3.0	
V _H min Note	Minimum Hysteresis Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	0.2	0.2	0.2	V
			4.5	0.4	0.4	0.4	
			6.0	0.5	0.5	0.5	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} ≤ V _{T-} min or V _{T+} max I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
			V _{IN} ≤ V _{T-} min or V _{T+} max I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	3.98	3.84	
6.0	5.48	5.34	5.2				
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} ≥ V _{T+} max I _{OUT} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
			V _{IN} ≥ V _{T+} max I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	0.26	0.33	
6.0	0.26	0.33	0.4				
I _{IN}	Maximum Input Leakage Current	V _{IN} =V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} =V _{CC} or GND I _{OUT} =0μA	6.0	1.0	10	40	μA

Note. V_Hmin>(V_{T-}min)-(V_{T+}max); V_Hmax=(V_{T+}max)+(V_{T-}min).

AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{IN}	Maximum Input Capacitance	-	10	10	10	pF

C _{PD}	Power Dissipation Capacitance (Per Gate)	Typical @25°C, V _{CC} =5.0 V			pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	24			

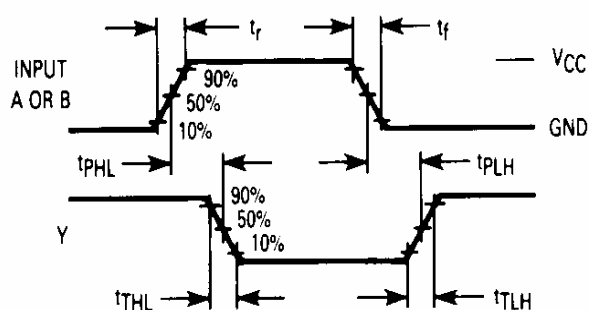
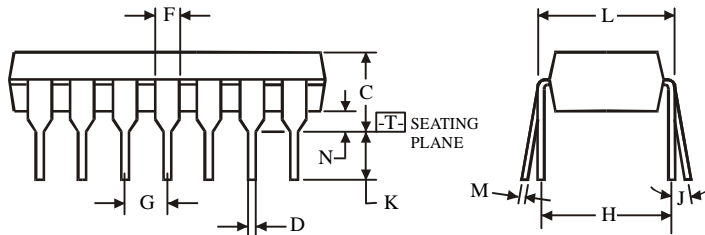
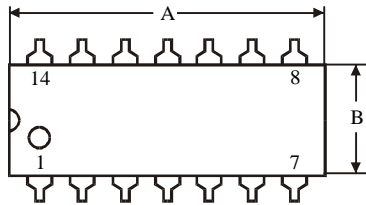
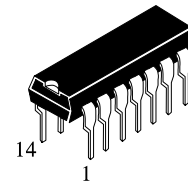


Figure 1. Switching Waveforms

**N SUFFIX PLASTIC DIP
(MS - 001AA)**



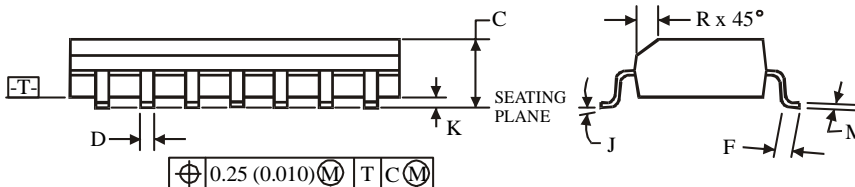
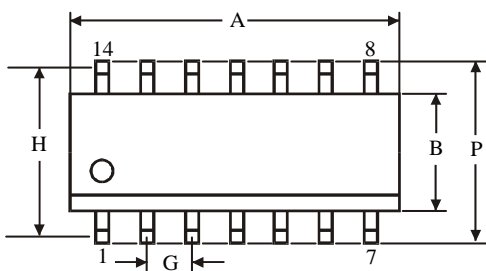
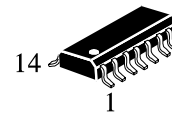
$\oplus 0.25 (0.010) \text{ (M) T}$

NOTES:

- Dimensions "A", "B" do not include mold flash or protrusions.
Maximum mold flash or protrusions 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	18.67	19.69
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

**D SUFFIX SOIC
(MS - 012AB)**



$\oplus 0.25 (0.010) \text{ (M) T C (M)}$

NOTES:

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side
for A; for B - 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	8.55	8.75
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.27	
J	0°	8°
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5