

KK74HC125A

Quad 3-State Noninverting Buffers

The KK74HC125A is identical in pinout to the LS/ALS125. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

The KK74HC125A noninverting buffers are designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The devices have four separate output enables that are active-low.

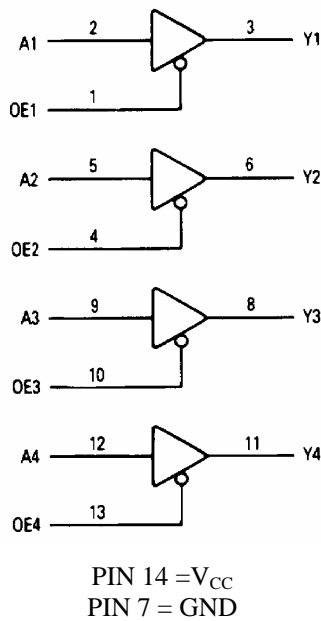
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices

N SUFFIX
PLASTIC

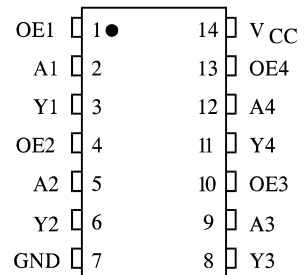
D SUFFIX
SOIC

ORDERING INFORMATION
 KK74HC125AN Plastic
 KK74HC125AD SOIC
 $T_A = -55^\circ$ to 125° C for all packages

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

| Inputs | | Output |
|--------|----|--------|
| A | OE | Y |
| H | L | H |
| L | L | L |
| X | H | Z |

X = don't care
 Z = high impedance

MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|------------------|--|------------------------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| V _{IN} | DC Input Voltage (Referenced to GND) | -1.5 to V _{CC} +1.5 | V |
| V _{OUT} | DC Output Voltage (Referenced to GND) | -0.5 to V _{CC} +0.5 | V |
| I _{IN} | DC Input Current, per Pin | ±20 | mA |
| I _{OUT} | DC Output Current, per Pin | ±35 | mA |
| I _{CC} | DC Supply Current, V _{CC} and GND Pins | ±75 | mA |
| P _D | Power Dissipation in Still Air, Plastic DIP+ SOIC Package+ | 750 500 | mW |
| T _{stg} | Storage Temperature | -65 to +150 | °C |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) | 260 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------------------------------|--|-----|-----------------|------|
| V _{CC} | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| V _{IN} , V _{OUT} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V _{CC} | V |
| T _A | Operating Temperature, All Package Types | -55 | +125 | °C |
| t _r , t _f | Input Rise and Fall Time (Figure 1) | | | |
| | V _{CC} =2.0 V | 0 | 1000 | ns |
| | V _{CC} =4.5 V | 0 | 500 | |
| | V _{CC} =6.0 V | 0 | 400 | |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|--|--|----------------------|----------------------|-----------|------------|------|
| | | | | 25 °C to -55°C | ≤85 °C | ≤125 °C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{OUT} = V _{CC} -0.1 V I _{OUT} ≤ 20 μA | 2.0 | 1.5 | 1.5 | 1.5 | V |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.2 | 4.2 | 4.2 | |
| V _{IL} | Maximum Low - Level Input Voltage | V _{OUT} =0.1 V I _{OUT} ≤ 20 μA | 2.0 | 0.5 | 0.5 | 0.5 | V |
| | | | 4.5 | 1.35 | 1.35 | 1.35 | |
| | | | 6.0 | 1.8 | 1.8 | 1.8 | |
| V _{OH} | Minimum High-Level Output Voltage | V _{IN} =V _{IH} I _{OUT} ≤ 20 μA | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | 6.0 | 5.9 | 5.9 | 5.9 | | |
| | | V _{IN} =V _{IH} I _{OUT} ≤ 6.0 mA I _{OUT} ≤ 7.8 mA | 4.5 | 3.98 | 3.84 | 3.7 | |
| 6.0 | 5.48 | 5.34 | 5.2 | | | | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{IN} =V _{IL} I _{OUT} ≤ 20 μA | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | 6.0 | 0.1 | 0.1 | 0.1 | | |
| | | V _{IN} =V _{IL} I _{OUT} ≤ 6.0 mA I _{OUT} ≤ 7.8 mA | 4.5 | 0.26 | 0.33 | 0.4 | |
| 6.0 | 0.26 | 0.33 | 0.4 | | | | |
| I _{IN} | Maximum Input Leakage Current | V _{IN} =V _{CC} or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| I _{OZ} | Maximum Three-State Leakage Current | Output in High-Impedance State V _{IN} =V _{IL} or V _{IH} V _{IN} =V _{CC} or GND | 6.0 | ±0.5 | ±5.0 | ±10 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{IN} =V _{CC} or GND I _{OUT} =0μA | 6.0 | 4.0 | 40 | 160 | μA |

AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit |
|-------------------------------------|--|---------------------------------------|----------------------|-------|--------|------|
| | | | 25 °C to -55°C | ≤85°C | ≤125°C | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3) | 2.0 | 90 | 115 | 135 | ns |
| | | 4.5 | 18 | 23 | 27 | |
| | | 6.0 | 15 | 20 | 23 | |
| t _{PLZ} , t _{PHZ} | Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4) | 2.0 | 120 | 150 | 180 | ns |
| | | 4.5 | 24 | 30 | 36 | |
| | | 6.0 | 20 | 26 | 31 | |
| t _{PZL} , t _{PZH} | Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4) | 2.0 | 90 | 115 | 135 | ns |
| | | 4.5 | 18 | 23 | 27 | |
| | | 6.0 | 15 | 20 | 23 | |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, Any Output (Figures 1 and 3) | 2.0 | 60 | 75 | 90 | ns |
| | | 4.5 | 12 | 15 | 18 | |
| | | 6.0 | 10 | 13 | 15 | |
| C _{IN} | Maximum Input Capacitance | - | 10 | 10 | 10 | pF |
| C _{OUT} | Maximum Three-State Output Capacitance (Output in High-Impedance State) | - | 15 | 15 | 15 | pF |
| C _{PD} | Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$ | Typical @25°C, V _{CC} =5.0 V | | | pF | |
| | | 45 | | | | |

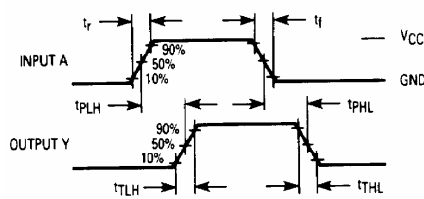


Figure 1. Switching Waveforms

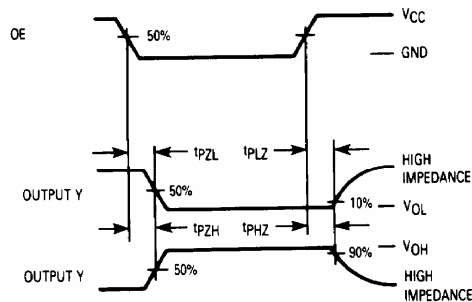
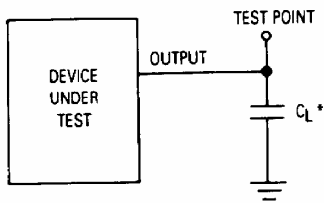
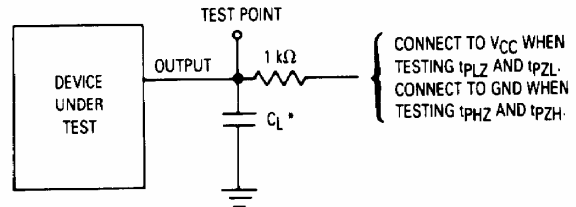


Figure 2. Switching Waveforms



*Includes all probe and jig capacitance.

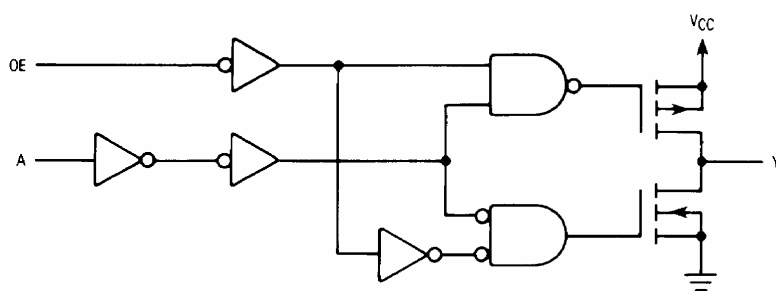
Figure 3. Test Circuit



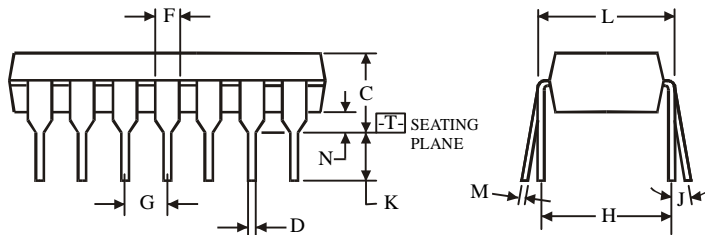
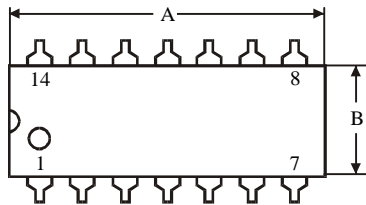
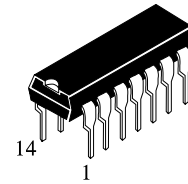
*Includes all probe and jig capacitance.

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM
(1/4 of the Device)



**N SUFFIX PLASTIC DIP
(MS - 001AA)**



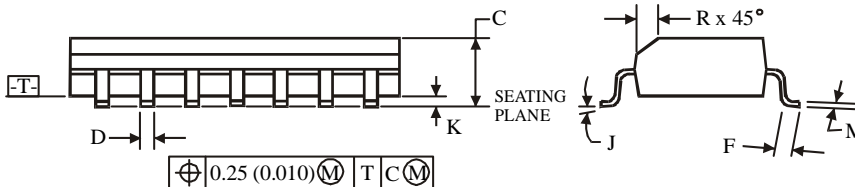
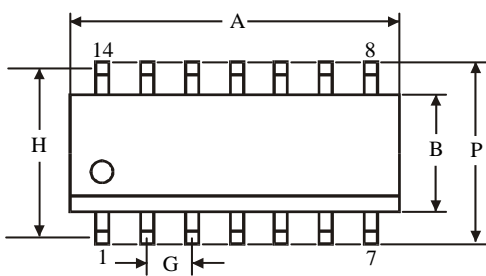
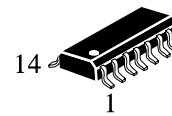
$\oplus 0.25 (0.010) \text{ (M) T}$

NOTES:

- Dimensions "A", "B" do not include mold flash or protrusions.
Maximum mold flash or protrusions 0.25 mm (0.010) per side.

| Symbol | Dimension, mm | |
|--------|---------------|-------|
| | MIN | MAX |
| A | 18.67 | 19.69 |
| B | 6.1 | 7.11 |
| C | | 5.33 |
| D | 0.36 | 0.56 |
| F | 1.14 | 1.78 |
| G | 2.54 | |
| H | 7.62 | |
| J | 0° | 10° |
| K | 2.92 | 3.81 |
| L | 7.62 | 8.26 |
| M | 0.2 | 0.36 |
| N | 0.38 | |

**D SUFFIX SOIC
(MS - 012AB)**



$\oplus 0.25 (0.010) \text{ (M) T C (M)}$

NOTES:

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.

| Symbol | Dimension, mm | |
|--------|---------------|------|
| | MIN | MAX |
| A | 8.55 | 8.75 |
| B | 3.8 | 4 |
| C | 1.35 | 1.75 |
| D | 0.33 | 0.51 |
| F | 0.4 | 1.27 |
| G | 1.27 | |
| H | 5.27 | |
| J | 0° | 8° |
| K | 0.1 | 0.25 |
| M | 0.19 | 0.25 |
| P | 5.8 | 6.2 |
| R | 0.25 | 0.5 |