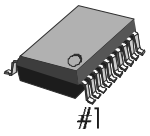
FREQUENCY SYNTHESIZER KB8821/22/23

INTRODUCTION

The KB8821/22/23 are high performance dual frequency synthesizers with integrated prescalers designed for RF operation up to 1.2GHz/2.0GHz/2.5GHz and IF operation up to 520MHz.
The KB8821/22/23 contain dual-modulus prescalers. The RF synthesizer adopts a 64/65 or an 128/129 prescaler(32/33 or 64/65 for the KB8823) and the IF synthesizer adopts an 8/9 or a 16/17 prescaler.
Using a proprietary digital phase-locked-loop technique, the KB8821/22/23 have linear phase detector characteristic and can be used for very stable, low noise local oscillator signal. Supply voltage can range from 2.7V to 4.0V. The KB8821/22/23 are now available in a 20-TSSOP/24-QFN package.

20-TSSOP-225



FEATURES

- Very low current consumption(8821:3.5mA, 22:4.5mA, 23:5.5mA)
- Operating voltage range : 2.7 ~ 4.0V
- Selectable power saving mode(Icc=1uA typical @3V)
- Dual modulus prescaler :
  KB8821/22 (RF) 64/65 or 128/129
  KB8823 (RF) 32/33 or 64/65
  KB8821/22/23 (IF) 8/9 or 16/17
- Programmability via serial bus interface
- No dead-zone PFD
- Variable charge pump output current
- High speed lock mode

ORDERING INFORMATION

Device	Package	Tem. Range
KB8821/22/23	20-TSSOP-225	-40 ~ +85°C
KB8821/22/23	24-QFN*	-40 ~ +85°C

* QFN : Quad Flat Non-leaded(see Addendum).

APPLICATIONS

- Cellular telephone systems : KB8821
- Portable wireless communications : KB8822 (PCS/PCN, cordless)
- Wireless Local Area Networks (W-LANs) : KB8823
- Other wireless communication systems

BLOCK DIAGRAM

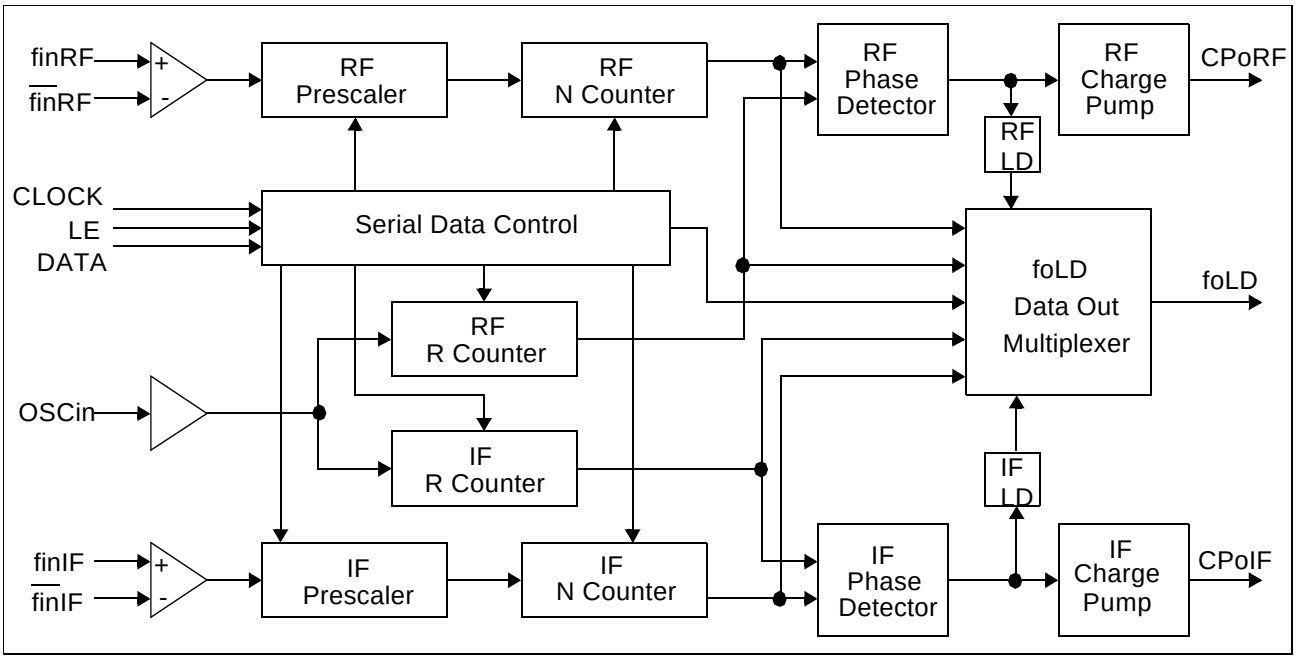


Figure 1. BLOCK DIAGRAM

SAMSUNG ELECTRONICS

BLOCK DIAGRAM- Continued

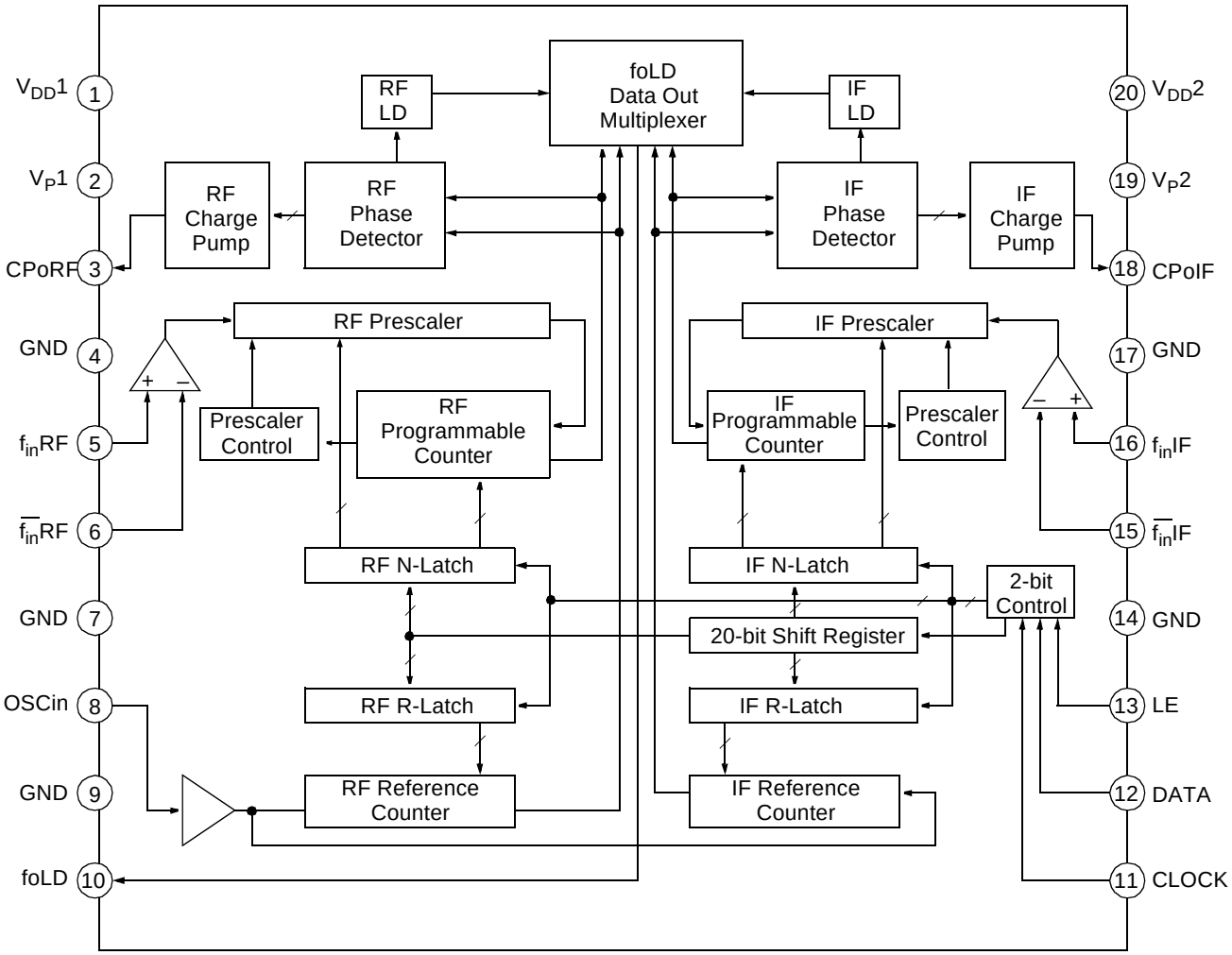
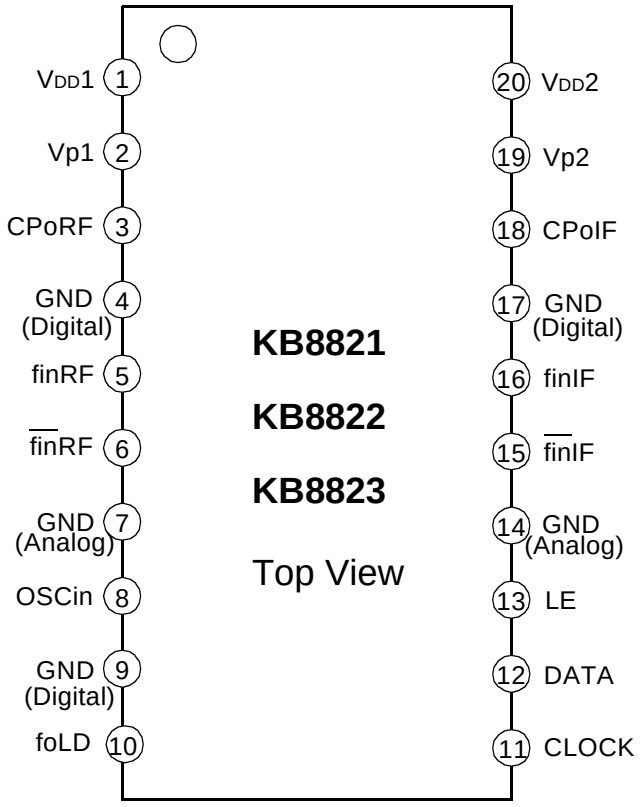


Figure 2. Detailed block diagram

PIN CONFIGURATION



20-TSSOP

20-Lead(0.173 Wide) Thin Shrink Small Outline Package(20-TSSOP)

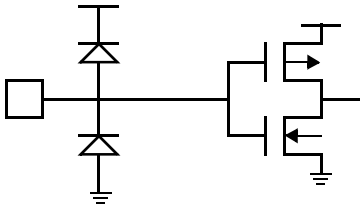
1. pin #9 = pin #17(internally connected).
2. Do not tie up Vp and V_{DD}
   : Vp is the source of digital noises. The power for analog part is supplied by V_{DD}. If Vp and V_{DD} are tied together, noisy Vp corrupts the power source for the analog part.

PIN DESCRIPTION

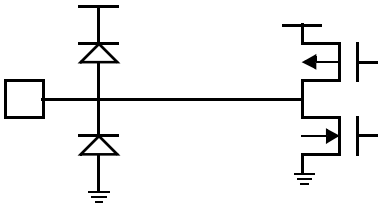
Pin No	Symbol	I / O	Description
1	$V_{DD}1$	-	Power supply voltage input for the RF PLL part. $V_{DD}1$ must equal $V_{DD}2$. In order to reject supply noise, bypass capacitors must be placed as close as possible to this pin and be connected directly to the ground plane.
2	Vp1	-	Power supply voltage input for RF charge pump($\geq V_{DD}1$).
3	CPoRF	O	Internal RF charge pump output for connection to an external loop filter whose filtered output drives an external VCO.
4	GND	-	Ground for RF digital blocks.
5	finRF	I	RF prescaler input. The signal comes from the external VCO.
6	$\overline{\text{fin}}$RF	I	The complementary input of the RF prescaler. A bypass capacitor must be placed as close as possible to this pin and be connected directly to the ground plane. The bypass capacitor is optional with some loss of sensitivity.
7	GND	-	Ground for RF analog blocks.
8	OSCin	I	Reference counter input. TCXO is connected via a coupling capacitor.
9	GND	-	Ground for IF digital blocks.
10	f_{oLD}	O	Multiplexed output of the RF/IF programmable counters, the reference counters, the lock detect signals and the shift registers. The output level is CMOS level. (see f_{out} Programmable Truth Table)
11	CLOCK	I	CMOS clock input. Serial data for the various counters is transfered into the 22-bit shift register on the rising edge of the clock signal.
12	DATA	I	Binary serial data input. The MSB of CMOS input data is entered first. The control bits are on the last two bits. CMOS input.
13	LE	I	Load enable CMOS input. When LE becomes high, the data in the shift register is loaded into one of the four latches(by the control bits).
14	GND	-	Ground for IF analog blocks.
15	$\overline{\text{fin}}$IF	I	The complementary input of the IF prescaler. A bypass capacitor must be placed as close as possible to this pin and be connected directly to the ground plane. The bypass capacitor is optional with some loss of sensitivity.
16	finIF	I	IF prescaler input. The signal comes from the external VCO.
17	GND	-	Ground for IF digital blocks.
18	CPoIF	O	Internal IF charge pump output for connection to an external loop filter whose filtered output drives an external VCO.
19	Vp2	-	Power supply voltage input for IF charge pump($\geq V_{DD}2$)
20	$V_{DD}2$	-	Power supply voltage input for the IF PLL part. $V_{DD}1$ must equal $V_{DD}2$. In order to reject supply noise, bypass capacitors must be placed as close as possible to this pin and be connected directly to the ground plane.

EQUIVALENT CIRCUIT DIAGRAM

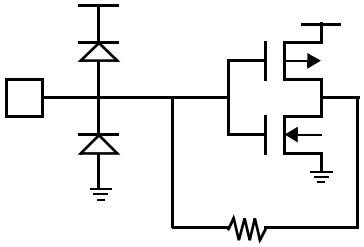
♦ CLOCK, DATA, LE



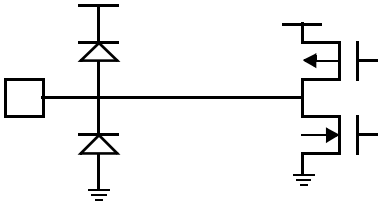
♦ foLD



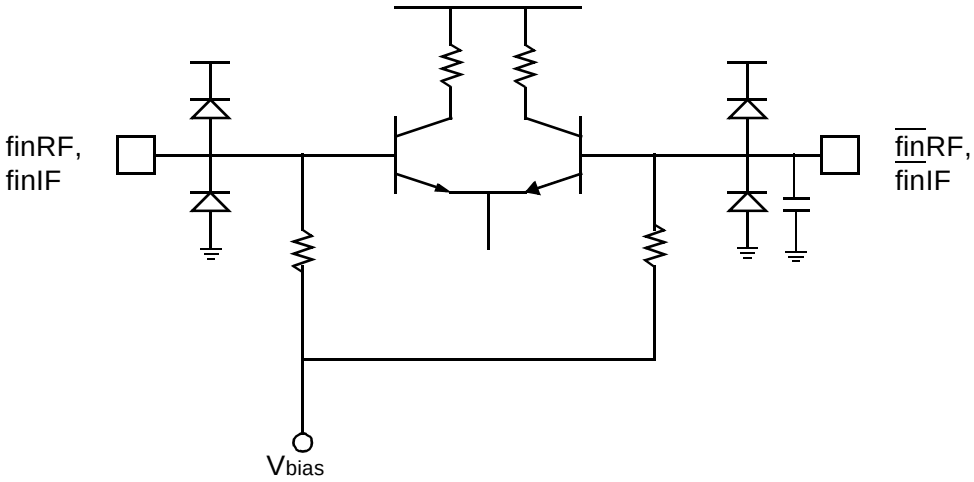
♦ OSCin



♦ CPoRF, CPoIF



♦ finRF, $\overline{\text{fin}}$RF, finIF, $\overline{\text{fin}}$IF



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	5.5	V
Power Dissipation	P_D	600	mW
Operating Temperature	T_a	-40°C ~ +85°C	°C
Storage Temperature	T_{STG}	-65°C ~ +150°C	°C

ELECTROSTATIC CHARACTERISTICS

Characteristic	Pin No.	ESD level	Unit
Human Body Model	All	< ±2000	V
Machine Model	All	< ±300	V
Charged Device Model	All	< ±800	V

** These devices are ESD sensitive. These devices must be handled in the ESD protected environment.

ELECTRICAL CHARACTERISTICS(V_{DD}=3.0V, V_P=3.0V, -40°C£T_a£85°C Unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage		V_{DD}		2.7	3.0	4.0	V
		V_P		V_{DD}	3.0	4.0	
Power Supply Current	KB8823 RF + IF	I_{DD}	V_{DD}=2.7V to 4.0V		5.5		mA
	KB8823 RF Only				4.0		
	KB8822 RF + IF				4.5		
	KB8822 RF Only				3.0		
	KB8821 RF + IF				3.5		
	KB8821 RF Only				2.0		
	KB882x IF Only				1.5		
Power down Current		I_{PWDN}	V_{DD}=3.0V		1.0	10	µA
Digital inputs : CLOCK, DATA and LE							
High-Level Input Voltage		V_{IH}	V_{DD}=2.7V to 4.0V	0.7V_{DD}			V
Low-Level Input Voltage		V_{IL}	V_{DD}=2.7V to 4.0V			0.3V_{DD}	V
High-Level Input Current		I_{IH}	V_{IH}= V_{DD}=4.0V	-1.0		+1.0	µA
Low-Level Input Current		I_{IL}	V_{IL}=0V, V_{DD}=4.0V	-1.0		+1.0	µA
Reference Divider Input : OSCin							
Input Current		I_{IHR}	V_{IH}= V_{DD}=4.0V			+100	µA
		I_{ILR}	V_{IL}=0V, V_{DD}=4.0V	-100			µA
Digital Output : foLD							
High Level Output Voltage		V_{OH}	Iout = -500µA	V_{DD}-0.4			V
Low Level Output Voltage		V_{OL}	Iout = +500µA			0.4	V

ELECTRICAL CHARACTERISTICS(V_{DD}=3.0V, V_P=3.0V, -40°C£T_a£85°C Unless otherwise specified)- Continued

Characteristic		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Charge Pump Outputs : CPoRF, CPoIF							
Charge Pump Output Current		I_{CP-SRC}	$V_{CP}=V_P/2$, I_{CPo}=Low		-1.125		mA
		$I_{CP-SINK}$	$V_{CP}=V_P/2$, I_{CPo}=Low		+1.125		
		I_{CP-SRC}	$V_{CP}=V_P/2$, I_{CPo}=High		-4.5		
		$I_{CP-SINK}$	$V_{CP}=V_P/2$, I_{CPo}=High		+4.5		
Charge Pump Leakage Current		I_{CPL}	$0.5V \le V_{CP} \le V_P-0.5V$	-2.5		+2.5	nA
Output Current Sink vs. Source Mismatch*		$I_{CP-SINK}$ vs I_{CP-SRC}	$V_{CP}=V_P/2$ T_a=25°C		3	10	%
Output Current Magnitude Variation vs. Temperature**		I_{CP} vs T	$V_{CP}=V_P/2$		10		%
Output Current Magnitude Variation vs. Voltage***		I_{CP} vs V_{CP}	$0.5V \le V_{CP} \le V_P-0.5V$ T_a=25°C		10	15	%
Programmable Divider							
Operating Frequency	KB8823	finRF	V_{DD}=2.7V to 4.0V	0.5		2.5	GHz
	KB8822			0.2		2.0	
	KB8821			0.1		1.2	
Operating Frequency		finIF	V_{DD}=3.0V	45		520	MHz
RF Input Sensitivity		P_{fin}RF	V_{DD}=3.0V	-15		0	dBm
			V_{DD}=4.0V	-10		0	
IF Input Sensitivity		P_{fin}IF	V_{DD}=2.7V to 4.0V	-10		0	dBm
Phase Detector Frequency		f_{PD}				10	MHz
Reference Divider							
Operating Frequency		OSCin		5		40	MHz
Input Sensitivity		V_{OSCin}		0.5			V_{PP}

ELECTRICAL CHARACTERISTICS(V_{DD}=3.0V, V_P=3.0V, -40°C≤T_a≤85°C Unless otherwise specified)- Continued

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Serial Data Control						
CLOCK Frequency	f_{CLOCK}				10	MHz
CLOCK Pulse Width High	t_{CWH}		50			ns
CLOCK Pulse Width Low	t_{CWL}		50			ns
DATA Set Up Time to CLOCK Risng Edge	t_{DS}		50			ns
DATA Hold Time after CLOCK Rising Edge	t_{DH}		10			ns
LE Pulse Width	t_{LEW}		50			ns
CLOCK Rising Edge to LE Rising Edge	t_{CLE}		50			ns

<For Charge Pump items>
I_a=Charge pump sink current at Vcp=Vp-ΔV, I_b=Charge pump sink current at Vcp=Vp/2, I_c=Charge pump sink current at Vcp=ΔV
I_d=Charge pump source current at Vcp=Vp-ΔV, I_e=Charge pump source current at Vcp=Vp/2, I_f=Charge pump source current at Vcp=ΔV
ΔV=Voltage offset from positive(for sink current) and negative(for source current) points from which the charge pump currents become flat.

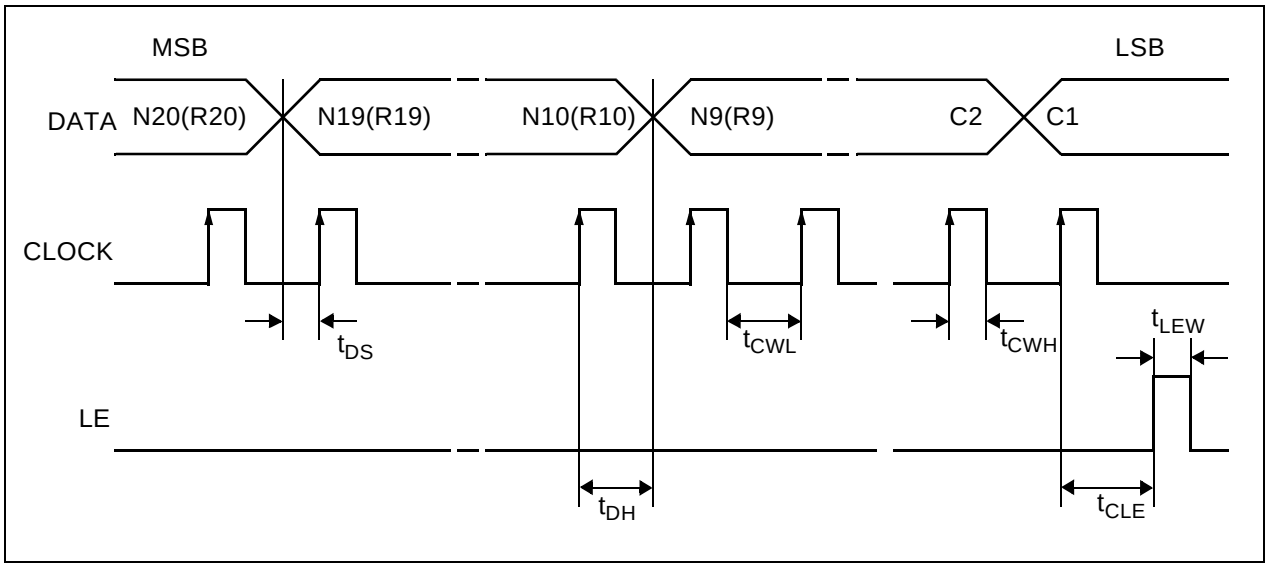
* Output Current Sink vs. Source Mismatch = [| I_b|-|I_e|] / [0.5 * {| I_b|+|I_e|}] * 100 (%)
** Output Current Magnitude Variation vs. Temperature =
[| I_b @any temp.| - |I_b @ 25°C|] / | I_b @ 25°C| * 100 (%) **and** [|I_e @any temp.| - |I_e @ 25°C|] / |I_e @ 25°C| * 100 (%)
*** Output Current Magnitude Variation vs. Voltage =
[0.5 * {|I_a|-|I_c|}] / [0.5 * {|I_a|+|I_c|}] * 100 (%) and [0.5 * {|I_d|-|I_f|}] / [0.5 * {|I_d|+|I_f|}] * 100 (%)

FUNCTIONAL DESCRIPTION

The Samsung KB882x are dual PLL frequency synthesizer ICs. KB882x combined with external LPFs and external VCOs form PLL frequency synthesizers. They include serial data control, R counter, N counter, prescaler, phase detector, charge pump, and etc.(Figure 1).

Serial data is moved into 20-bit shift register on the rising edge of the clock(Figure 2). These data enters MSB first. When LE becomes HIGH, data in the shift register is moved into one of the 4 latches(by the 2-bit control). The divide ratios of the prescaler and the counters are determined by the data stored in the latches. The external VCO output signal is divided by the prescaler and the N counter. External reference signal is divided by the R counter. These two signals are the two input signals to the phase detector. The phase detector drives the charge pump by comparing frequencies and phases of the above two signals.The charge pump and the external LPF make the control voltage for the external VCO and finally the VCO generates the appropriate frequency signal.

Serial Data Input Timing



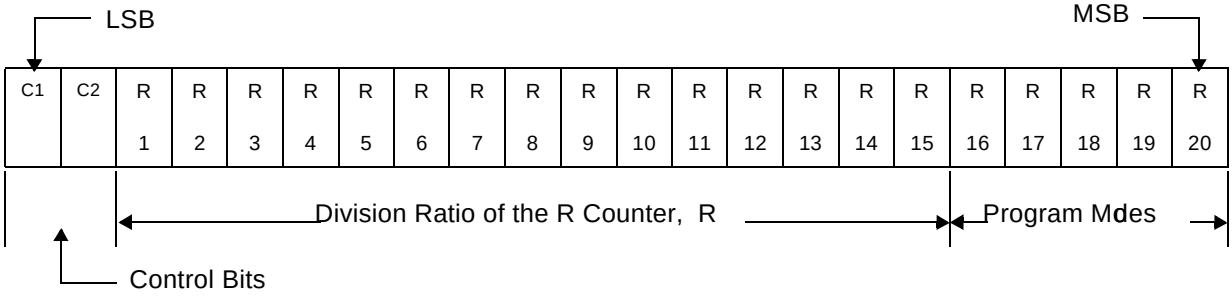
FUNCTIONAL DESCRIPTION- Continued

Control Bits

Control Bits		DATA Location
C1	C2	
0	0	IF R Counter
0	1	RF R Counter
1	0	IF N Counter
1	1	RF N Counter

Programmable Reference Counter(IF / RF R Counter)

If the Control Bits are 00(IF) or 01(RF), data is moved from the 20-bit shift register into the R-latch which sets the reference counter. Serial data format is shown in the table below.



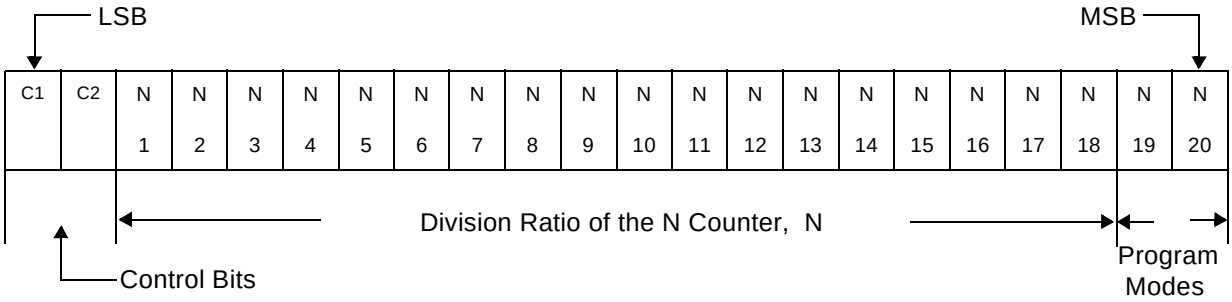
♦ 15-Bit Programmable Reference Counter Ratio

Division Ratio	R 15	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Division ratio : 3 to 32767
Data are shifted in MSB first

FUNCTIONAL DESCRIPTION- Continued

Programmable Counter(N Counter)
If the Control Bits are 10(IF) or 11(RF), data is transferred from the 20-bit shift register into the N-latch. N Counter consists of 7-bit swallow counter(A counter) and 11-bit main counter(B counter). Serial data format is shown below.



♦ 7-Bit Swallow Counter Division Ratio(A Counter)

RF

Division Ratio(A)	N 7	N 6	N 5	N 4	N 3	N 2	N 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Division ratio : 0 to 127
B≥ A

IF

Division Ratio(A)	N 7	N 6	N 5	N 4	N 3	N 2	N 1
0	X	X	X	0	0	0	0
1	X	X	X	0	0	0	1
•	•	•	•	•	•	•	•
15	X	X	X	1	1	1	1

Division ratio : 0 to 15
B≥ A

X = DONT CARE condition

♦ 11-Bit Main Counter Division Ratio(B Counter)

Division Ratio	N 18	N 17	N 16	N 15	N 14	N 13	N 12	N 11	N 10	N 9	N 8
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Division ratio : 3 to 2047

FUNCTIONAL DESCRIPTION- Continued

Pulse Swallow Function

$f_{VCO}=[(P X B) + A] x f_{OSCin} / R$

f_{VCO} : External VCO output frequency

P : Preset modulus of dual modulus prescaler

(for KB8821/22 RF:P=64 or 128, for KB8823 RF:P=32 or 64, for IF: P=8 or 16)

B : 11-bit main counter division ratio ($3 \leq B \leq 2047$)

A : 7-bit swallow counter division ratio

(for RF: $0 \leq A \leq 127$, for IF: $0 \leq A \leq 15$, $A \leq B$)

f_{OSCin} : External reference frequency(from external oscillator)

R : 15-bit reference counter division ratio ($3 \leq R \leq 32767$)

Program Mode

C1	C2	R16	R17	R18	R19	R20
0	0	IF Phase Detector Polarity	IF I_{CPo}	IF CPoIF High Impedance	IF LD	IF Fo
0	1	RF Phase Detector Polarity	RF I_{CPo}	RF CPoIF High Impedance	RF LD	RF Fo

C1	C2	N19	N20
1	0	IF Prescaler	Pwdn IF
1	1	RF Prescaler	Pwdn RF

♦ Mode Select Truth Table

	Phase Detector Polarity	CPoIF High Impedance	I_{CPo}	IF Prescaler	RF Prescaler KB8821/22 (KB8823)	Pwdn
0	Negative	Normal Operation	Low	8/9	64/65 (32/33)	Pwr Up
1	Positive	High Impedance	High	16/17	128/129 (64/65)	Pwr Dn

* The charge pump output current of I_{CPo} LOW = $1/4 \times I_{CPo}$ HIGH.

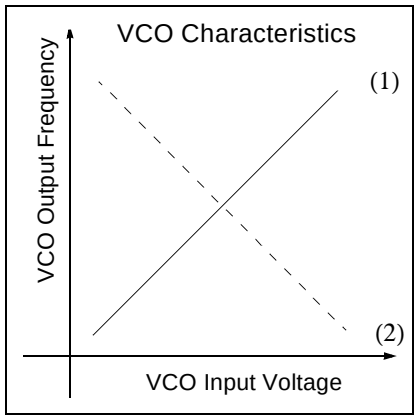
FUNCTIONAL DESCRIPTION - Continued

♦ Phase Detector Polarity

Depending on VCO characteristics, R16 bit should be set as follows :

VCO characteristics are positive like (1) : R16 HIGH

VCO characteristics are negative like (2) : R16 LOW



♦ foLD (Pin10) Output Truth Table

RF R19 (RF LD)	IF R19 (IF LD)	RF R20 (RF fo)	IF R20 (IF fo)	foLD Output State
0	0	0	0	Disabled (default LOW)
0	1	0	0	IF Lock Detect
1	0	0	0	RF Lock Detect
1	1	0	0	RF and IF Lock Detect
0	0	0	1	IF Reference Divider Output
0	0	1	0	RF Reference Divider Output
0	1	0	1	IF Programmable Divider Output
0	1	1	0	RF Programmable Divider Output
0	0	1	1	High Speed Lock mode
0	1	1	1	IF Counter Reset
1	0	1	1	RF Counter Reset
1	1	1	1	RF and IF Counter Reset

- When the PLL is locked and a lock detect mode is selected, the foLD output is HIGH, with narrow pulses LOW.
- Counter Reset mode resets R & N counters.
- The high speed lock mode sets the foLD output pin to be connected to ground with a low impedance ($\leq 110\Omega$).

FUNCTIONAL DESCRIPTION- Continued

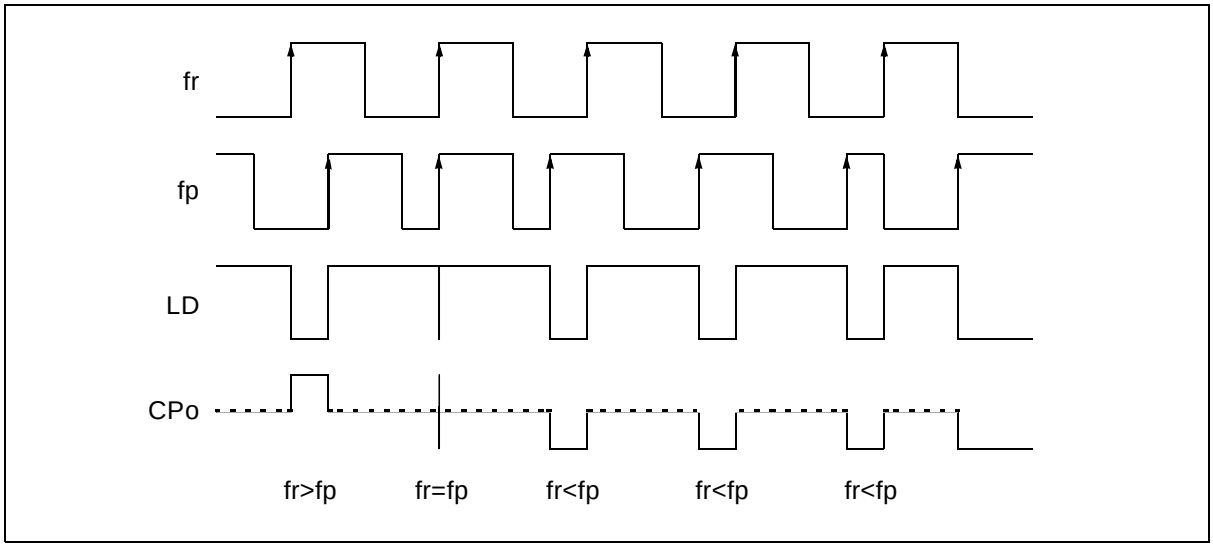
♦ Powerdown mode operation

There are synchronous and asynchronous powerdown modes for KB8821/22/23.
Synchronous powerdown mode occurs if R18 bit is LOW, N20 bit is HIGH and charge pump output is in high impedance state. In the synchronous power down mode, the powerdown function is activated by the charge pump to diminish unwanted frequency jumps. Asynchronous powerdown mode occurs if R18 bit is HIGH and N20 bit is HIGH.
When the PLL goes to either synchronous or asynchronous powerdown mode, preamp becomes debiased, R & N counters keeps their load conditions and the charge pump becomes high impedance state. The oscillator circuitry function becomes disabled only when both IF and RF powerdown bits are activated, i.e. N20 HIGH.
The PLL returns to an active powerup mode when N20 bit becomes LOW(either in synchronous or asynchronous modes).

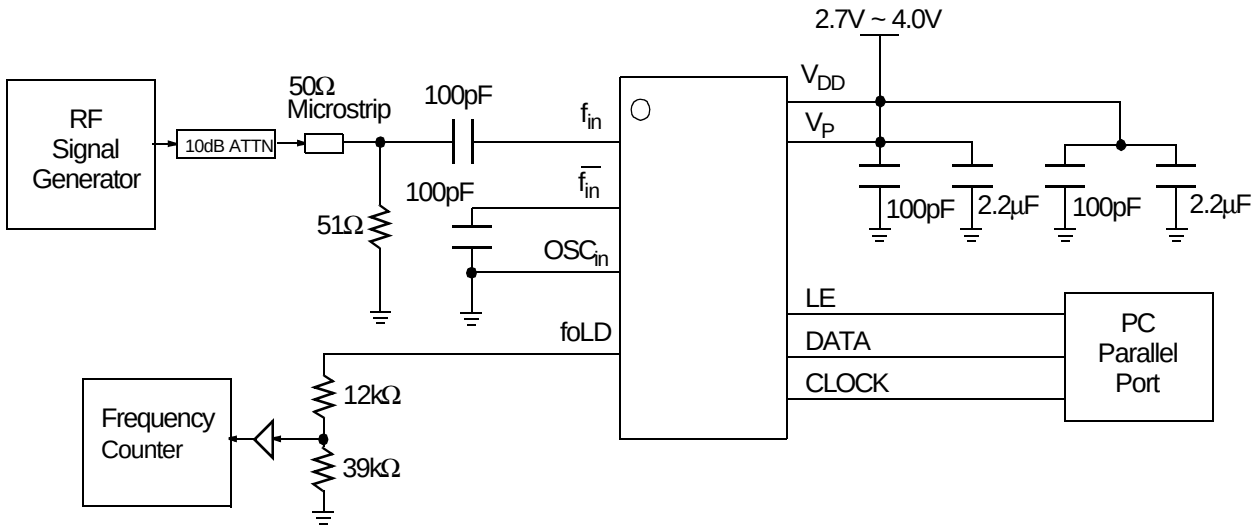
R18	N20	Powerdown mode status
0	0	PLL active
1	0	PLL active, only charge pump high impedance
0	1	Synchronous powerdown
1	1	Asynchronous powerdown

Phase Detector and Charge pump Characteristics

Phase difference detection range : $-2\pi \sim +2\pi$
When R16 = HIGH

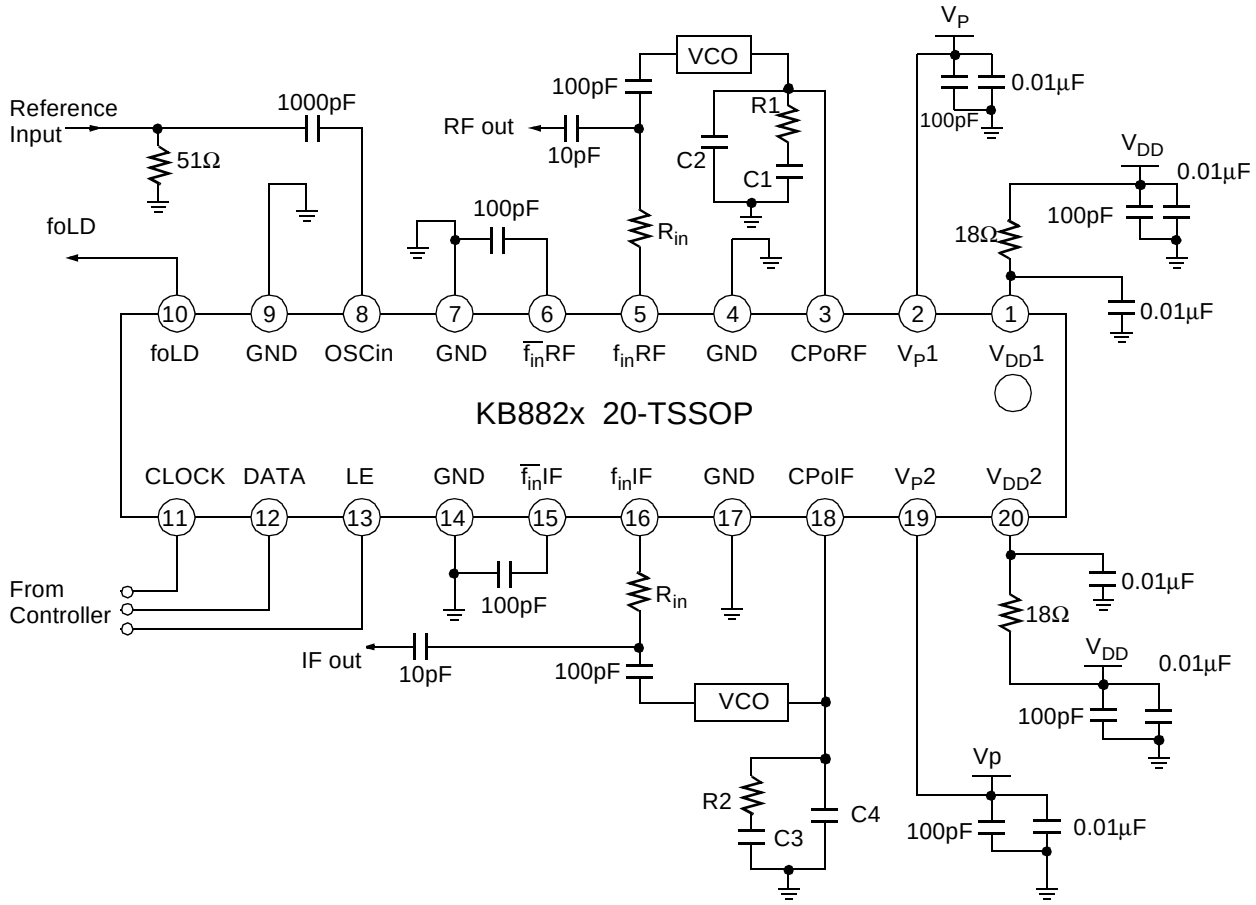


RF SENSITIVITY MEASUREMENT CIRCUIT



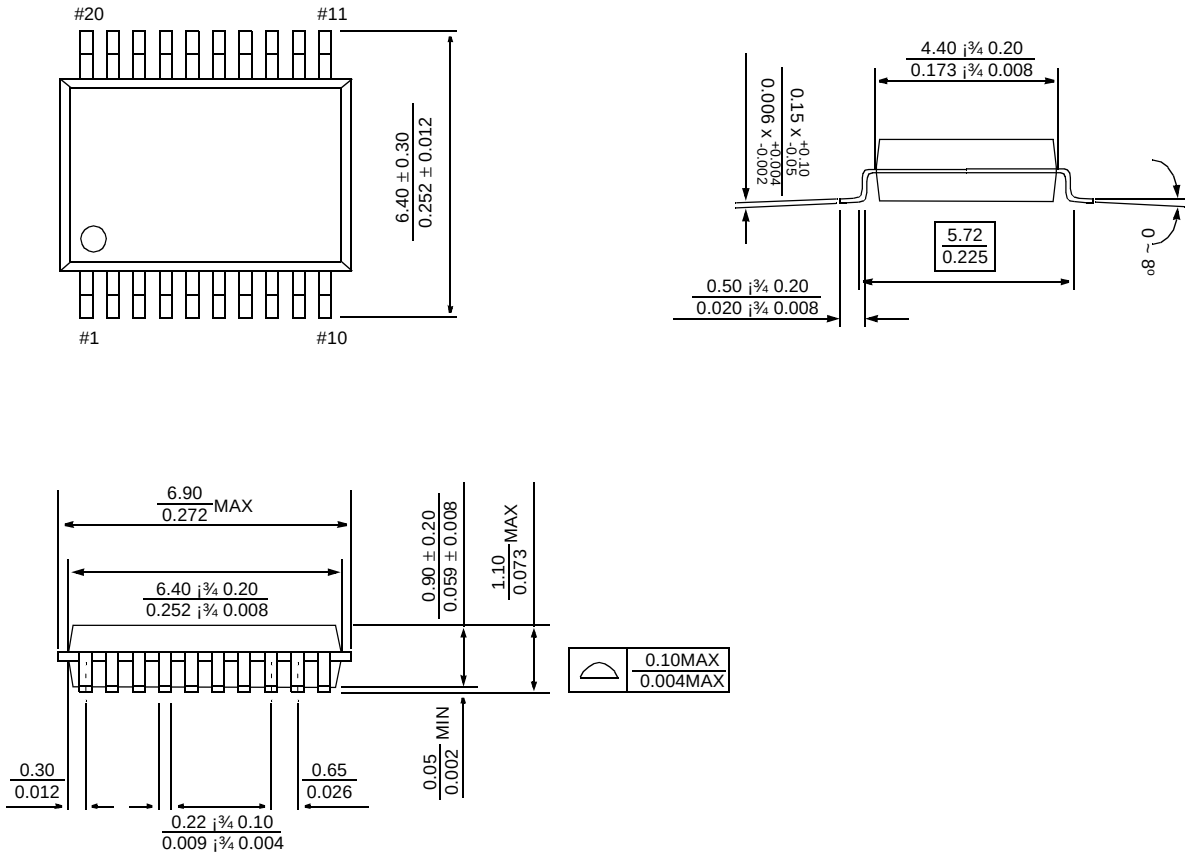
** N=10,000 R=50 P=64
** Sensitivity limit is determined when the error of the divided RF output(foLD) becomes ≥1 Hz.

TYPICAL APPLICATION CIRCUIT



** The role of Rin : Rin makes VCO output power go to the load rather than the PLL.
The value of Rin depends on the VCO power level.

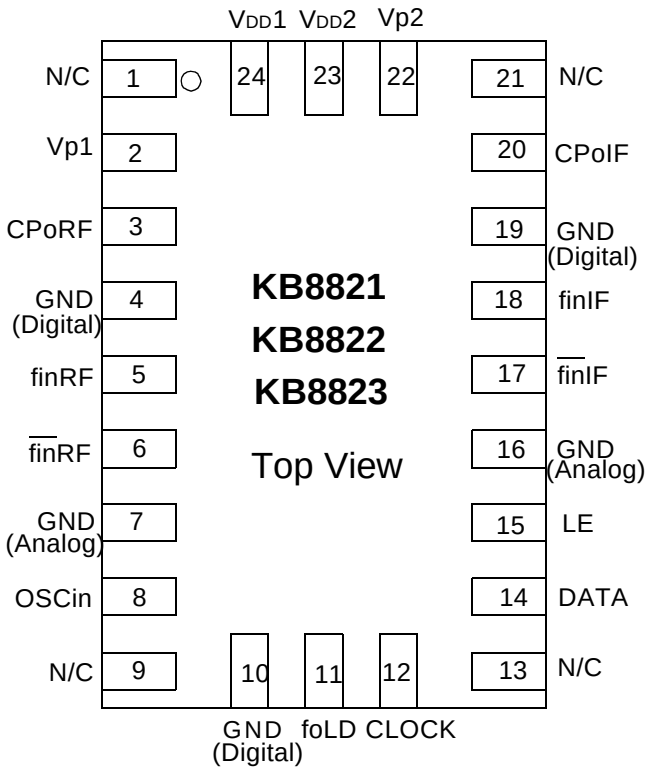
PACKAGE DIMENSIONS



20-Lead TSSOP Package
(Samsung 20-TSSOP-225)

Addendum(for 24-QFN package)

PIN CONFIGURATION(24-QFN, not to scale)



* N/C pins must be connected to GND(to Analog GND if possible).

24-QFN

24 PIN Quad Flat Non-leaded (24-QFN) Package

1. pin #10 = pin #19(internally connected).
2. Do not tie up Vp and V_{DD}
   : Vp is the source of digital noises. The power for analog part is supplied by V_{DD}. If Vp and V_{DD} are tied together, noisy Vp corrupts the power source for the analog part.

PIN DESCRIPTION(24-QFN)

Pin No (20-TSSOP)	Pin No (24QFN)	Symbol	I / O	Description
1	24	$V_{DD}1$	-	Power supply voltage input for the RF PLL part. $V_{DD}1$ must equal $V_{DD}2$. In order to reject supply noise, bypass capacitors must be placed as close as possible to this pin and be connected directly to the ground plane.
-	1	-	N/C	No connection.
2	2	Vp1	-	Power supply voltage input for RF charge pump($\geq V_{DD}1$).
3	3	CPoRF	O	Internal RF charge pump output for connection to an external loop filter whose filtered output drives an external VCO.
4	4	GND	-	Ground for RF digital blocks.
5	5	finRF	I	RF prescaler input. The signal comes from the external VCO.
6	6	$\overline{\text{fin}}$RF	I	The complementary input of the RF prescaler. A bypass capacitor must be placed as close as possible to this pin and be connected directly to the ground plane. The bypass capacitor is optional with some loss of sensitivity.
7	7	GND	-	Ground for RF analog blocks.
8	8	OSCin	I	Reference counter input. TCXO is connected via a coupling capacitor.
-	9	-	N/C	No connection.
9	10	GND	-	Ground for IF digital blocks.
10	11	f_{oLD}	O	Multiplexed output of the RF/IF programmable counters, the reference counters, the lock detect signals and the shift registers. The output level is CMOS level. (see f_{out} Programmable Truth Table)
11	12	CLOCK	I	CMOS clock input. Serial data for the various counters is transfered into the 22-bit shift register on the rising edge of the clock signal.
-	13	-	N/C	No connection.
12	14	DATA	I	Binary serial data input. The MSB of CMOS input data is entered first. The control bits are on the last two bits. CMOS input.
13	15	LE	I	Load enable CMOS input. When LE becomes high, the data in the shift register is loaded into one of the four latches(by the control bits).
14	16	GND	-	Ground for IF analog blocks.
15	17	$\overline{\text{fin}}$IF	I	The complementary input of the IF prescaler. A bypass capacitor must be placed as close as possible to this pin and be connected directly to the ground plane. The bypass capacitor is optional with some loss of sensitivity.
16	18	finIF	I	IF prescaler input. The signal comes from the external VCO.
17	19	GND	-	Ground for IF digital blocks.
18	20	CPoIF	O	Internal IF charge pump output for connection to an external loop filter whose filtered output drives an external VCO.
-	21	-	N/C	No connection.
19	22	Vp2	-	Power supply voltage input for IF charge pump($\geq V_{DD}2$)

20	23	$V_{DD}2$	-	Power supply voltage input for the IF PLL part. $V_{DD}1$ must equal $V_{DD}2$. In order to reject supply noise, bypass capacitors must be placed as close as possible to this pin and be connected directly to the ground plane.