3.6 Memory Module (K5L5563CAA-D770)

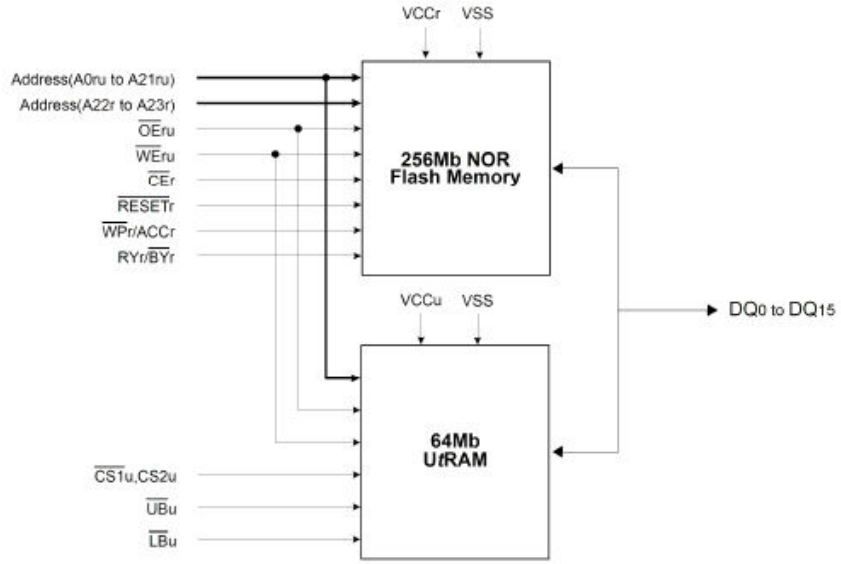

Figure.3-6-1 K5L5563CAA-D770 FUNCTIONAL BLOCK DIAGRAM

3.6.1 FEATURES

<Common>

- Operating Temperature : -25℃ ~ 85℃
- Package : 84Ball FBGA _ 8.0mm x 11.6mm x 1.2mmt 0.8mm ball pitch

<NOR Flash>

- Single Voltage, 2.7V to 3.1V for Read and Write operations
- Organization
  16M x16 bit (Word mode Only)
- Fast Read Access Time : 70ns
- Page Mode Operation
  8 Words Page access allows fast asychronous read
  Page Read Access Time : 30ns
- Read While Program/Erase Operation
- Multiple Bank architectures (4 banks)
  Bank 0: 32Mbit (32Kw x 4 and 128Kw x 15)
  Bank 1: 96Mbit (128Kw x 48)
  Bank 2: 96Mbit (128Kw x 48)
  Bank 3: 32Mbit (32Kw x 4 and 128Kw x 15)
- OTP Block : Extra 256 word
  - 128word for factory and 128word for customer OTP
- Power Consumption (typical value)
  - Active Read Current: 30mA (@5MHz)
  - Program/Erase Current: 25mA
  - Read While Program or Read While Erase Current: 65mA
  - Standby Mode/Auto Sleep Mode: 20uA

• Support Single & 32word Buffer Program
• WP/ACC input pin
- Allows special protection of two outermost boot blocks on both ends of flash array at VIL, regardless of block protect status
- Removes special protection at VIH, the two outermost blocks on both ends of flash array return to normal block protect status
- Reduce program time at VHH : 6us/word at Write Buffer
• Erase Suspend/Resume
• Program Suspend/Resume
• Unlock Bypass Program
• Hardware /RESET Pin
• Command Register Operation
• Supports Common Flash Memory Interface
• Endurance: 100,000 Program/Erase Cycles Minimum
• Data Retention: 10 years
<UtRAM>
• Process technology: CMOS
• Organization: 4M x 16 bit
• Power supply voltage: 2.7V~3.1V
• 4-Page Read
• Three state outputs
• Supports power saving modes
Internal TCSR (Temperature Compensated Self Refresh)

3.6.2 GENERAL DESCRIPTION

The K5L5563CAA is a Multi Chip Package Memory which combines 256Mbit NOR Flash Memory and 64Mbit Page UtRAM.

The 256Mb NOR F lash featuring single 3.0V power supply, is an 256Mbit NOR-type Flash Memory organized as 16M x16. The memory architecture of the device is designed to divide its memory arrays into 134 blocks with independent hardware protection. This block architecture provides highly flexible erase and program capability. The NOR Flash consists of four banks. This device is capable of reading data from one bank while programming or erasing in the other banks. The device offers fast page access time of 30ns with random access time of 70ns. The device's fast access times allow high speed microprocessors to operate without wait states. The device performs a program operation in unit of 16 bits (Word) and erases in units of a block. Single or multiple blocks can be erased. The block erase operation is completed within typically 1.6 sec. The device requires 15mA as program/erase current in the commercial and extended temperature ranges.

The 64Mb UtRAM is fabricated by SAMSUNG′ s advanced CMOS technology using one transistor memory cell. The device supports 4 page read operation and Industrial temperature range. The device also supports internal Temperature Compensated Self Refresh mode for the standby power saving at room temperature range.

The K5L5563CAA is suitable for the memory of mobile communication system to reduce not only mount area but also power consumption. This device is available in 84-ball FBGA package.

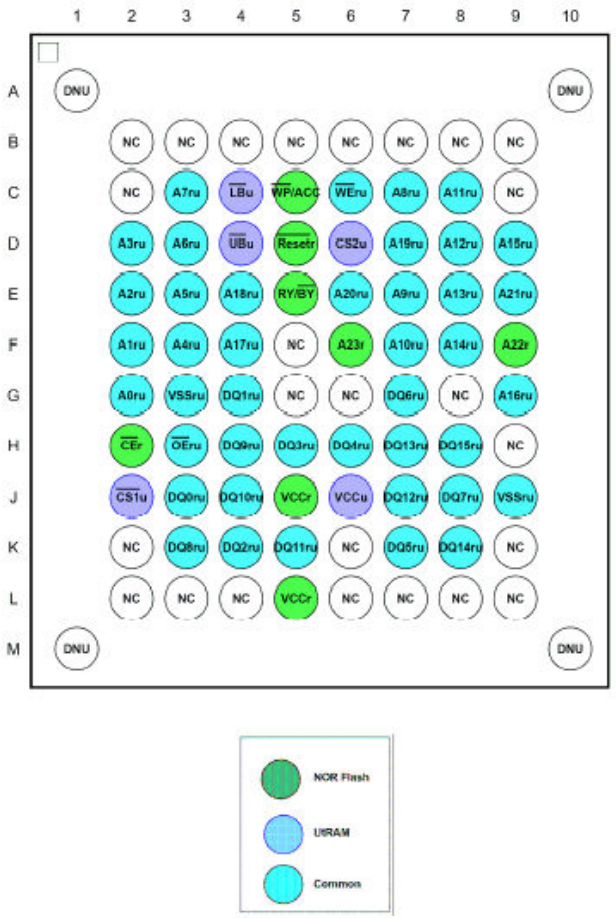

Figure.3-6-2 K5L5563CAA-D770 PIN CONFIGURATION

Ball Name	Description	Ball Name	Description
A0 to A21	Address Inputs (Common)	$\overline{WE}$	Write Enable (Common)
A22 to A23	Address Inputs (NOR)	$\overline{UB}$u	Upper Byte (UtRAM)
DQ0 to DQ15	Data Input/output (Common)	$\overline{LB}$u	Lower Byte (UtRAM)
$\overline{CE}$r	Chip Enable (NOR)	Vccr	Power Supply (NOR)
$\overline{CS}$1u,CS2u	Chip Select (UtRAM)	Vccu	Power Supply (UtRAM)
$\overline{OE}$	Output Enable (Common)	Vss	Ground (Common)
$\overline{RESET}$	Hardware Reset (NOR)	NC	No Connection
$\overline{WP}$/ACC	Hardware Write Protection/ Program Acceleration (NOR)	DNU	Do Not Use
RY/$\overline{BY}$	Ready/Busy Output (NOR)		

Figure.3-6-3 K5L5563CAA-D770 PIN Description