

DUAL OPERATIONAL AMPLIFIER

■ GENERAL DESCRIPTION

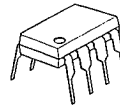
The NJM4558/4559 integrated circuit are a dual high-gain operational amplifier internally compensated and constructed on a single silicon chip using an advanced epitaxial process.

Combining the features of the NJM741 with the close parameter matching and tracking of a dual device on a monolithic chip results in unique performance characteristics. Excellent channel separation allow the use of the dual device in single NJM741 operational amplifier applications providing density. It is especially well suited for applications in differential-in, differential-out as well as in potentiometric amplifiers and where gain and phase matched channels are mandatory.

■ FEATURES

- Operating Voltage (±4V ~ ±18V)
- High Voltage Gain (100dB typ.)
- High Input Resistance (5MΩ typ.)
- Package Outline DIP8, DMP8, SIP8, SSOP8
- Bipolar Technology

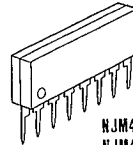
■ PACKAGE OUTLINE



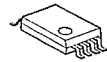
NJM4558D  
NJM4559D



NJM4558M  
NJM4559M

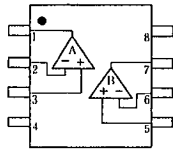


NJM4558L  
NJM4559L

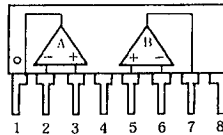


NJM4558V  
NJM4559V

■ PIN CONFIGURATION



NJM4558D, NJM4558M, NJM4558V  
NJM4559D, NJM4559M, NJM4559V

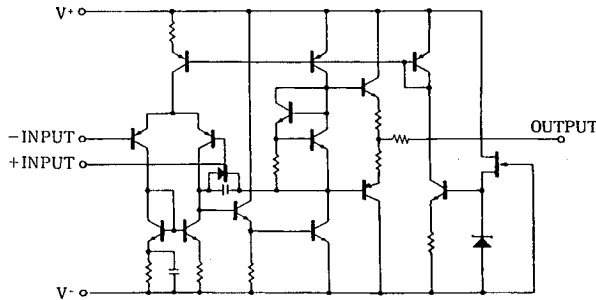


NJM4558L  
NJM4559L

PIN FUNCTION

1. A OUTPUT
2. A-INPUT
3. A+INPUT
4. V-
5. B+INPUT
6. B-INPUT
7. B OUTPUT
8. V+

■ EQUIVALENT CIRCUIT (1/2 Shown)



## ■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V <sup>+</sup> /V <sup>-</sup>	±18	V
Differential Input Voltage	V <sub>ID</sub>	±30	V
Input Voltage	V <sub>IC</sub>	±15 (note)	V
Power Dissipation	P <sub>D</sub>	(DIP8) 500	mW
		(DMP8) 300	mW
		(SSOP8) 250	mW
		(SIP8) 800	mW
Operating Temperature Range	T <sub>opr</sub>	-40 ~ +85	°C
Storage Temperature Range	T <sub>stg</sub>	-40 ~ +125	°C

(note) For supply voltage less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

## ■ ELECTRICAL CHARACTERISTICS

(V<sup>+</sup>/V<sup>-</sup> = ±15V Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V <sub>IO</sub>	R <sub>s</sub> ≤ 10kΩ	—	0.5	6	mV
Input Offset Current	I <sub>IO</sub>		—	5	200	nA
Input Bias Current	I <sub>B</sub>		—	25	500	nA
Input Resistance	R <sub>IN</sub>		0.3	5	—	MΩ
Large Signal Voltage Gain	A <sub>V</sub>	R <sub>L</sub> ≥ 2kΩ, V <sub>O</sub> = ±10V	86	100	—	dB
Maximum Output Voltage Swing 1	V <sub>OM1</sub>	R <sub>L</sub> ≥ 10kΩ	±12	±14	—	V
Maximum Output Voltage Swing 2	V <sub>OM2</sub>	R <sub>L</sub> ≥ 2Ω	±10	±13	—	V
Input Common Mode Voltage Range	V <sub>ICM</sub>		±12	14	—	V
Common Mode Rejection Ratio	CMR	R <sub>S</sub> ≤ 10kΩ	70	90	—	dB
Supply Voltage Rejection Ratio	SVR	R <sub>S</sub> ≤ 10kΩ	76.5	90	—	dB
Operating Current	I <sub>CC</sub>		—	3.5	5.7	mA
Slew Rate						
NJM4558	SR		—	1	—	V/μS
NJM4559	SR		—	2	—	V/μS
Equivalent Input Noise Voltage	V <sub>NI</sub>	RIAA, R <sub>S</sub> = 1kΩ, 30kHz LPF	—	1.4	—	μVrms
Gain Bandwidth Product	GB					
NJM4558				3		MHz
NJM4559				6		MHz