

## 150mA Dual LDO with Low Noise, High PSRR, and Low I<sub>Q</sub>

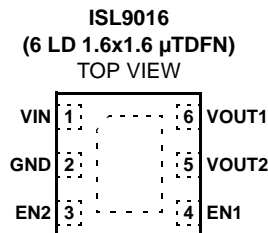
ISL9016 is a high performance dual LDO capable of providing up to 150mA current on each channel. It features a low standby current and very high PSRR and is stable with output capacitance of 1 $\mu$ F to 4.7 $\mu$ F with an ESR of up to 200m $\Omega$ .

The device integrates a separate enable function for each output. The quiescent current is typically 49 $\mu$ A when only one LDO is enabled and typically 80 $\mu$ A when both LDOs are enabled. When both LDOs are under shutdown condition, the drawing current is typically less than 1 $\mu$ A.

ISL9016 provides a wide input voltage range from 1.8V to 6.5V. It also has a high PSRR of 80dB at 1kHz and 45dB at 1MHz. ISL9016 also provides output current limit, overheat protection, reverse current protection, as well as excellent load transient response.

ISL9016 is offered in a tiny 1.6mmx1.6mm 6 Ld  $\mu$ TDFN package. Output voltage options are available from 1.2V to 3.3V. Several combinations of voltage outputs are standard and others may be available upon request.

### Pinout



### Features

- Dual Integrated 150mA High Performance LDOs
- High PSRR: 80dB @ 1kHz and 45dB @ 1MHz
- Reverse Current Protection
- Low Quiescent Current
  - 49 $\mu$ A (Single LDO Enabled)/80 $\mu$ A (Dual LDOs Enabled)
- Excellent Load Transient Response
- Typically  $\pm$ 0.8% Output Voltage Accuracy
- Low Output Noise: Typically 25 $\mu$ V<sub>RMS</sub>
- Wide Input Voltage Capability: 1.8V to 6.5V
- Low Dropout Voltage: Typically 120mV @ 150mA
- Separate Enable Control for each LDO
- Stable with 1 $\mu$ F to 4.7 $\mu$ F Ceramic Output Capacitors
- Soft-start to Limit Input Current Surge During Enable
- Current Limit and Overheat Protection
- Tiny 6 Ld 1.6mmx1.6mm  $\mu$ TDFN package
- Pb-free (RoHS Compliant)

### Applications

- PDAs, Cell Phones and Smart Phones
- Portable Instruments, MP3/4 Players, PMP, DSC
- Handheld Devices including Medical Handhelds

## Ordering Information

PART NUMBER (Notes 1, 3)	PART MARKING	VO1 VOLTAGE (V) (Note 2)	VO2 VOLTAGE (V) (Note 2)	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG DWG. #
ISL9016IRUWCZ-T	N7	1.2	1.8	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUWGZ-T	N6	1.2	2.7	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUWJZ-T	N2	1.2	2.8	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUWKZ-T	N1	1.2	2.85	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUBWZ-T	R7	1.5	1.2	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUBBZ-T	R6	1.5	1.5	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUCWZ-T	R5	1.8	1.2	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUCBZ-T	R4	1.8	1.5	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUFWZ-T	R3	2.5	1.2	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUFBZ-T	N8	2.5	1.5	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUFCZ-T	N9	2.5	1.8	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUFFZ-T	P0	2.5	2.5	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUGWZ-T	P1	2.7	1.2	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUGCZ-T	R2	2.7	1.8	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUGGZ-T	N3	2.7	2.7	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUJWZ-T	P2	2.8	1.2	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUJBZ-T	P3	2.8	1.5	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUJCZ-T	N4	2.8	1.8	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUJZ-T	N0	2.8	2.8	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUKWZ-T	P5	2.85	1.2	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUKFZ-T	P4	2.85	2.5	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUKKZ-T	N5	2.85	2.85	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUMWZ-T	P6	3.0	1.2	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUMBZ-T	P7	3.0	1.5	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUMCZ-T	P8	3.0	1.8	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUMKZ-T	P9	3.0	2.85	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUNWZ-T	R0	3.3	1.2	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A
ISL9016IRUNCZ-T	R1	3.3	1.8	-40 to +85	6 Ld $\mu$ TDFN	L6.1.6x1.6A

### NOTES:

1. Please refer to TB347 for details on reel specifications.
2. For other output voltages, contact Intersil marketing or local sales office.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

**Absolute Maximum Ratings**

$V_{IN}$ to GND	-0.3V to +7.1V
All Other Pins to GND	-0.3 to ( $V_{IN} + 0.3$ )V

**Recommended Operating Conditions**

Supply Voltage ( $V_{IN}$ )	1.8V to 6.5V
Each LDO Load Current	up to 150mA
Ambient Temperature Range ( $T_A$ )	-40°C to +85°C

**Thermal Information**

Thermal Resistance	$\theta_{JA}$ (°C/W)
6 Ld $\mu$ TDFN Package (Note 4)	117.5
Junction Temperature Range	-40°C to +125°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Pb-Free Reflow Profile	see link below <a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

**NOTE:**

- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

**Electrical Specifications**

Unless otherwise noted, all parameter limits are guaranteed over the recommended operating conditions and the typical specifications are measured at the following conditions:  $T_A = +25^\circ\text{C}$ ;  $V_{IN} = (V_O + 0.5\text{V})$  to 6.5V with a minimum  $V_{IN}$  of 1.8V;  $C_{IN} = 1\mu\text{F}$ ;  $C_O = 1\mu\text{F}$ . Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC CHARACTERISTICS</b>						
Supply Voltage	$V_{IN}$		1.8		6.5	V
UVLO Threshold	$V_{UV+}$			1.710	1.775	V
	$V_{UV-}$		1.55	1.62		
Input Quiescent Current		Quiescent condition: $I_{O1} = 0\mu\text{A}$ ; $I_{O2} = 0\mu\text{A}$				
	$I_{DD1}$	One LDO active		49	67	$\mu\text{A}$
	$I_{DD2}$	Both LDO active		80	100	$\mu\text{A}$
Shutdown Current	$I_{DDS}$	@ +25°C		0.1	1.0	$\mu\text{A}$
Regulation Voltage Accuracy		$V_{IN} = V_O + 0.5\text{V}$ to 6.5V, $I_O = 10\mu\text{A}$ to 150mA, $T_A = +25^\circ\text{C}$	-0.8		+0.8	%
		$V_{IN} = V_O + 0.5\text{V}$ to 6.5V, $I_O = 10\mu\text{A}$ to 150mA, $T_A = -40^\circ\text{C}$ to +85°C	-1.8		+1.8	%
Maximum Output Current	$I_{MAX}$	Each LDO, Continuous	150			mA
Internal Current Limit	$I_{LIM}$		175	265	355	mA
Dropout Voltage (Note 5)	$V_{DO1}$	$I_O = 150\text{mA}$ ; $1.2\text{V} \leq V_O \leq 2.1\text{V}$		250	425	mV
	$V_{DO2}$	$I_O = 150\text{mA}$ ; $2.1\text{V} \leq V_O \leq 2.8\text{V}$		200	325	mV
	$V_{DO3}$	$I_O = 150\text{mA}$ ; $2.8\text{V} \leq V_O$		120	200	mV
Thermal Shutdown Temperature	$T_{SD+}$			145		°C
	$T_{SD-}$			110		°C
<b>AC CHARACTERISTICS</b>						
Ripple Rejection		$I_O = 10\text{mA}$ , $V_{IN} = 3.7\text{V}(\text{min})$ , $V_O = 2.7\text{V}$ , $T_A = +25^\circ\text{C}$				
		@ 1kHz		80		dB
		@ 10kHz		60		dB
		@ 100kHz		50		dB
		@ 1MHz		45		dB
Output Noise Voltage		$V_{IN} = 4.2\text{V}$ , $I_O = 10\text{mA}$ , $T_A = +25^\circ\text{C}$ , BW = 10Hz to 100kHz		25		$\mu\text{V}_{RMS}$
<b>DEVICE START-UP CHARACTERISTICS</b>						
Device Enable Time	$t_{EN}$	Time from assertion of the ENx pin to when the output voltage reaches 95% of the $V_O(\text{nom})$		400	600	$\mu\text{s}$

**Electrical Specifications**

Unless otherwise noted, all parameter limits are guaranteed over the recommended operating conditions and the typical specifications are measured at the following conditions:  $T_A = +25^\circ\text{C}$ ;  $V_{IN} = (V_O + 0.5\text{V})$  to 6.5V with a minimum  $V_{IN}$  of 1.8V;  $C_{IN} = 1\mu\text{F}$ ;  $C_O = 1\mu\text{F}$ . Parameters with MIN and/or MAX limits are 100% tested at  $+25^\circ\text{C}$ , unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LDO Soft-Start Ramp Rate	$t_{SSR}$	Slope of linear portion of LDO output voltage ramp during start-up		30	60	$\mu\text{s/V}$
<b>EN PIN CHARACTERISTICS</b>						
Input Low Voltage	$V_{IL}$	$T_A = -20^\circ\text{C}$ to $+85^\circ$	-0.3		0.4	V
Input High Voltage	$V_{IH}$		1.1		$V_{IN} + 0.3$	V
Input Leakage Current	$I_{IL}, I_{IH}$				0.1	$\mu\text{A}$
<b>REVERSE CURRENT CHARACTERISTICS</b>						
Output Reverse Leakage Current (Note 6)	$I_{ORLC}$	$V_{IN} = 0\text{V}, V_{OUT} = 5.5\text{V}$		8	15	$\mu\text{A}$

## NOTES:

- $V_{OX} = 0.98 \cdot V_{OX}(\text{NOM})$ ; Valid for  $V_{OX}$  greater than 1.80V.
- Output reverse leakage current is measured with  $V_{IN}$  pin grounded and  $V_{OUT}$  pin connected to 5.5V.

Typical Operating Performance

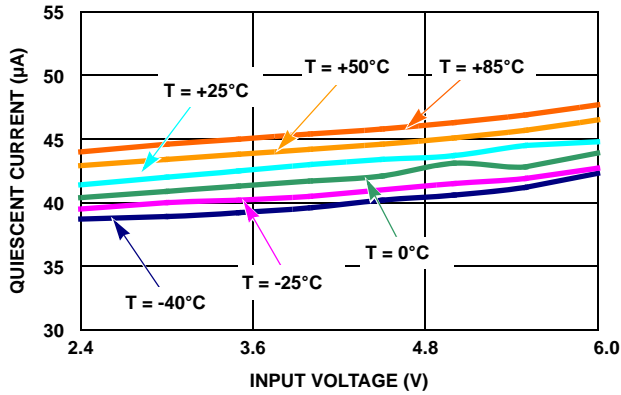


FIGURE 1. QUIESCENT CURRENT vs INPUT VOLTAGE (V<sub>OUT1</sub> = 2.1V, ONLY LDO1 ENABLED)

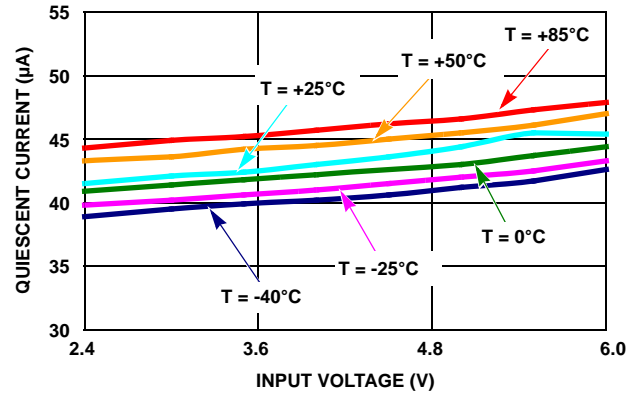


FIGURE 2. QUIESCENT CURRENT vs INPUT VOLTAGE (V<sub>OUT2</sub> = 2.1V, ONLY LDO2 ENABLED)

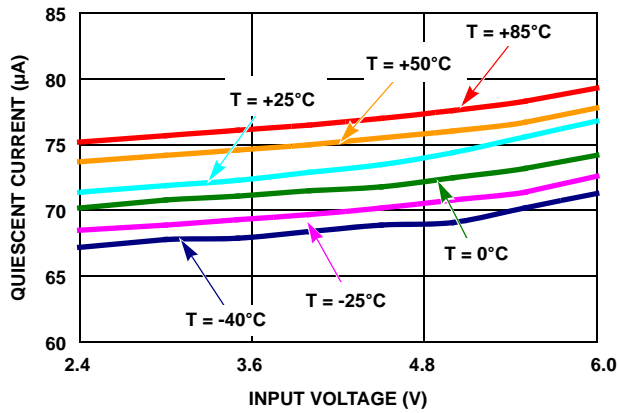


FIGURE 3. QUIESCENT CURRENT vs INPUT VOLTAGE (V<sub>OUT1</sub> = V<sub>OUT2</sub> = 2.1V, LDO1 AND LDO2 ENABLED)

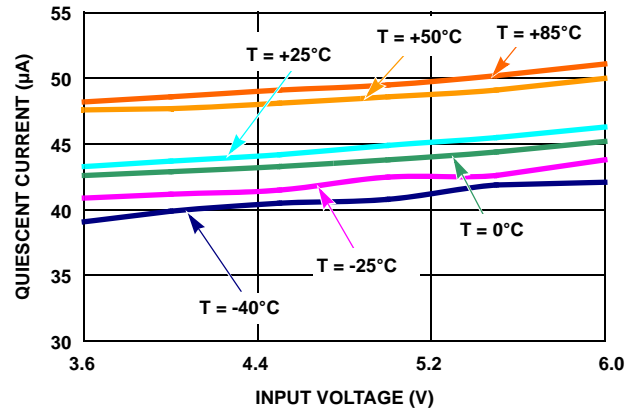


FIGURE 4. QUIESCENT CURRENT vs INPUT VOLTAGE (V<sub>OUT1</sub> = 3.3V, ONLY LDO1 ENABLED)

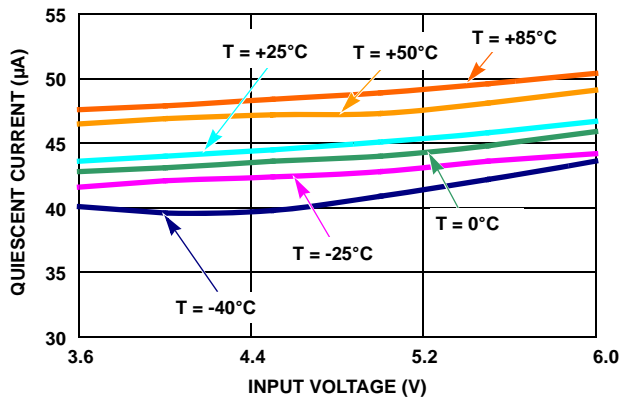


FIGURE 5. QUIESCENT CURRENT vs INPUT VOLTAGE (V<sub>OUT2</sub> = 3.3V, ONLY LDO2 ENABLED)

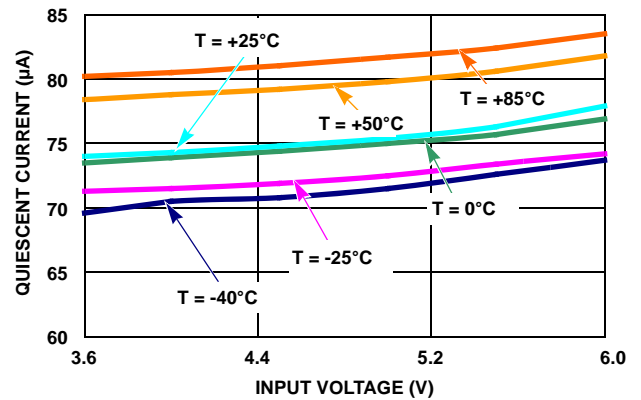


FIGURE 6. QUIESCENT CURRENT vs INPUT VOLTAGE (V<sub>OUT1</sub> = V<sub>OUT2</sub> = 3.3V, LDO1 AND LDO2 ENABLED)

Typical Operating Performance

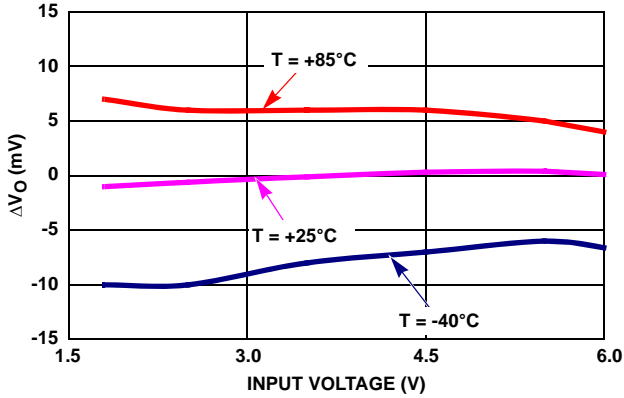


FIGURE 7.  $\Delta V_{OUT}$  vs INPUT VOLTAGE  
( $V_{OUT\_NOMINAL} = 1.2V$ ,  $I_{OUT} = 50mA$ )

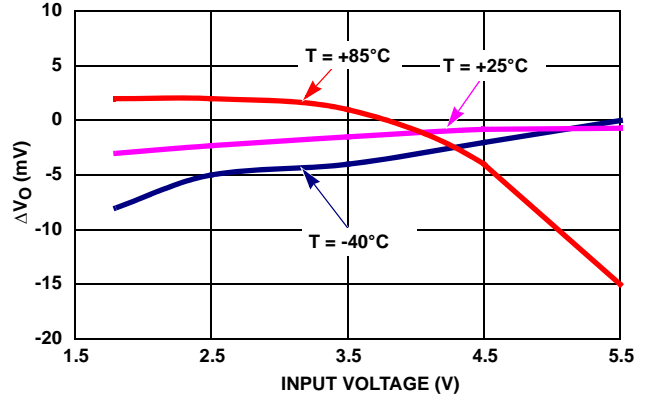


FIGURE 8.  $\Delta V_{OUT}$  vs INPUT VOLTAGE  
( $V_{OUT\_NOMINAL} = 1.2V$ ,  $I_{OUT} = 150mA$ )

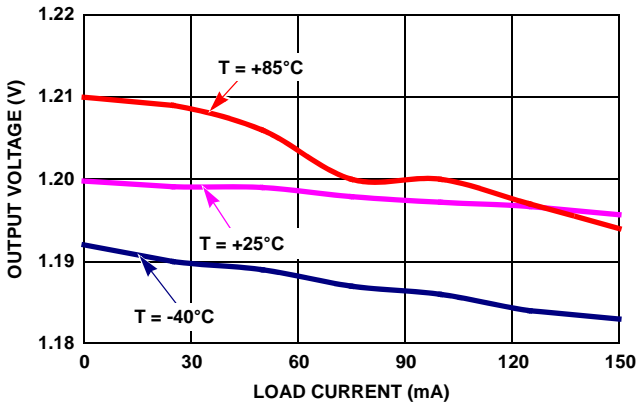


FIGURE 9. LOAD REGULATION ( $V_{IN} = 1.8V$ ,  $V_{OUT} = 1.2V$ )

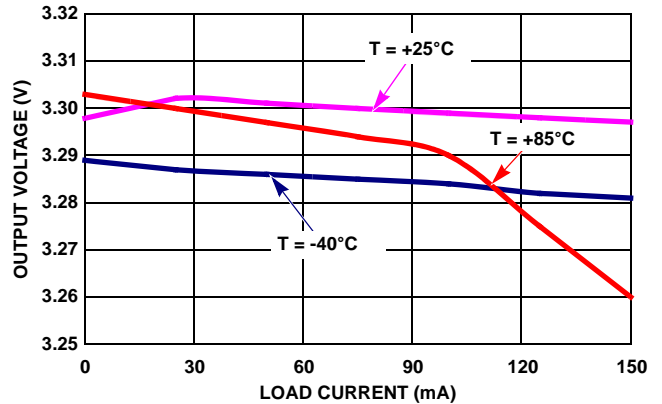


FIGURE 10. LOAD REGULATION ( $V_{IN} = 4.5V$ ,  $V_{OUT} = 3.3V$ )

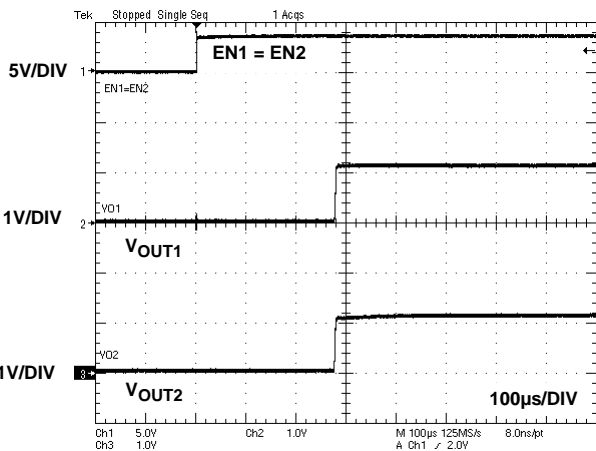


FIGURE 11. ENABLE OPERATION ( $V_{IN} = 3.6V$ ,  
 $V_{OUT1} = V_{OUT2} = 1.2V$ )

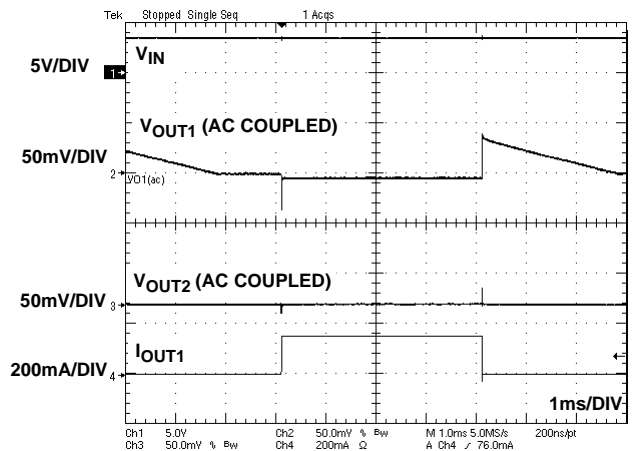


FIGURE 12. LOAD TRANSIENT RESPONSE ( $V_{IN} = 3.6V$ ,  
 $V_{OUT1} = V_{OUT2} = 1.2V$ ,  $I_{OUT1}$  0.01mA TO 150mA)

Typical Operating Performance

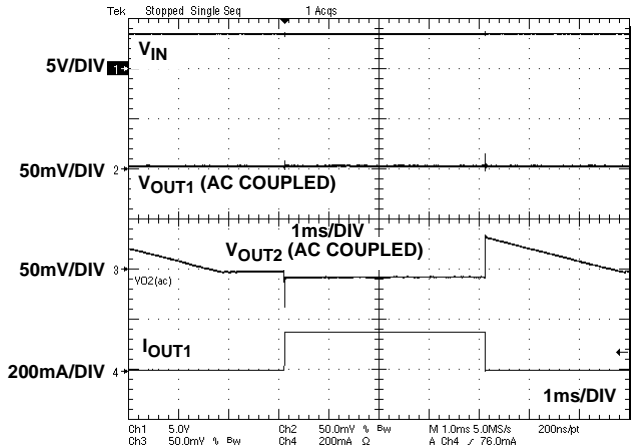


FIGURE 13. LOAD TRANSIENT RESPONSE ( $V_{IN} = 3.6V$ ,  $V_{OUT1} = V_{OUT2} = 1.2V$ ,  $I_{OUT2}$  0.01mA TO 150mA)

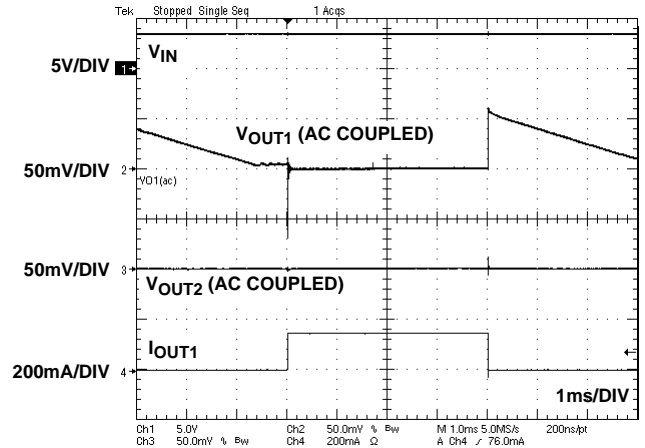


FIGURE 14. LOAD TRANSIENT RESPONSE ( $V_{IN} = 3.6V$ ,  $V_{OUT1} = V_{OUT2} = 3.3V$ ,  $I_{OUT1}$  0.01mA TO 150mA)

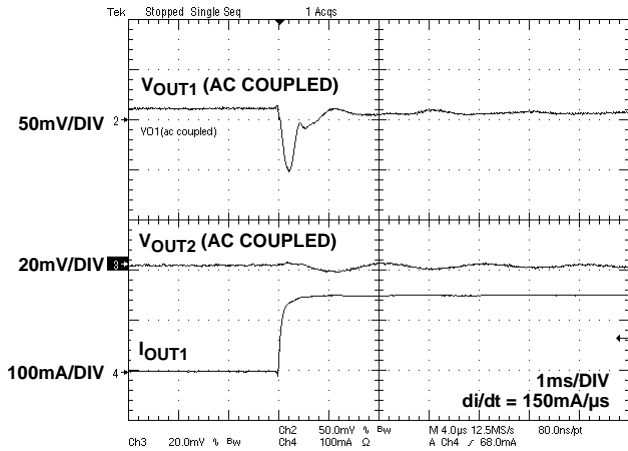


FIGURE 15. LOAD TRANSIENT RESPONSE ( $V_{IN} = 1.8V$ ,  $V_{OUT1} = V_{OUT2} = 1.2V$ ,  $I_{OUT1}$  0.01mA TO 150mA)

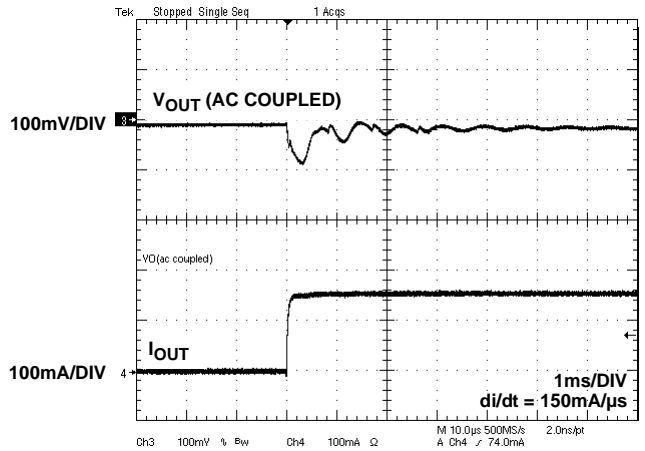
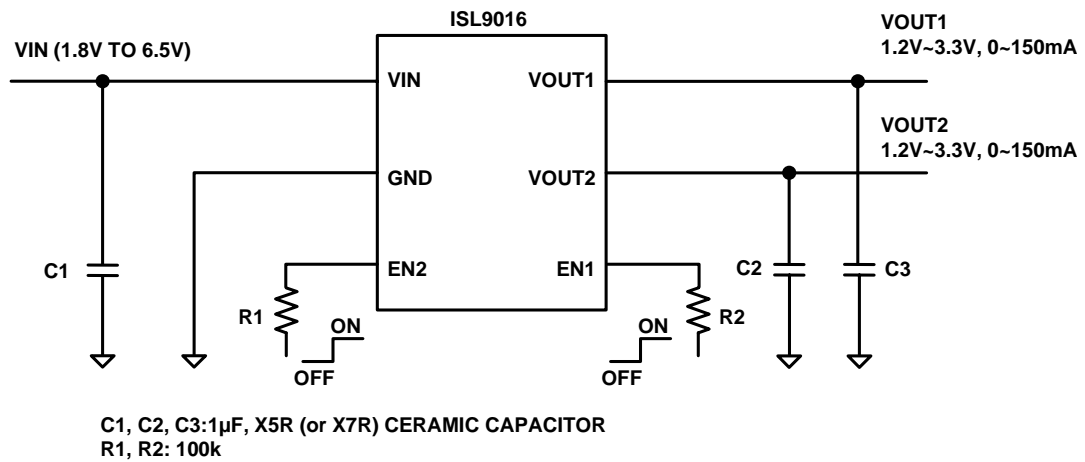


FIGURE 16. LOAD TRANSIENT RESPONSE ( $V_{IN} = 3.3V$ ,  $V_{OUT1} = V_{OUT2} = 1.2V$ ,  $I_{OUT1}$  0.01mA TO 150mA)

**Pin Descriptions**

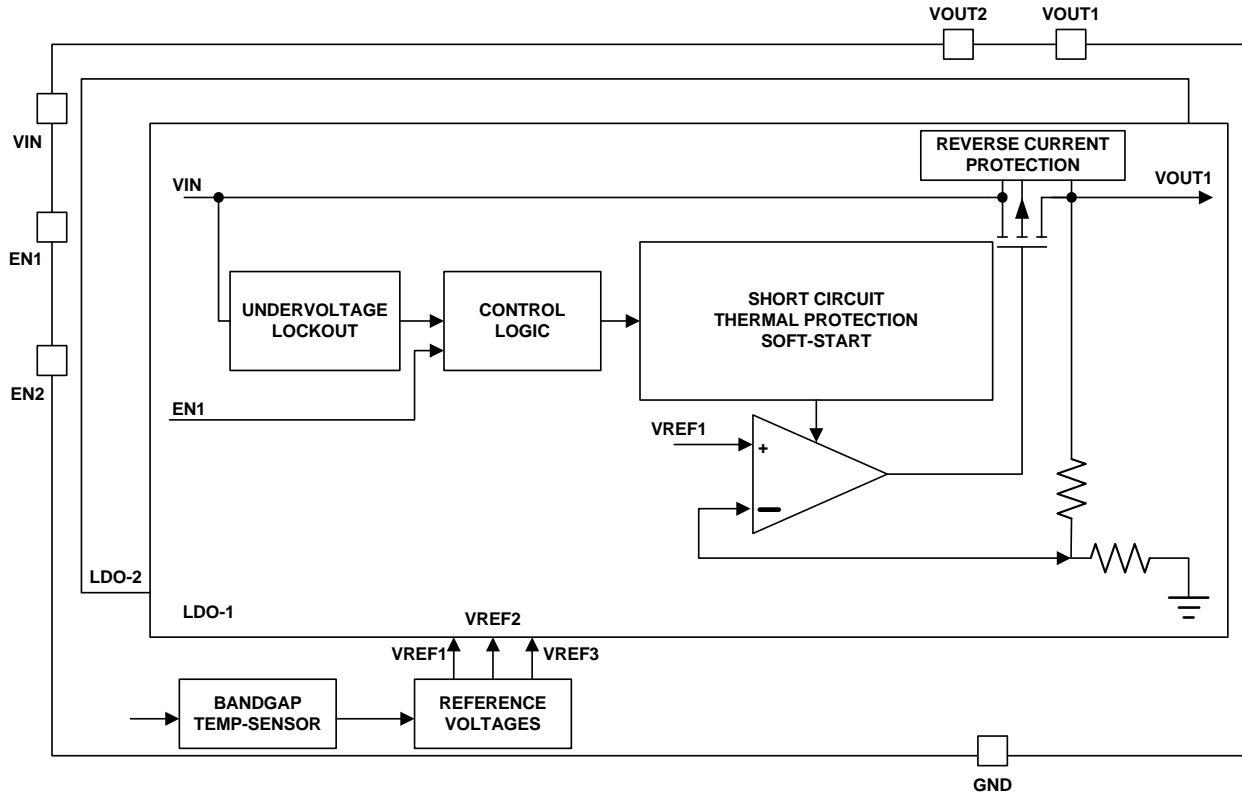
PIN #	PIN NAME	DESCRIPTION
1	VIN	Supply Voltage/LDO Input. Connect a 1 $\mu$ F capacitor to GND.
2	GND	GND is the connection to system ground. Connect to PCB Ground plane.
3	EN2	LDO2 Enable pin. Enable = High, Disable = Low. A 100k resistor should be connected between EN2 and the control voltage rail. Do NOT leave it floating.
4	EN1	LDO1 Enable pin. Enable = High, Disable = Low. A 100k resistor should be connected between EN1 and the control voltage rail. Do NOT leave it floating.
5	VOUT2	LDO2 Output. Connect capacitor with a value from 1 $\mu$ F to 4.7 $\mu$ F to GND (1 $\mu$ F recommended).
6	VOUT1	LDO1 Output. Connect capacitor with a value from 1 $\mu$ F to 4.7 $\mu$ F to GND (1 $\mu$ F recommended).
-	E-Pad	Connect the e-pad to the system ground.

**Typical Application Diagram**





## Block Diagram



## Functional Description

ISL9016 contains two high performance LDO's. High performance is achieved through a circuit which delivers fast transient response to varying load conditions. In a quiescent condition, the ISL9016 adjusts its biasing to achieve the lowest standby current consumption.

The device also integrates current limit protection, thermal shutdown protection, reverse current protection and soft-start. Thermal shutdown protects the device against overheating. Soft-start limits the start-up input current surges. In some certain application circuits, the output voltage may be externally held up, meanwhile, the input voltage could be connected to ground, or connected to some voltage lower than the output side, or be left open circuit. ISL9016 features the reverse current protection; it can limit the current flow from output to input. This protection will automatically initiate when  $V_{OUT}$  is detected to be higher than  $V_{IN}$ . When  $V_{IN}$  is pulled to ground and  $V_{OUT}$  is held at 5.5V, the current flow from  $V_{OUT}$  to  $V_{IN}$  is typically less than 8 $\mu$ A.

### Enable Control

The ISL9016 has two separate enable pins,  $EN1$  and  $EN2$ , which independently enable/disable each of the LDO outputs. When both  $EN1$  and  $EN2$  are low, the whole device is in shutdown mode. In this condition, all on-chip circuits are off, and the device draws minimum current, typically less than 0.1mA. When one or both the  $EN$  pins go high, the

LDO1 and/or LDO2 will be enabled accordingly based on the voltage signal applied on its related  $EN$  pin and start from the soft-start. Likewise, when one or both  $EN$  pins go low, LDO1 and/or LDO2 will be disabled based on the signal applied on its related  $EN$  pin. A 100k $\Omega$  (or above) pull-up resistor should be connected between  $ENx$  pin and the external control voltage (as shown in the "Typical Application Diagram" on page 8).

### LDO Protections

ISL9016 offers several protections which make it ideal for using in battery-powered application circuits.

ISL9016 provides short-circuit protection by limiting the output current to typical 265mA. When short circuit happens, the circuit is limited at 265mA (typical). If the short circuit lasts long enough, the die temperature increases, and the over-temperature protection circuit will turn off the output.

When the die temperature reaches about +145 $^{\circ}$ C, the thermal protection starts working. Under the overheat condition, only the LDO sourcing more than 50mA will be shut off. This does not affect the operation of the other LDO. If both LDOs source more than 50mA and an overheat condition occurs, both LDO outputs will be disabled. Once the die temperature falls back to about +110 $^{\circ}$ C, the disabled LDO(s) are re-enabled and soft-start automatically takes place.

In certain applications, the following input/output situations may occur:

With output voltage externally held up higher than the input voltage:

1. Input is pulled to ground;
2. input is left open circuit; and
3. input is pulled to some intermediate voltage

ISL9016 provides the reverse current protection to limit the current flow from output to input under these situations. When input is pulled to ground and output is held to 5.5V, the typical reverse current from output to input side is less than 8 $\mu$ A.

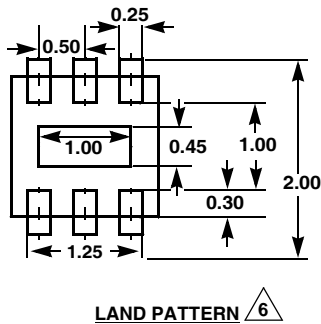
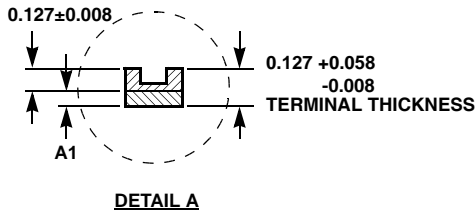
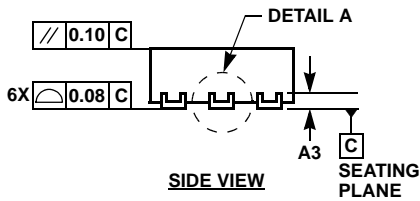
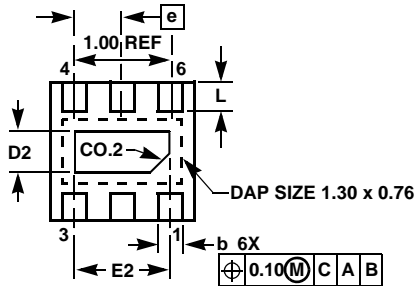
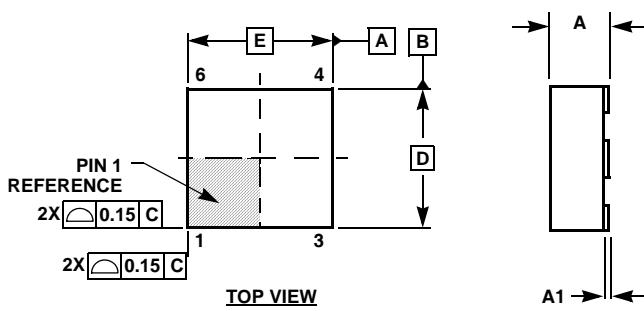
### ***Input and Output Capacitors***

The ISL9016 provides a linear regulator that has low quiescent current, fast transient response, and overall stability across the recommended operating conditions. A ceramic capacitor (X5R or X7R) with a capacitance of 1 $\mu$ F to 4.7 $\mu$ F with an ESR up to 200m $\Omega$  is suitable for ISL9016 to maintain its output stability. The ground connection of the output capacitor should be connected directly to the GND pin of the device, and also placed close to the device. Similarly for the input capacitor, usually a 1 $\mu$ F ceramic capacitor (X5R or X7R) is suitable for most cases, but if large, fast rising-time load transient condition is expected, a higher value input capacitor may be necessary to achieve better performance.

### ***Board Layout Recommendations***

A good PCB layout will be an important step to achieve good performance. It is recommended to design the board with separate ground planes for input and output, and connect both ground planes at the GND pin of the device. Consideration should be taken when placing the components and route the trace to minimize the ground impedance, as well as keep the parasitic inductance low. Usually the input/output capacitors should be placed close to the device with good ground connection.

Ultra Thin Dual Flat No-Lead Plastic Package (UTDFN)



L6.1.6x1.6A

6 LEAD ULTRA THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3	0.127 REF			-
b	0.15	0.20	0.25	-
D	1.55	1.60	1.65	4
D2	0.40	0.45	0.50	-
E	1.55	1.60	1.65	4
E2	0.95	1.00	1.05	-
e	0.50 BSC			-
L	0.25	0.30	0.35	-

Rev. 1 6/06

NOTES:

1. Dimensions are in mm. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals. Coplanarity shall not exceed 0.08mm.
3. Warpage shall not exceed 0.10mm.
4. Package length/package width are considered as special characteristics.
5. JEDEC Reference MO-229.
6. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)