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ISD4002 Series

Single-Chip Voice Record/Playback Devices
120-, 150-, 180-, and 240-Second Durations

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ChipCorder®
TECHNOLOGY BY ISD

ISD4002 Series

Single-Chip Voice Record/Playback Devices 120-, 150-, 180-, and 240-Second Durations

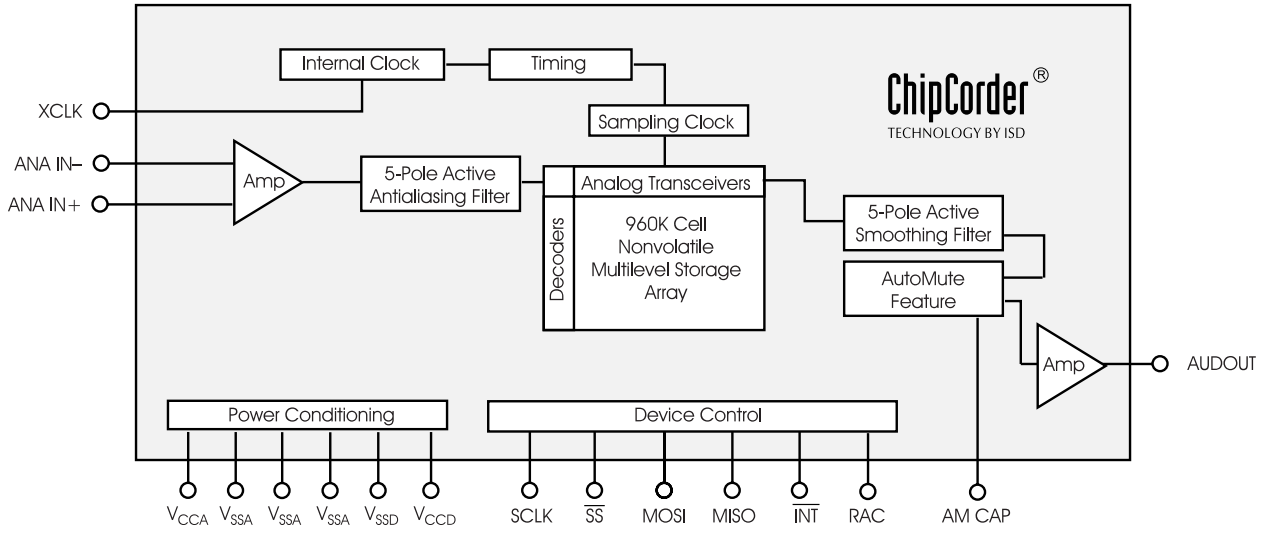
Advanced Information

GENERAL DESCRIPTION

The ISD4002 ChipCorder® products provide high-quality, 3-volt, single-chip record/playback solutions for 2- to 4-minute messaging applications ideal for cellular phones and other portable products. The CMOS-based devices include an on-chip oscillator, anti-aliasing filter, smoothing filter, AutoMute™ feature, audio amplifier, and high density, multilevel Flash storage array. The ISD4002 series is designed to be used in a microprocessor- or microcontroller-based system. Address and control are accomplished through a Serial Peripheral Interface (SPI) or Microwire Serial Interface to minimize pin count.

Recordings are stored in on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through ISD's patented multilevel storage technology. Voice and audio signals are stored directly into solid-state memory in their natural form, providing high-quality voice reproduction.

Figure: ISD4002 Series Block Diagram



FEATURES

- Single-chip voice record/playback solution
- Single +3 volt supply
- Low-power consumption
  - Operating current:
    I_{CC} Play = 15 mA (typical)
    I_{CC} Rec = 25 mA (typical)
  - Standby current: 1 µA (typical)
- Single-chip durations of 120, 150, 180, and 240 seconds
- High-quality, natural voice/audio reproduction
- AutoMute feature provides background noise attenuation during periods of silence
- No algorithm development required
- Microcontroller SPI or Microwire™ Serial Interface
- Fully addressable to handle multiple messages
- Nonvolatile message storage
- Power consumption controlled by SPI or Microwire control register
- 100-year message retention (typical)
- 100K record cycles (typical)
- On-chip clock source
- Available in die form, PDIP, SOIC, TSOP, and chip scale packaging (CSP)
- Extended temperature (–20°C to +70°C) and industrial temperature (–40°C to +85°C) versions available

Table: ISD4002 Series Summary

Part Number	Duration (seconds)	Input Sample Rate (KHz)	Typical Filter Pass Band (KHz)
ISD4002-120	120	8.0	3.4
ISD4002-150	150	6.4	2.7
ISD4002-180	180	5.3	2.3
ISD4002-240	240	4.0	1.7

DETAILED DESCRIPTION

SPEECH/SOUND QUALITY

The ISD4002 ChipCorder Series includes devices offered at 4.0, 5.3, 6.4, and 8.0 KHz sampling frequencies, allowing the user a choice of speech quality options. Increasing the duration within a product series decreases the sampling frequency and bandwidth, which affects sound quality. Please refer to the ISD4002 Series Product Summary table on the front page to compare filter pass band and product durations.

Analog speech samples are stored directly into on-chip nonvolatile memory without the digitization or compression associated with other solutions. Direct analog storage provides higher quality reproduction of voice, music, tones, and sound effects than other solid-state solutions.

DURATION

To meet end system requirements, the ISD4002 Series Products are single-chip solutions at 120, 150, 180, and 240 seconds.

FLASH STORAGE

One of the benefits of ISD's ChipCorder technology is the use of on-chip nonvolatile memory, which provides zero-power message storage. Typically, the stored message is retained for 100 years and the device can be re-recorded over 100,000 times.

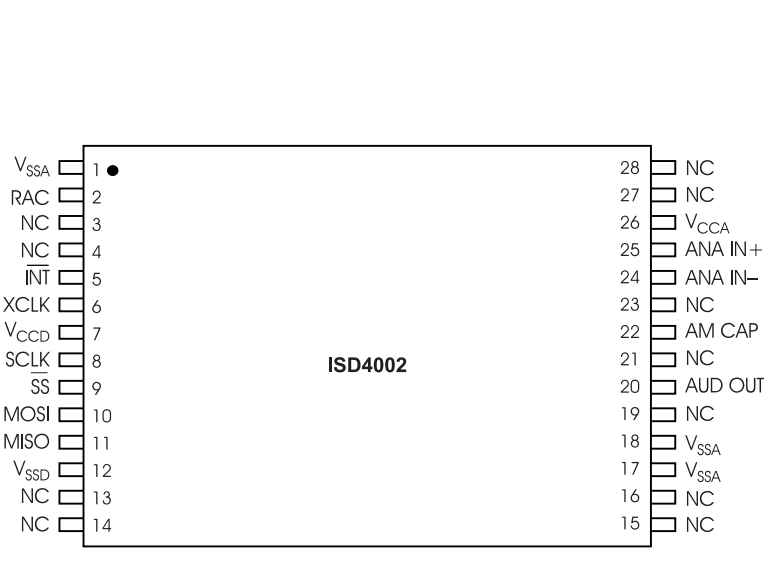
MICROCONTROLLER INTERFACE

A four-wire (SCLK, MOSI, MISO, $\overline{SS}$) SPI interface is provided for ISD4002 control and addressing functions. The ISD4002 is configured to operate as a peripheral slave device, with a microcontroller-based SPI bus interface. Read/write access to all the internal registers occurs through this SPI interface. An interrupt signal ($\overline{INT}$) and internal read-only Status Register are provided for handshake purposes.

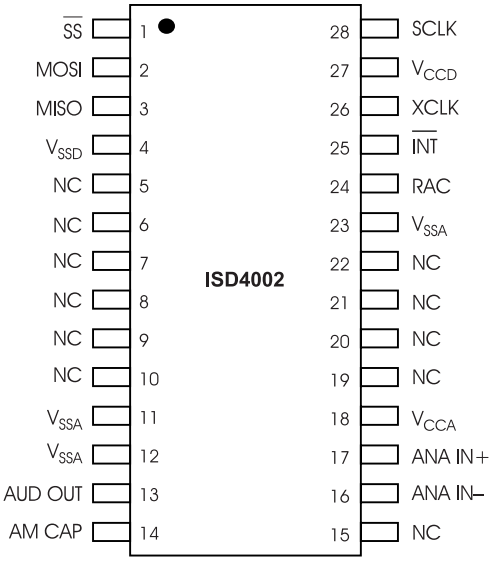
PROGRAMMING

The ISD4002 Series is also ideal for playback-only applications, where single or multiple message playback is controlled through the SPI port. Once the desired message configuration is created, duplicates can easily be generated via an ISD programmer.

Figure 1: ISD4002 Series TSOP and PDIP/SOIC Pinouts

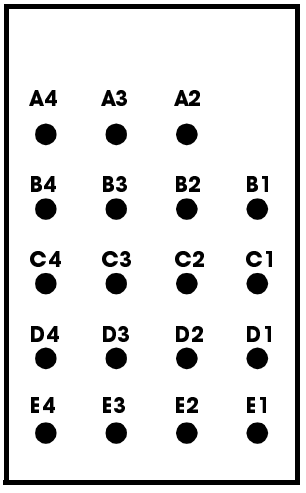


28-PIN TSOP



PDIP/SOIC

Figure 2: ISD4002 CSP Pinout



Name	Ball Location	TSOP Pin #
V_{SSA}	A2	18
AM CAP	A3	22
ANA IN+	A4	25
V_{SSA}	B1	17
AUDOUT	B2	20
ANA IN–	B3	24
V_{CCA}	B4	26
V_{SSD1}	C1	12
V_{SSD2}	C2	N/A
V_{CCD2}	C3	N/A

Name	Ball Location	TSOP Pin #
V_{SSA}	C4	1
MOSI	D1	10
SCLK	D2	8
XCLK	D3	6
RAC	D4	2
MISO	E1	11
SS	E2	9
V_{CCD1}	E3	7
INT	E4	5

PIN DESCRIPTIONS

VOLTAGE INPUTS (V_{CCA}, V_{CCD})

To minimize noise, the analog and digital circuits in the ISD4002 devices use separate power busses. These +3 V busses are brought out to separate pins and should be tied together as close to the supply as possible. In addition, these supplies should be decoupled as close to the package as possible.

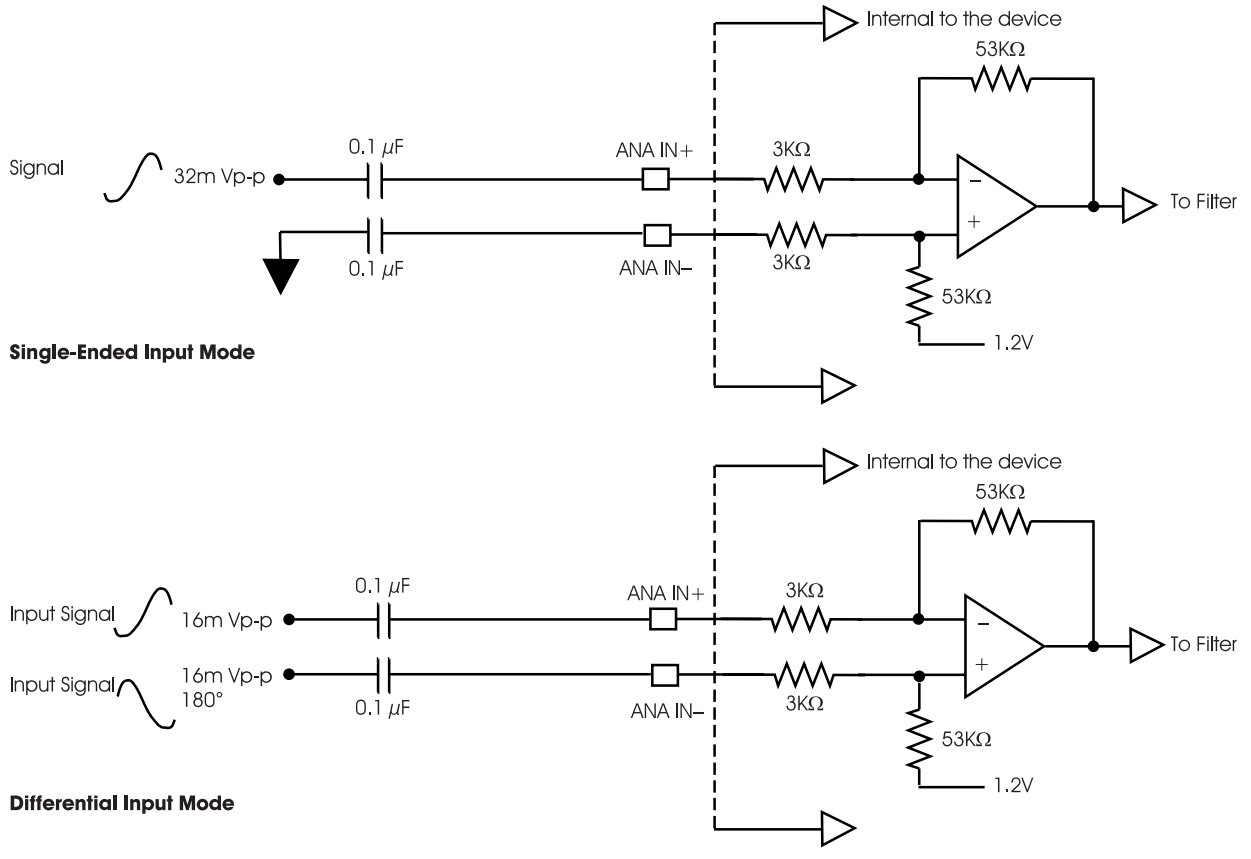
GROUND INPUTS (V_{SSA}, V_{SSD})

The ISD4002 Series utilizes separate analog and digital ground busses. The analog ground (V_{SSA}) pins should be tied together as close to the package as possible and connected through a low-impedance path to power supply ground. The digital ground (V_{SSD}) pin should be connected through a separate low-impedance path to power supply ground. These ground paths should be large enough to ensure that the impedance between the V_{SSA} pins and the V_{SSD} pin is less than 3 Ω. The backside of the die is connected to V_{SS} through the substrate resistance. In a chip-on-board design, the die attach area must be connected to V_{SS} or left floating.

NON-INVERTING ANALOG INPUT (ANA IN+)

This pin is the non-inverting analog input that transfers the signal to the device for recording. The analog input amplifier can be driven single ended or differentially. In the single-ended input mode, a 32 mVp-p (peak-to-peak) maximum signal should be capacitively connected to this pin for optimal signal quality. The external capacitor associated with ANA IN+ together with the 3 KΩ input impedance are selected to give cutoff at the low frequency end of the voice passband. In the differential-input mode, the maximum input signal at ANA IN+ should be 16 mVp-p for optimal signal quality. The circuit connections for the two modes are shown in the ISD4002 Series ANA IN Modes figures on page 3.

Figure 3: ISD4002 Series ANA IN Modes



INVERTING ANALOG INPUT (ANA IN–)

This pin is the inverting analog input that transfers the signal to the device for recording in the differential-input mode. In this differential-input mode, a 16 mVp-p maximum input signal at ANA IN– should be capacitively coupled to this pin for optimal signal quality, as shown in the ISD4002 Series ANA IN Modes, Figure 3. This capacitor value should be equal to the coupling capacitor used on the ANA IN+ pin. The input impedance at ANA IN is nominally 56 KΩ. In the single-ended mode, ANA IN– should be capacitively coupled to V_{SSA} through a capacitor equal to that used on the ANA IN+ input.

AUDIO OUTPUT (AUD OUT)

This pin provides the audio output to the user. It is capable of driving a 5 KΩ impedance. It is recommended that this pin be AC coupled.

NOTE *The AUD OUT pin is always at 1.2 volts when the device is powered up. When in playback, the output buffer connected to this pin can drive a load as small as 5 KΩ. When in record, a resistor connects AUD OUT to the internal 1.2 volt analog ground supply. This resistor is approximately 850 KΩ, but will vary somewhat according to the sample rate of the device. This relatively high impedance allows this pin to be connected to an audio bus without loading it down.*

SLAVE SELECT ($\overline{SS}$)

This input, when LOW, will select the ISD4002 device.

MASTER OUT SLAVE IN (MOSI)

This is the serial input to the ISD4002 device. The master microcontroller places data on the MOSI line one half-cycle before the rising clock edge to be clocked in by the ISD4002 device.

MASTER IN SLAVE OUT (MISO)

This is the serial output of the ISD4002 device. This output goes into a high-impedance state if the device is not selected.

SERIAL CLOCK (SCLK)

This is the clock input to the ISD4002. It is generated by the master device (microcontroller) and is used to synchronize data transfers in and out of the device through the MISO and MOSI lines. Data is latched into the ISD4002 on the rising edge of SCLK and shifted out of the device on the falling edge of SCLK.

INTERRUPT ($\overline{\text{INT}}$)

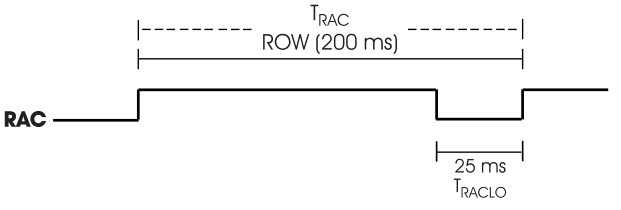
The ISD4002 interrupt pin goes LOW and stays LOW when an Overflow (OVF) or End of Message (EOM) marker is detected. This is an open drain output pin. Each operation that ends in an EOM or OVF will generate an interrupt including the message cueing cycles. The interrupt will be cleared the next time an SPI cycle is initiated. The interrupt status can be read by an RINT instruction.

Overflow Flag (OVF)—The Overflow flag indicates that the end of the ISD4002's analog memory has been reached during a record or playback operation.

End of Message (EOM)—The End-of-Message flag is set only during playback operation when an EOM is found. There are eight EOM flag position options per row.

ROW ADDRESS CLOCK (RAC)

This is an open drain output pin that provides a signal with a 200 ms period at the 8 KHz sampling frequency. (This represents a single row of memory and there are 600 rows of memory in the ISD4002 Series devices.) This signal stays HIGH for 175 ms and stays LOW for 25 ms when it reaches the end of a row.



The RAC pin stays HIGH for 218.75 μsec and stays LOW for 31.25 μsec in Message Cueing mode (see page 6 for a more detailed description of Message Cueing). Refer to the AC Parameters table for RAC timing information on other sample rate products.

When a record command is first initiated, the RAC pin remains HIGH for an extra T_{RACLO} period. This is due to the need to load sample and hold circuits internal to the device. This pin can be used for message management techniques.

EXTERNAL CLOCK INPUT (XCLK)

The external clock input for the ISD4002 products has an internal pull-down device. These products are configured at the factory with an internal sampling clock frequency centered to ± 1 percent of specification. The frequency is then maintained to a variation of ± 2.25 percent over the entire commercial temperature and operating voltage ranges. The internal clock has a –6/+4 percent tolerance, over the extended temperature, industrial temperature and voltage ranges. A regulated power supply is recommended for industrial temperature range parts. If greater precision is required, the device can be clocked through the XCLK pin in Table 1.

Table 1: External Clock Input Clocking Table

Part Number	Sample Rate	Required Clock
ISD4002-120	8.0 KHz	1024 KHz
ISD4002-150	6.4 KHz	819.2 KHz
ISD4002-180	5.3 KHz	682.7 KHz
ISD4002-240	4.0 KHz	512 KHz

These recommended clock rates should not be varied because the anti-aliasing and smoothing filters are fixed. Thus, aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two internally. ***If the XCLK is not used, this input should be connected to ground.***

AUTOMUTE™ FEATURE (AM CAP)

This pin is used in controlling the AutoMute feature. The AutoMute feature attenuates the signal when it drops below an internally set threshold. This helps to eliminate noise (with 6 dB of attenuation) when there is no signal (i.e., during periods of silence). A 1 μF capacitor to ground should be connected to the AM CAP pin. This capacitor becomes a part of an internal peak detector which senses the signal amplitude (peak). This peak level is compared to an internally set threshold to determine the AutoMute trip point. For large signals the AutoMute attenuation is set to 0 dB while 6 dB of attenuation occurs for silence. The 1 μF capacitor also affects the rate at which the AutoMute feature changes with the signal amplitude (or the attack time). The Automute feature can be disabled by connecting the AM CAP pin to V_{CCA}.

SERIAL PERIPHERAL INTERFACE (SPI) DESCRIPTION

The ISD4002 series operates from an SPI serial interface. The SPI interface operates with the following protocol.

The data transfer protocol assumes that the microcontroller's SPI shift registers are clocked on the falling edge of the SCLK. With the ISD4002, data is clocked in on the MOSI pin on the rising clock edge. Data is clocked out on the MISO pin on the falling clock edge.

1. All serial data transfers begin with the falling edge of $\overline{SS}$ pin.
2. $\overline{SS}$ is held LOW during all serial communications and held HIGH between instructions.
3. Data is clocked in on the rising clock edge and data is clocked out on the falling clock edge.
4. Play and record operations are initiated by enabling the device by asserting the $\overline{SS}$ pin LOW, shifting in an opcode and an address field to the ISD4002 device (refer to the Opcode Summary on the following page).
5. The opcodes and address fields are as follows: <5 control bits> and <11 address bits>.
6. Each operation that ends in an EOM or Overflow will generate an interrupt, including the Message Cueing cycles. The Interrupt will be cleared the next time an SPI cycle is initiated.
7. As Interrupt data is shifted out of the ISD4002 MISO pin, control and address data is simultaneously being shifted into the MOSI pin. Care should be taken such that the data shifted in is compatible with current system operation. It is possible to read interrupt data and start a new operation within the same SPI cycle.
8. An operation begins with the RUN bit set and ends with the RUN bit reset.
9. All operations begin with the rising edge of $\overline{SS}$.

MESSAGE CUEING

Message cueing allows the user to skip through messages, without knowing the actual physical location of the message. This operation is used during playback. In this mode, the messages are skipped 1600 times faster than in normal playback mode. It will stop when an EOM marker is reached. Then, the internal address counter will point to the next message.

Table 2: Opcode Summary

Instruction	Opcode <5 bits> Address <11 bits>	Operational Summary
POWERUP	00100 <XXXXXXXXXXX>	Power-Up: Device will be ready for an operation after T_{PUD}.
SETPLAY	11100 <0, A9–A0>	Initiates playback from address <A9–A0>.
PLAY	11110 <XXXXXXXXXXX>	Playback from the current address (until EOM or OVF).
SETREC	10100 <0, A9–A0>	Initiates a record operation from address <A9–A0>.
REC	10110 <XXXXXXXXXXX>	Records from current address until OVF is reached.
SETMC	11101 <0, A9–A0>	Initiates Message Cueing (MC) from address <A9–A0>.
MC(1)	11111 <XXXXXXXXXXX>	Performs a Message Cue. Proceeds to the end of the current message (EOM) or enters OVF condition if no more messages are present.
STOP	0X110 <XXXXXXXXXXX>	Stops current operation.
STOPPWRDN	0X01X <XXXXXXXXXXX>	Stops current Operation and enters stand-by (power-down) mode.
RINT(2)	0X110 <XXXXXXXXXXX>	Read Interrupt status bits: Overflow and EOM.

1. *Message Cueing can be selected only at the beginning of a play operation.*
2. *As the Interrupt data is shifted out of the ISD4002, control and address data is being shifted in. Care should be taken such that the data shifted in is compatible with current system operation. It is possible to read interrupt data and start a new operation at the same time. See Figure 6 through Figure 9 for Opcode format.*

POWER-UP SEQUENCE

The ISD4002 will be ready for an operation after T_{PUD} (approximately 25 ms for 8 KHz sample rate). The user needs to wait T_{PUD} before issuing an operational command. For example, to play from address 00 the following programing cycle should be used.

Playback Mode

1. Send POWERUP command.
2. Wait T_{PUD} (power-up delay).
3. Send SETPLAY command with address 00.
4. Send PLAY command.

The device will start playback at address 00 and it will generate an interrupt when an EOM is reached. It will then stop playback.

Record Mode

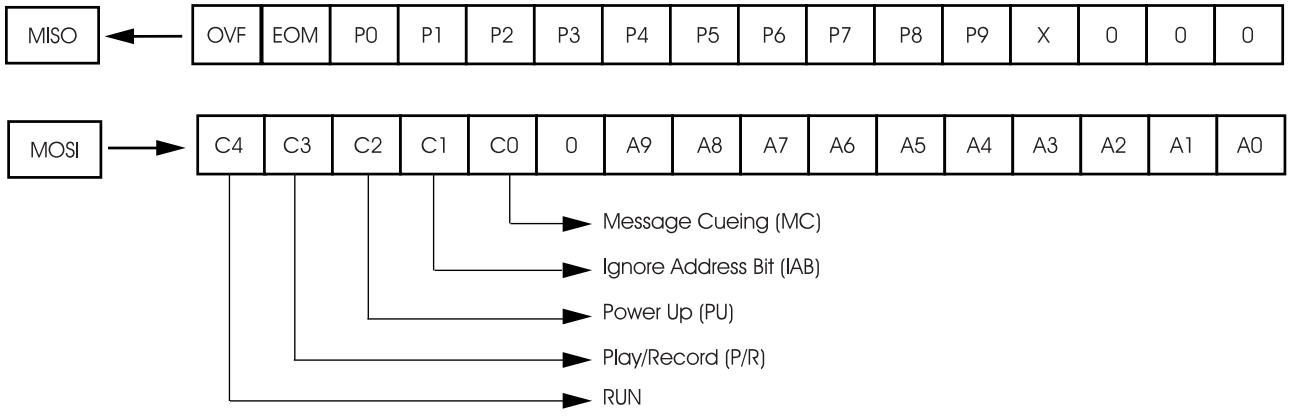
1. Send POWERUP command.
2. Wait T_{PUD} (power-up delay).
3. Send POWERUP command.
4. Wait 2 x T_{PUD} (power-up delay).
5. Send SETREC command with address 00.
6. Send REC command.

The device will start recording at address 00 and it will generate an interrupt when an overflow is reached (end of memory array). It will then stop recording.

SPI PORT

The following diagram describes the SPI port and the control bits associated with it.

Figure 4: SPI Port



SPI CONTROL REGISTER

The SPI control register provides control of individual device functions such as play, record, message cueing, power-up and power-down, start and stop operations, and ignore address pointers.

Table 3: SPI Control Register

Control Register	Bit	Device Function	Control Register	Bit	Device Function
RUN		Enable or Disable an operation	PU		Master power control
=	1	Start	=	1	Power-Up
=	0	Stop	=	0	Power-Down
P/$\overline{R}$		Selects play or record operation	IAB[1]		Ignore address control bit
=	1	Play	=	1	Ignore input address register (A9–A0)
=	0	Record	=	0	Use the input address register contents for an operation (A9–A0)
MC		Enable or Disable Message Cueing	P9–P0		Output of the row pointer register
=	1	Enable Message Cueing	A9–A0		Input address register
=	0	Disable Message Cueing			

1. *When IAB (Ignore Address Bit) is set to 0, a playback or record operation starts from address (A9–A0). For consecutive playback or record, IAB should be changed to a 1 before the end of that row (see RAC timing). Otherwise the ISD4002 will repeat the operation from the same row address. For memory management, the Row Address Clock (RAC) pin and IAB can be used to move around the memory segments.*

Figure 5: SPI Interface Simplified Block Diagram

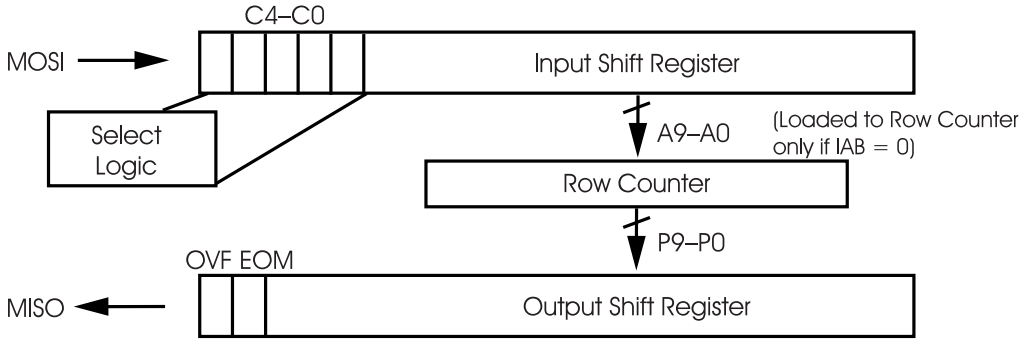


Table 4: Absolute Maximum Ratings (Packaged Parts)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pin	(V_{SS} – 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pin (Input current limited to ±20 mA)	(V_{SS} – 1.0 V) to (V_{CC} + 1.0 V)
Voltage applied to MOSI, SCLK, and $\overline{SS}$ pins (Input current limited to ±20 mA)	(V_{SS} – 1.0 V) to (V_{CC} + 1.0 V)
Lead temperature (soldering – 10 seconds)	300°C
V_{CC} – V_{SS}	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 5: Operating Conditions (Packaged Parts)

Condition	Value
Commercial operating temperature range[1]	0°C to +70°C
Extended operating temperature[1]	–20°C to +70°C
Industrial operating temperature[1]	–40°C to +85°C
Supply voltage (V_{CC})[2]	+2.7 V to +3.3 V
Ground voltage (V_{SS})[3]	0 V

1. *Case temperature.*
2. $V_{CC} = V_{CCA} = V_{CCD}$.
3. $V_{SS} = V_{SSA} = V_{SSD}$.

Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min(2)	Typ(1)	Max(2)	Units	Conditions
V_{IL}	Input Low Voltage			V_{CC} x 0.2	V	
V_{IH}	Input High Voltage	V_{CC} x 0.8			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 10 µA
V_{OL1}	RAC, $\overline{INT}$ Output Low Voltage			0.4	V	I_{OL} = 1 mA
V_{OH}	Output High Voltage	V_{CC} – 0.4			V	I_{OH} = –10 µA
I_{CC}	V_{CC} Current (Operating) — Playback — Record		 15 25	 30 40	 mA mA	 $R_{EXT} = \infty$ (3) $R_{EXT} = \infty$ (3)
I_{SB}	V_{CC} Current (Standby)		1	10	µA	(3) (4)
I_{IL}	Input Leakage Current			±1	µA	
I_{HZ}	MISO Tristate Current		1	10	µA	
R_{EXT}	Output Load Impedance	5			KΩ	
$R_{ANA\ IN+}$	ANA IN+ Input Resistance	2.2	3.0	3.8	KΩ	
$R_{ANA\ IN-}$	ANA IN– Input Resistance	40	56	71	KΩ	
A_{ARP}	ANA IN+ or ANA IN– to AUD OUT Gain		25		dB	(5)

1. *Typical values: T_A = 25°C and 3.0 V.*
2. *All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *V_{CCA} and V_{CCD} connected together.*
4. *$\overline{SS}$ = V_{CCA} = V_{CCD}, XCLK = MOSI = V_{SSA}= V_{SSD} and all other pins floating.*
5. *Measured with AutoMute feature disabled.*

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min(2)	Typ(1)	Max(2)	Units	Conditions
F_S	Sampling Frequency	ISD4002-120		8.0		KHz	(5)
		ISD4002-150		6.4		KHz	(5)
		ISD4002-180		5.3		KHz	(5)
		ISD4002-240		4.0		KHz	(5)
F_{CF}	Filter Pass Band	ISD4002-120		3.4		KHz	3-dB Roll-Off Point(3) (7)
		ISD4002-150		2.7		KHz	3-dB Roll-Off Point(3) (7)
		ISD4002-180		2.3		KHz	3-dB Roll-Off Point(3) (7)
		ISD4002-240		1.7		KHz	3-dB Roll-Off Point(3) (7)
T_{REC}	Record Duration	ISD4002-120		120		sec	(6)
		ISD4002-150		150		sec	(6)
		ISD4002-180		180		sec	(6)
		ISD4002-240		240		sec	(6)

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min(2)	Typ(1)	Max(2)	Units	Conditions
T_{PLAY}	Playback Duration	ISD4002-120		120		sec	(6)
		ISD4002-150		150		sec	(6)
		ISD4002-180		180		sec	(6)
		ISD4002-240		240		sec	(6)
T_{PUD}	Power-Up Delay	ISD4002-120		25		msec	
		ISD4002-150		31.25		msec	
		ISD4002-180		37.5		msec	
		ISD4002-240		50		msec	
T_{STOP} or T_{PAUSE}	Stop or Pause in Record or Play	ISD4002-120		50		msec	
		ISD4002-150		62.5		msec	
		ISD4002-180		75		msec	
		ISD4002-240		100		msec	
T_{RAC}	RAC Clock Period	ISD4002-120		200		msec	(10)
		ISD4002-150		250		msec	(10)
		ISD4002-180		300		msec	(10)
		ISD4002-240		400		msec	(10)
T_{RACLO}	RAC Clock Low Time	ISD4002-120		25		msec	
		ISD4002-150		31.25		msec	
		ISD4002-180		37.5		msec	
		ISD4002-240		50		msec	
T_{RACM}	RAC Clock Period in Message Cueing Mode	ISD4002-120		125		µsec	
		ISD4002-150		156.3		µsec	
		ISD4002-180		187.5		µsec	
		ISD4002-240		250		µsec	
T_{RACML}	RAC Clock Low Time in Message Cueing Mode	ISD4002-120		15.63		µsec	
		ISD4002-150		19.53		µsec	
		ISD4002-180		23.44		µsec	
		ISD4002-240		31.25		µsec	
THD	Total Harmonic Distortion			1	2	%	@ 1 KHz
V_{IN}	ANA IN Input Voltage				32	mV	Peak-to-Peak(4) (8) (9)

1. *Typical values: T_A = 25°C and 3.0 V.*
2. *All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cut off depends upon the value of external capacitors (see Pin Descriptions).*
4. *Single-ended input mode. In the differential input mode, V_{IN} maximum for ANA IN+ and ANA IN– is 16 mVp-p.*
5. *Sampling Frequency can vary as much as ±2.25 percent over the commercial temperature, and voltage ranges, and –6/+4 percent over the extended temperature, industrial temperature and voltage ranges. For greater stability, an external clock can be utilized (see Pin Descriptions).*
6. *Playback and Record Duration can vary as much as ±2.25 percent over the commercial temperature and voltage ranges, and –4/+6 percent over the extended temperature, industrial temperature and voltage ranges. For greater stability, an external clock can be utilized (see Pin Descriptions).*
7. *Filter specification applies to the anti-aliasing filter and the smoothing filter. Therefore, from input to output, expect a 6dB drop by nature of passing through both filters.*
8. *The typical output voltage will be approximately 570 mVp-p with V_{IN} at 32 mVp-p.*
9. *For optimal signal quality, this maximum limit is recommended.*
10. *When a record command is sent, $T_{RAC} = T_{RAC} + T_{RACLO}$ on the first row addressed.*

Table 8: Absolute Maximum Ratings (Die)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pad	(V_{SS} – 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pad (Input current limited to ±20 mA)	(V_{SS} – 1.0 V) to (V_{CC} + 1.0 V)
Voltage applied to MOSI, SCLK, and $\overline{SS}$ pins (Input current limited to ±20 mA)	(V_{SS} – 1.0 V) to (V_{CC} + 1.0 V)
V_{CC} – V_{SS}	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 9: Operating Conditions (Die)

Condition	Value
Commercial operating temperature range	0°C to +50°C
Supply voltage (V_{CC})[1]	+2.7 V to +3.3 V
Ground voltage (V_{SS})[2]	0 V

1. $V_{CC} = V_{CCA} = V_{CCD}$
2. $V_{SS} = V_{SSA} = V_{SSD}$.

Table 10: DC Parameters (Die)

Symbol	Parameters	Min[2]	Typ[1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			V_{CC} x 0.2	V	
V_{IH}	Input High Voltage	V_{CC} x 0.8			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 10 µA
V_{OL1}	RAC, $\overline{INT}$ Output Low Voltage			0.4	V	I_{OL} = 1 mA
V_{OH}	Output High Voltage	V_{CC} – 0.4			V	I_{OH} = –10 µA
I_{CC}	V_{CC} Current (Operating) — Playback — Record		 15 25	 30 40	 mA mA	 $R_{EXT} = \infty$ [3] $R_{EXT} = \infty$ [3]
I_{SB}	V_{CC} Current (Standby)		1	10	µA	[3] [4]
I_{IL}	Input Leakage Current			±1	µA	
I_{HZ}	MISO Tristate Current		1	10	µA	
R_{EXT}	Output Load Impedance	5			KΩ	

Table 10: DC Parameters (Die)

Symbol	Parameters	Min(2)	Typ(1)	Max(2)	Units	Conditions
$R_{ANA\ IN+}$	ANA IN+ Input Resistance	2.2	3.0	3.8	KΩ	
$R_{ANA\ IN-}$	ANA IN– Input Resistance	40	56	71	KΩ	
A_{ARP}	ANA IN+ or ANA IN– to AUDOUT Gain		25		dB	(5)

1. *Typical values: T_A = 25°C and 3.0 V.*
2. *All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *V_{CCA} and V_{CCD} connected together.*
4. *$\overline{SS}$ = V_{CCA}= V_{CCD}, XCLK = MOSI = V_{SSA} = V_{SSD} and all other pins floating.*
5. *Measured with AutoMute feature disabled.*

Table 11: AC Parameters (Die)

Symbol	Characteristic		Min(2)	Typ(1)	Max(2)	Units	Conditions
F_S	Sampling Frequency	ISD4002-120		8.0		KHz	(5)
		ISD4002-150		6.4		KHz	(5)
		ISD4002-180		5.3		KHz	(5)
		ISD4002-240		4.0		KHz	(5)
F_{CF}	Filter Pass Band	ISD4002-120		3.4		KHz	3dB Roll-Off Point (3) (6)
		ISD4002-150		2.7		KHz	3dB Roll-Off Point (3) (6)
		ISD4002-180		2.3		KHz	3dB Roll-Off Point (3) (6)
		ISD4002-240		1.7		KHz	3dB Roll-Off Point (3) (6)
T_{REC}	Record Duration	ISD4002-120		120		sec	(5)
		ISD4002-150		150		sec	(5)
		ISD4002-180		180		sec	(5)
		ISD4002-240		240		sec	(5)
T_{PLAY}	Playback Duration	ISD4002-120		120		sec	(5)
		ISD4002-150		150		sec	(5)
		ISD4002-180		180		sec	(5)
		ISD4002-240		240		sec	(5)
T_{PUD}	Power-Up Delay	ISD4002-120		25		msec	
		ISD4002-150		31.25		msec	
		ISD4002-180		37.5		msec	
		ISD4002-240		50		msec	
T_{STOP} or T_{PAUSE}	Stop or Pause in Record or Play	ISD4002-120		50		msec	
		ISD4002-150		62.5		msec	
		ISD4002-180		75		msec	
		ISD4002-240		100		msec	

Table 11: AC Parameters (Die)

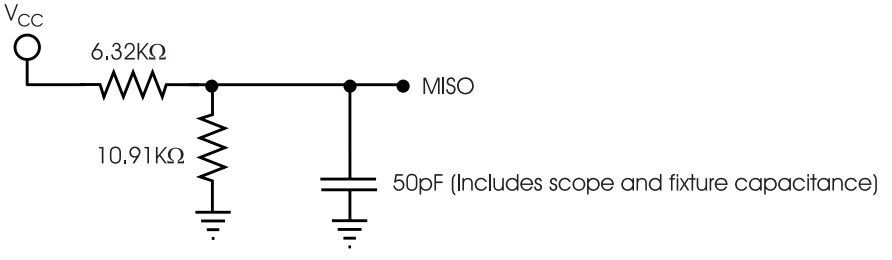
Symbol	Characteristic		Min(2)	Typ(1)	Max(2)	Units	Conditions
T_{RAC}	RAC Clock Period	ISD4002-120		200		msec	
		ISD4002-150		250		msec	
		ISD4002-180		300		msec	
		ISD4002-240		400		msec	
T_{RACLO}	RAC Clock Low Time	ISD4002-120		25		msec	(9)
		ISD4002-150		31.25		msec	(9)
		ISD4002-180		37.5		msec	(9)
		ISD4002-240		50		msec	(9)
T_{RACM}	RAC Clock Period in Message Cueing Mode	ISD4002-120		125		µsec	
		ISD4002-150		156.3		µsec	
		ISD4002-180		187.5		µsec	
		ISD4002-240		250		µsec	
T_{RACML}	RAC Clock Low Time in Message Cueing Mode	ISD4002-120		15.63		µsec	
		ISD4002-150		19.53		µsec	
		ISD4002-180		23.44		µsec	
		ISD4002-240		31.25		µsec	
THD	Total Harmonic Distortion			1	2	%	@ 1 KHz
V_{IN}	ANA IN Input Voltage				32	mV	Peak-to-Peak(4) (7) (8)

1. *Typical values: T_A = 25°C and 3.0 V.*
2. *All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cut off depends upon the value of external capacitors (see Pin Descriptions).*
4. *Single-ended input mode. In the differential input mode, V_{IN} maximum for ANA IN+ and ANA IN– is 16 mV peak-to-peak.*
5. *Sampling Frequency and Duration can vary as much as ±2.25 percent over the commercial temperature and voltage ranges. For greater stability, an external clock can be utilized (see Pin Descriptions).*
6. *Filter specification applies to the anti-aliasing filter and to the smoothing filter.*
7. *The typical output voltage will be approximately 570 mV peak-to-peak with V_{IN} at 32 mV peak-to-peak.*
8. *For optimal signal quality, this maximum limit is recommended.*
9. *When a record command is sent, $T_{RAC} = T_{RAC} + T_{RACLO}$ on the first row addressed.*

Table 12: SPI AC Parameters(1)

Symbol	Characteristics	Min	Max	Units	Conditions
T_{SSS}	$\overline{SS}$ Setup Time	500		nsec	
T_{SSH}	$\overline{SS}$ Hold Time	500		nsec	
T_{DIS}	Data in Setup Time	200		nsec	
T_{DIH}	Data in Hold Time	200		nsec	
T_{PD}	Output Delay		500	nsec	
T_{DF}(2)	Output Delay to hiZ		500	nsec	
T_{SSmin}	$\overline{SS}$ HIGH	1		µsec	
T_{SCKhi}	SCLK High Time	400		nsec	
T_{SCKlow}	SCLK Low Time	400		nsec	
F_0	CLK Frequency		1,000	KHz	

1. *Typical values: T_A= 25°C and 3.0 V. Timing measured at 50 percent of the V_{CC} level.*
2. *Tristate test condition.*



TIMING DIAGRAMS

Figure 6: Timing Diagram

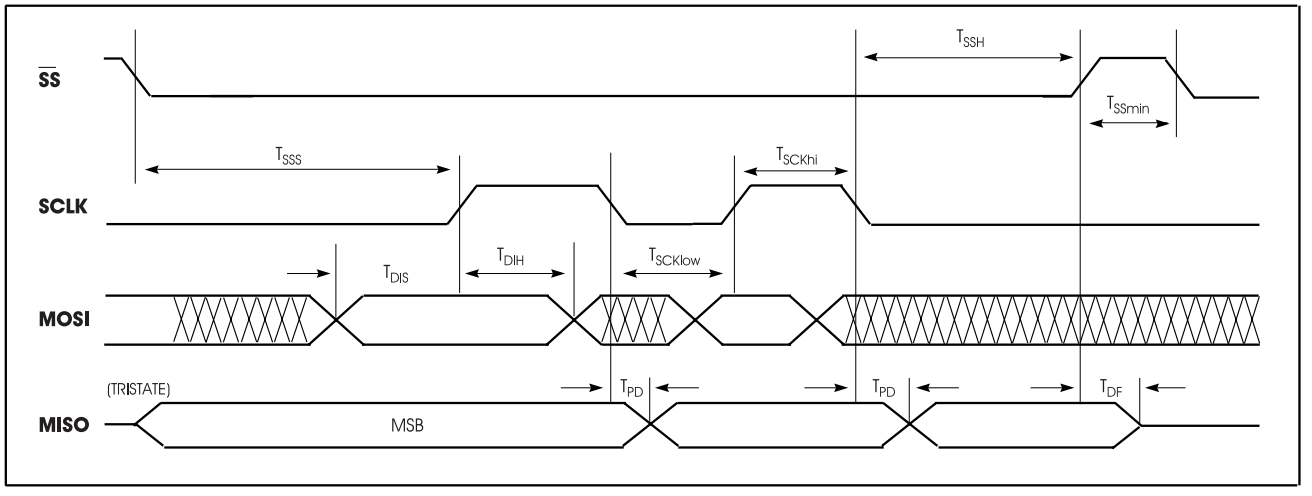


Figure 7: 8-Bit Command Format

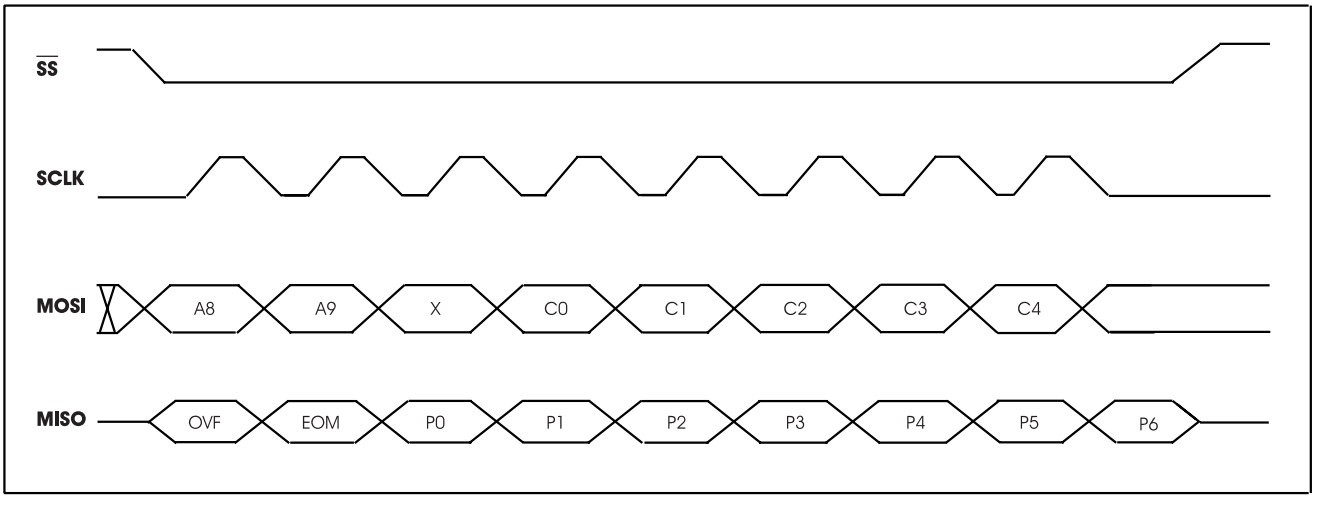


Figure 8: 16-Bit Command Format

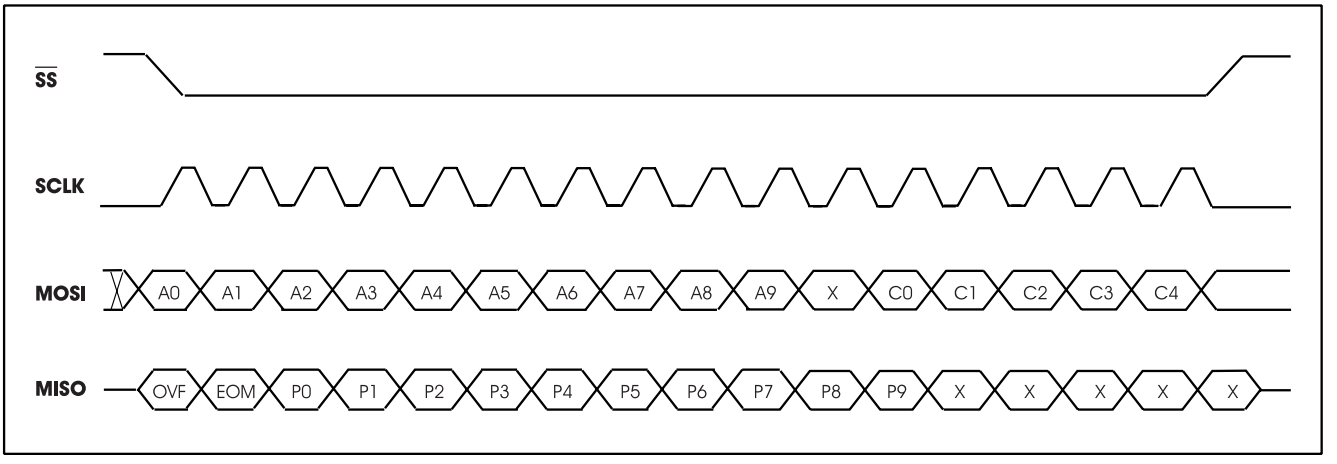


Figure 9: Playback/Record and Stop Cycle

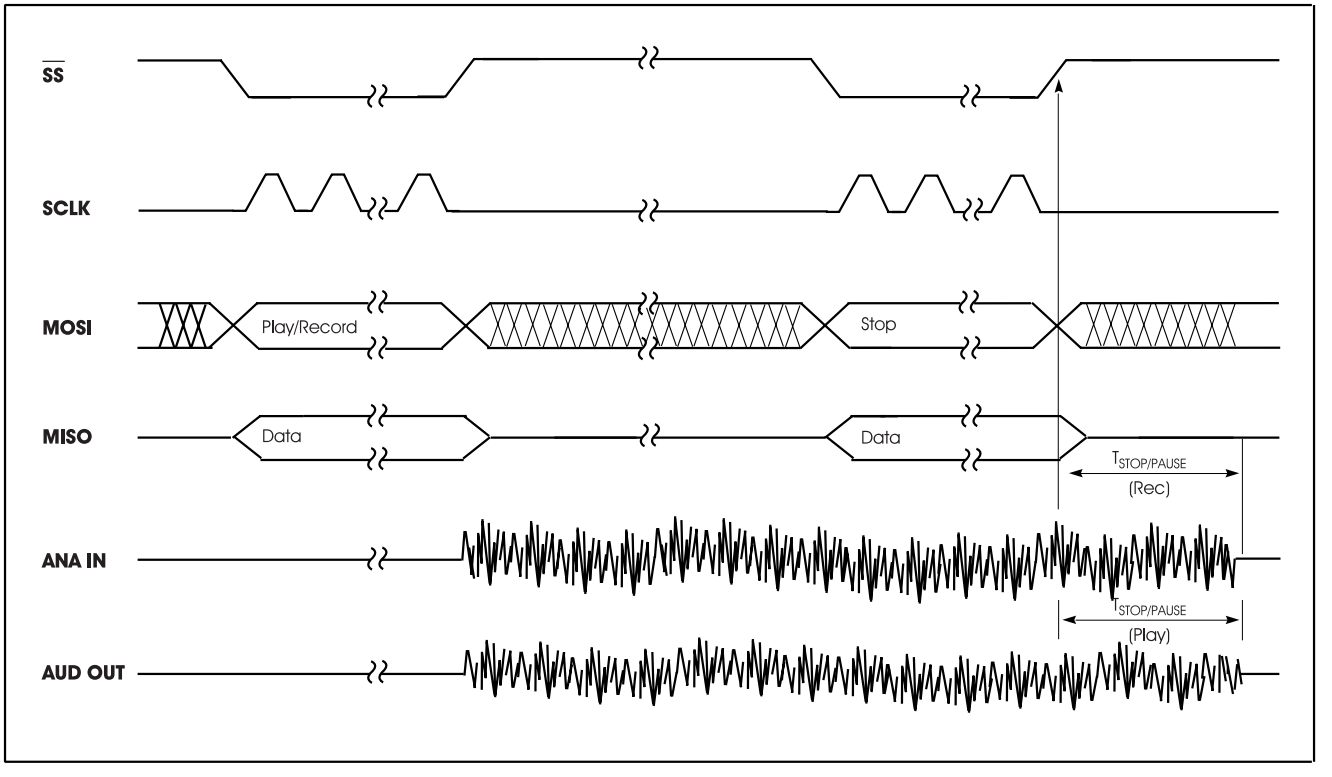
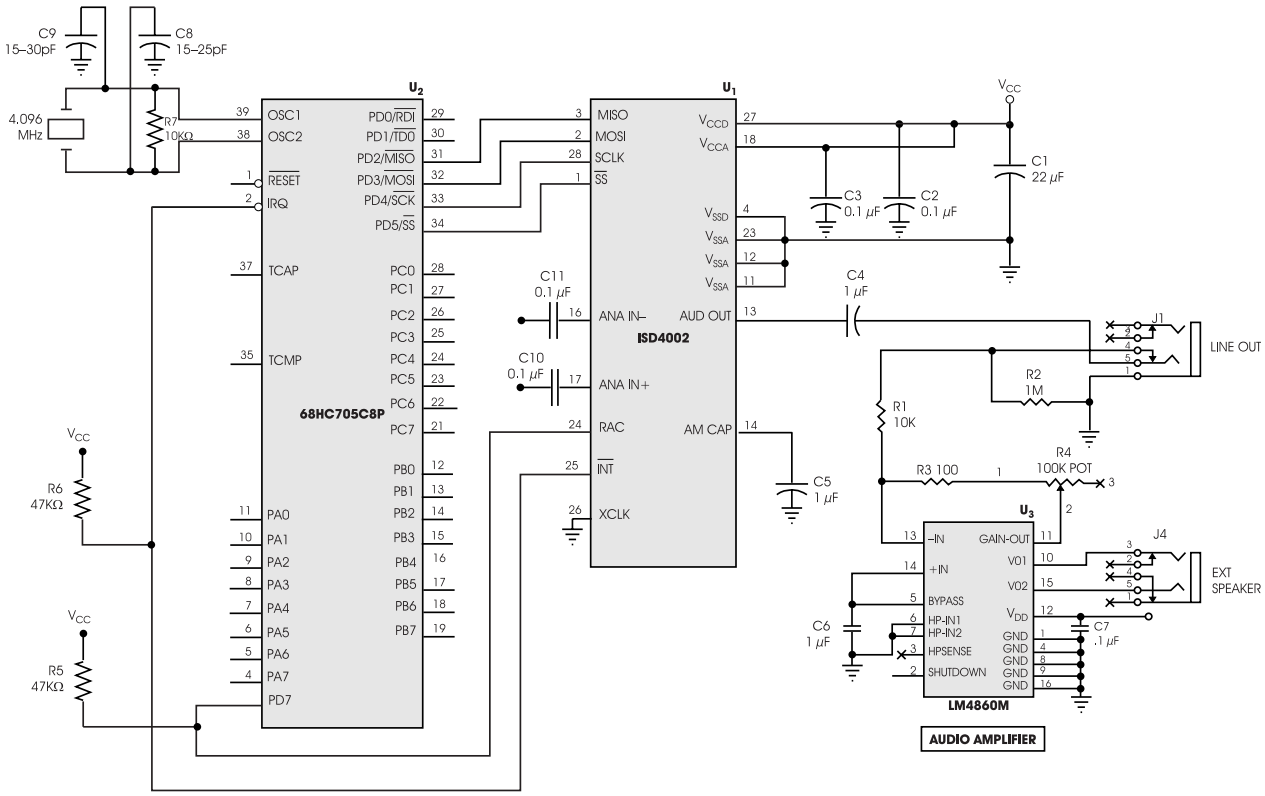
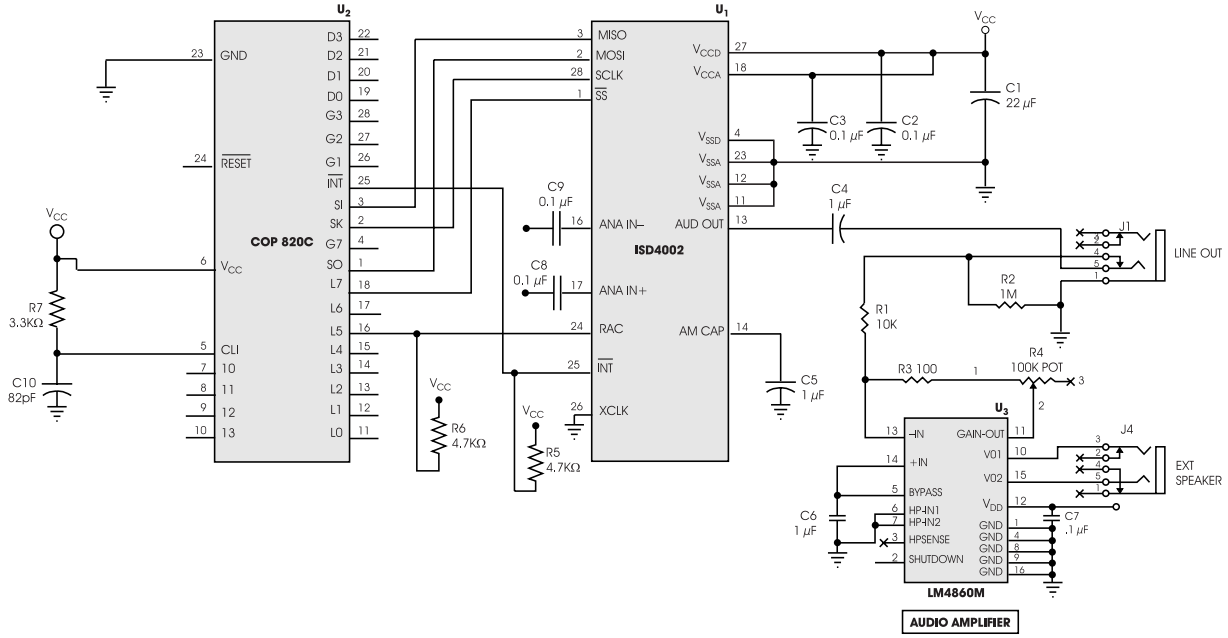


Figure 10: Application Example Using SPI(1)



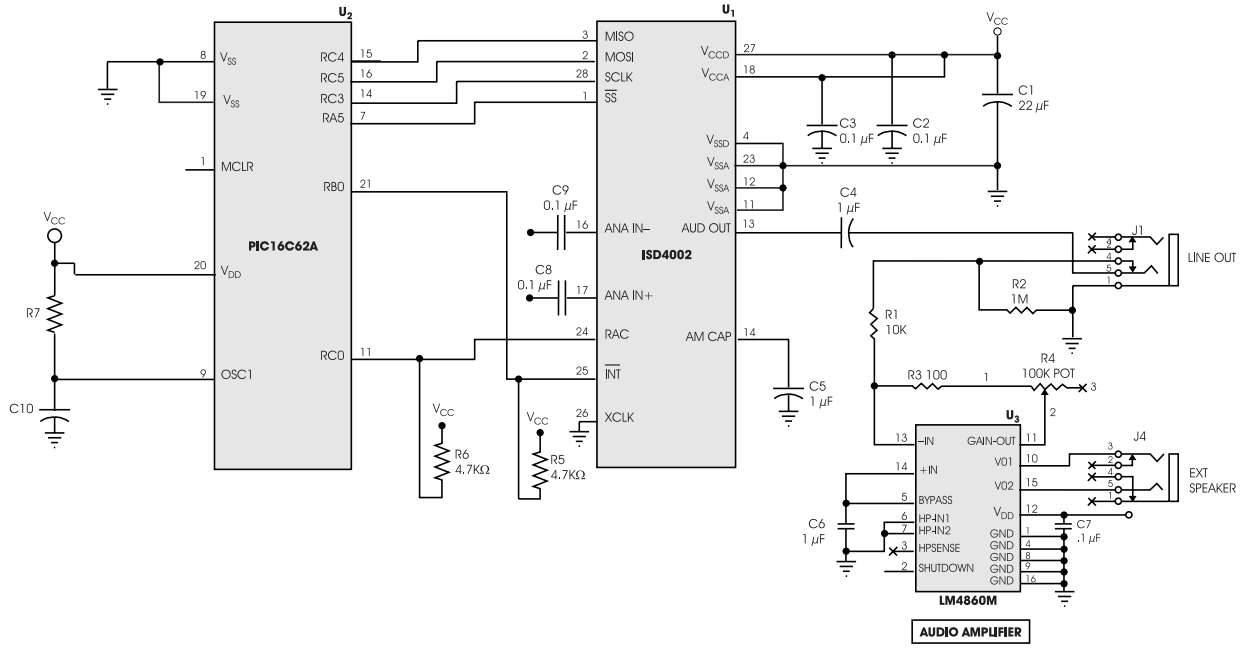
1. *This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.*
2. *Please make sure the bypass capacitor, C2 is as close as possible to the package.*

Figure 11: Application Example Using Microwire(1)



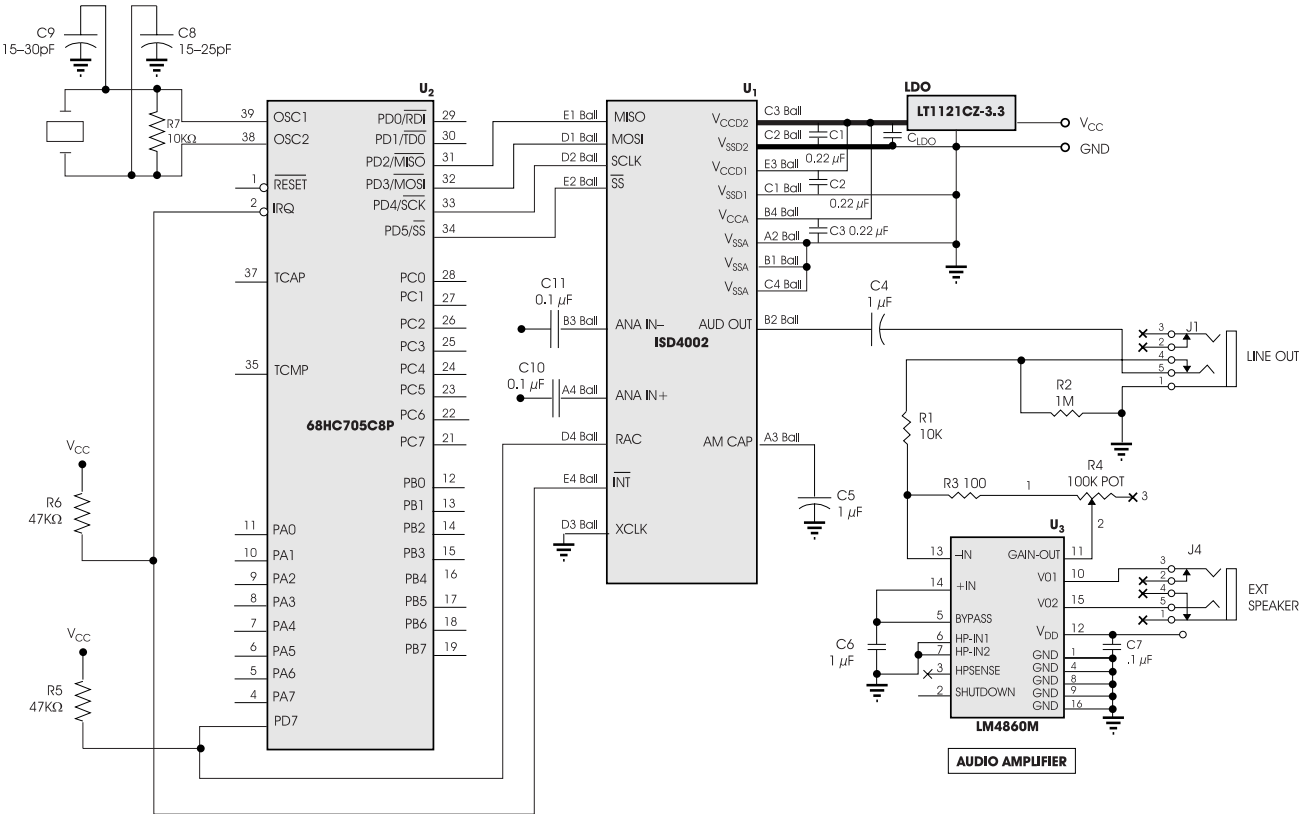
1. *This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.*
2. *Please make sure the bypass capacitor, C2 is as close as possible to the package.*

Figure 12: Application Example Using SPI Port on Microcontroller(1)



1. *This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.*
2. *Please make sure the bypass capacitor, C2 is as close as possible to the package.*

Figure 13: Application Example Using SPI with a Chip Scale Packaged Device



1. *This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.*
2. *Please make sure all bypass capacitors are as close as possible to the package.*
3. *Ground plane must be used to connect all V_{SSA} pins together. If a ground plane is not available then a short and low impedance path is necessary.*
4. *Route ANA IN+ and ANA IN– away from V_{CCD} and V_{SSD} return paths.*
5. *Biasing for electret microphone must come from V_{CCA} and V_{SSA}.*
6. *AM CAP must return to V_{SSA}.*
7. *Traces from V_{CCD2} to the LDO (Low Dropout regulator) and from V_{SSD2} to the LDO ground should be as thick as possible. The distance between these two traces should be as short as possible.*

DEVICE PHYSICAL DIMENSIONS

Figure 14: 28-Lead 8x13.4 mm Plastic Thin Small Outline Package (TSOP) Type I (E)

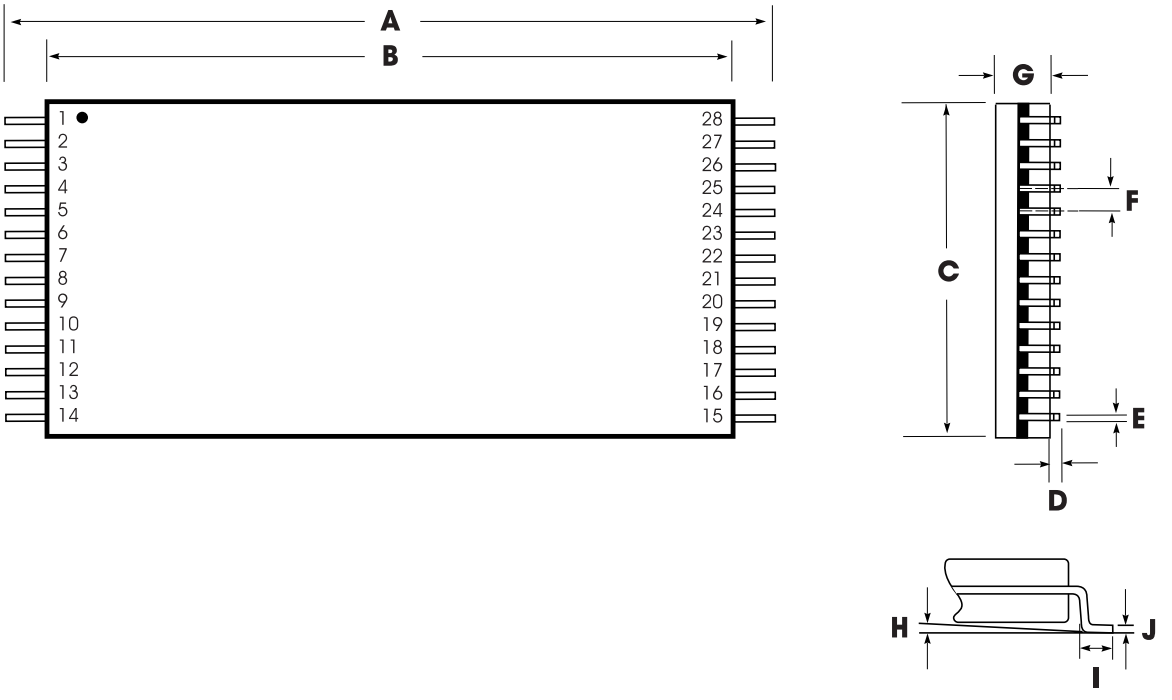


Table 13: Plastic Thin Small Outline Package (TSOP) Type I (E) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.520	0.528	0.535	13.20	13.40	13.60
B	0.461	0.465	0.469	11.70	11.80	11.90
C	0.311	0.315	0.319	7.90	8.00	8.10
D	0.002		0.006	0.05		0.15
E	0.007	0.009	0.011	0.17	0.22	0.27
F		0.0217			0.55	
G	0.037	0.039	0.041	0.95	1.00	1.05
H	0°	3°	6°	0°	3°	6°
I	0.020	0.022	0.028	0.50	0.55	0.70
J	0.004		0.008	0.10		0.21

NOTE: *Lead coplanarity to be within 0.004 inches.*

Figure 15: 28-Lead 0.600-Inch Plastic Dual Inline Package (PDIP) (P)

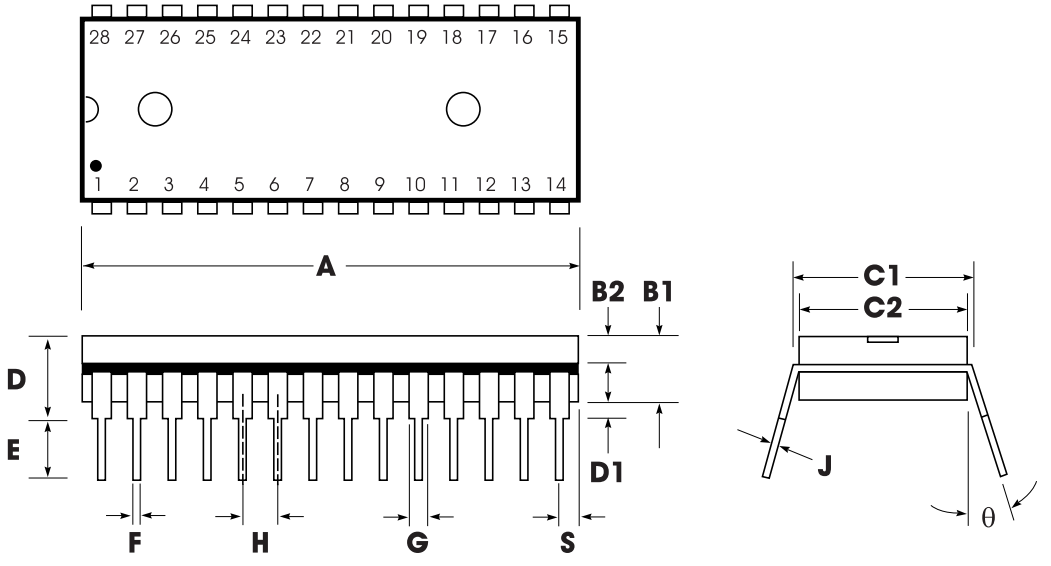


Table 14: Plastic Dual Inline Package (PDIP) (P) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.65
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
q	0°		15°	0°		15°

Figure 16: 28-Lead 0.300-Inch Plastic Small Outline Integrated Circuit (SOIC) (S)

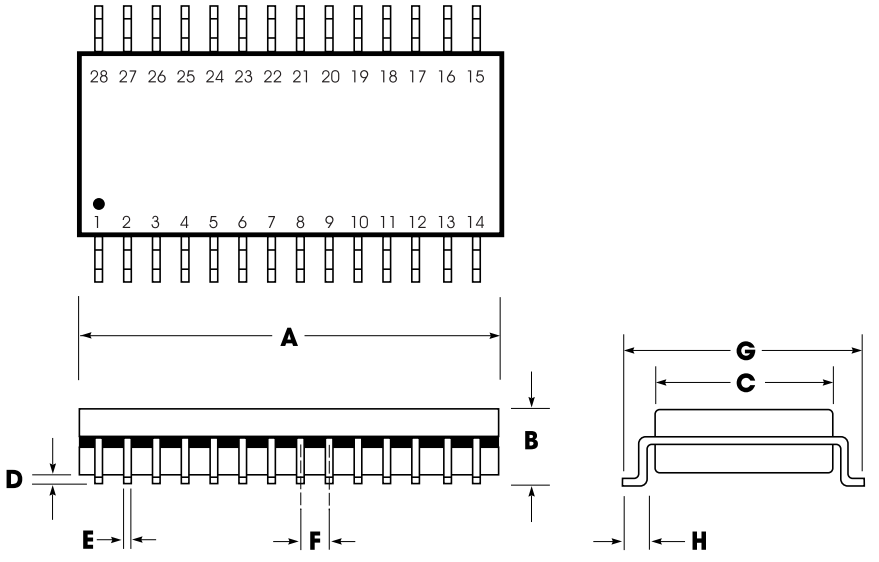


Table 15: Plastic Small Outline Integrated Circuit (SOIC) (S) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.701	0.706	0.711	17.81	17.93	18.06
B	0.097	0.101	0.104	2.46	2.56	2.64
C	0.292	0.296	0.299	7.42	7.52	7.59
D	0.005	0.009	0.0115	0.127	0.22	0.29
E	0.014	0.016	0.019	0.35	0.41	0.48
F		0.050			1.27	
G	0.400	0.406	0.410	10.16	10.31	10.41
H	0.024	0.032	0.040	0.61	0.81	1.02

NOTE: *Lead coplanarity to be within 0.004 inches.*

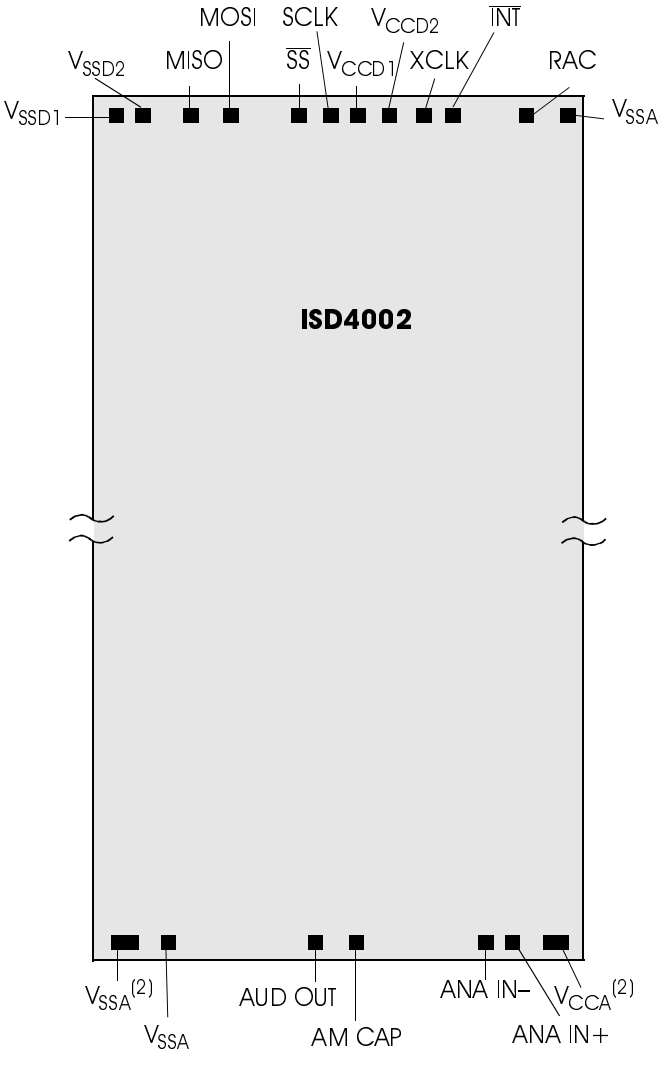
Figure 17: ISD4002 Series Bonding Physical Layout(1) (Unpackaged Die)

ISD4002 Series

I. Die Dimensions
X: 166.6 ±1 mils
Y: 222.5 ±1 mils

II. Die Thickness
11.5 ±0.5 mils(3)

III. Pad Opening (min)
90 x 90 microns
3.5 x 3.5 mils



1. *The backside of die is internally connected to V_{SS}. It **MUST NOT** be connected to any other potential or damage may occur.*
2. *Double bond recommended.*
3. *This is the current die thickness. Please contact ISD as this thickness may change in the future.*

Table 16: ISD4002 Series Device Pin/Pad Designations, with Respect to Die Center (µm)

Pin	Pin Name	X Axis	Y Axis
V_{SSA}[1]	V_{SS} Analog Power Supply	–1898.1	–2607.4
V_{SSA}	V_{SS} Analog Power Supply	–1599.9	–2607.4
AUD OUT	Audio Output	281.9	–2607.4
AM CAP	AutoMute	577.3	–2607.4
ANA IN –	Inverting Analog Input	1449.3	–2607.4
ANA IN +	Noninverting Analog Input	1603.5	–2607.4
V_{CCA}[1]	V_{CC} Analog Power Supply	1898.7	–2607.4
V_{SSA}	V_{SS} Analog Power Supply	1885.7	2606.7
RAC	Row Address Clock	1483.8	2606.7
$\overline{INT}$	Interrupt	794.8	2606.7
XCLK	External Clock Input	564.8	2606.7
V_{CCD1}	V_{CC} Digital Power Supply	384.9	2606.7
V_{CCD2}	V_{CC} Digital Power Supply	169.5	2606.7
SCLK	Slave Clock	–14.7	2606.7
$\overline{SS}$	Slave Select	–198.1	2606.7
MOSI	Master Out Slave In	–1063.7	2606.7
MISO	Master In Slave Out	–1325.6	2606.7
V_{SSD1}	V_{SS} Digital Power Supply	–1665.3	2606.7
V_{SSD2}	V_{SS} Digital Power Supply	–1836.9	2606.7

1. *Double bond recommended.*

Figure 18: ISD4002 Chip Scale Package (CSP) (Z)

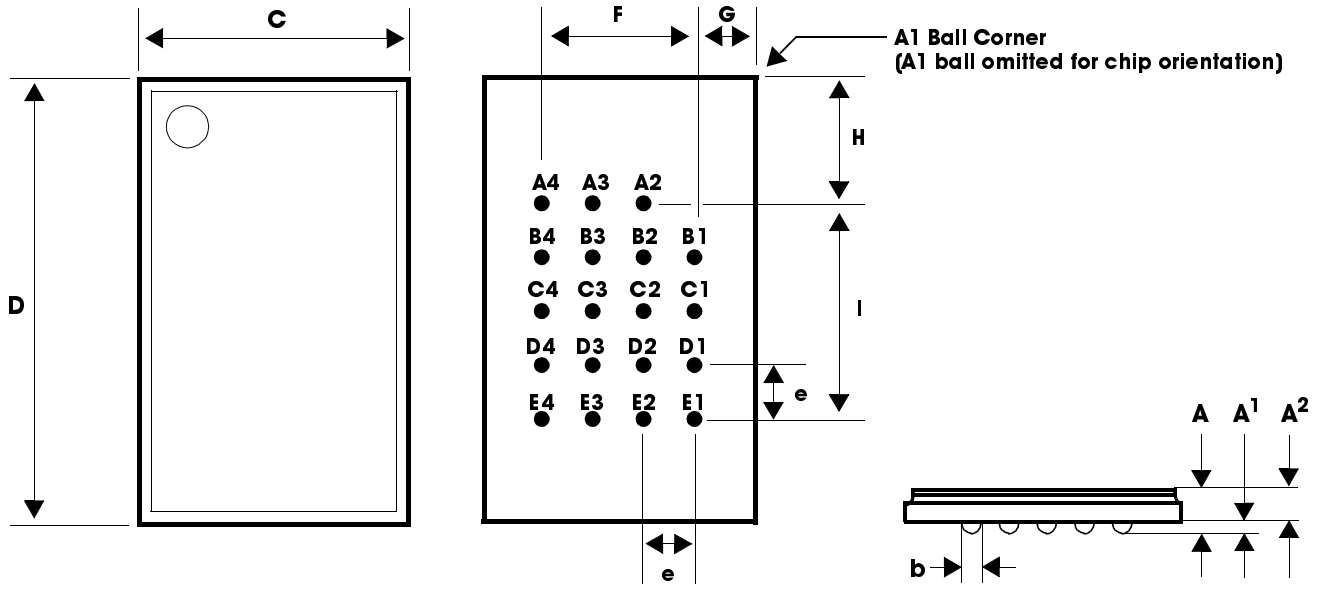


Table 17: CSP Dimensions

Symbol	Min.	Nom.	Max.
A	—	—	0.85
A^1	0.15	—	—
A^2	—	0.55	—
b	0.30	0.35	0.40
C	—	4.70	—
D	—	6.10	—
e		0.75	
F	—	2.25	—
G	—	1.22	—
H	—	1.55	—
I	—	3.00	—

Name	Ball Location	TSOP Pin #
V_{SSA}	A2	18
AM CAP	A3	22
ANAIN+	A4	25
V_{SSA}	B1	17
AUDOUT	B2	20
ANAIN–	B3	24
V_{CCA}	B4	26
V_{SSD1}	C1	12
V_{SSD2}	C2	N/A
V_{CCD2}	C3	N/A
V_{SSA}	C4	1
MOSI	D1	10
SCLK	D2	8
XCLK	D3	6
RAC	D4	2
MISO	E1	11
SS	E2	9
V_{CCD1}	E3	7
INT	E4	5

ORDERING INFORMATION

Product Number Descriptor Key

ISD4002– _ _ _ _ _

Product Family
ISD4000 Family

Product Series
02 = Second Series (2–4 min))

Duration:
120 = 120 seconds
150 = 150 seconds
180 = 180 seconds
240 = 240 seconds

Special Temperature Field:
Blank = Commercial Packaged (0°C to +70°C)
or Commercial Die (0°C to +50°C)
D = Extended (–20°C to +70°C)
I = Industrial (–40°C to +85°C)

Package Type:
E = 28-Lead 8x13.4mm Plastic Thin Small Outline Package (TSOP) Type 1
P = 28-Lead 0.600-Inch Plastic Dual Inline Package (PDIP)
S = 28-Lead 0.300-Inch Plastic Small Outline Package (SOIC)
X = Die
Z = Chip Scale Package (CSP)

When ordering ISD4002 Series devices, please refer to the following valid part numbers.

Part Number	Part Number	Part Number	Part Number
ISD4002-120E	ISD4002-150E	ISD4002-180E	ISD4002-240E
ISD4002-120ED	ISD4002-150ED	ISD4002-180ED	ISD4002-240ED
ISD4002-120EI	ISD4002-150EI	ISD4002-180EI	ISD4002-240EI
ISD4002-120P	ISD4002-150P	ISD4002-180P	ISD4002-240P
ISD4002-120S	ISD4002-150S	ISD4002-180S	ISD4002-240S
ISD4002-120SI	ISD4002-150SI	ISD4002-180SI	ISD4002-240SI
ISD4002-120X	ISD4002-150X	ISD4002-180X	ISD4002-240X
ISD4002-120Z	ISD4002-150Z	ISD4002-180Z	ISD4002-240Z
ISD4002-120ZD	ISD4002-150ZD	ISD4002-180ZD	ISD4002-240ZD
ISD4002-120ZI	ISD4002-150ZI	ISD4002-180ZI	ISD4002-240ZI

For the latest product information, access ISD's worldwide website at http://www.isd.com.