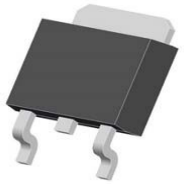
KERSEMI ELECTRONIC CO.,LTD.

# IRFR24N15D
# IRFU24N15D

D-Pak
IRFR24N15D



I-Pak
IRFU24N15D

## Applications

- High frequency DC-DC converters

## Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective $C_{OSS}$ to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current

| $V_{DSS}$ | $R_{DS(on)}$ max | $I_D$ |
|---|---|---|
| **150V** | **95mΩ** | **24A** |

## Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V | 24 | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V | 17 | |
| $I_{DM}$ | Pulsed Drain Current ① | 96 | |
| $P_D$ @$T_C$ = 25°C | Power Dissipation | 140 | W |
| | Linear Derating Factor | 0.92 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 30 | V |
| dv/dt | Peak Diode Recovery dv/dt ③ | 4.9 | V/ns |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to + 175 | °C |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case ) | |

## Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case | —— | 1.1 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB mount)* | —— | 50 | |
| $R_{\theta JA}$ | Junction-to-Ambient | —— | 110 | |

## Static @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 150 | —— | —— | V | $V_{GS}$ = 0V, $I_D$ = 250μA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | —— | 0.18 | —— | V/°C | Reference to 25°C, $I_D$ = 1mA ⑥ |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | —— | 82 | 95 | mΩ | $V_{GS}$ = 10V, $I_D$ = 14A ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 3.0 | —— | 5.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250μA |
| $I_{DSS}$ | Drain-to-Source Leakage Current | —— | —— | 25 | μA | $V_{DS}$ = 150V, $V_{GS}$ = 0V |
| | | —— | —— | 250 | | $V_{DS}$ = 120V, $V_{GS}$ = 0V, $T_J$ = 150°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | —— | —— | 100 | nA | $V_{GS}$ = 30V |
| | Gate-to-Source Reverse Leakage | —— | —— | -100 | | $V_{GS}$ = -30V |

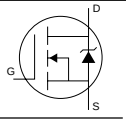
## Dynamic @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $g_{fs}$ | Forward Transconductance | 8.2 | —— | —— | S | $V_{DS}$ = 25V, $I_D$ = 14A |
| $Q_g$ | Total Gate Charge | —— | 30 | 45 | nC | $I_D$ = 14A |
| $Q_{gs}$ | Gate-to-Source Charge | —— | 7.4 | 11 | | $V_{DS}$ = 120V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | —— | 17 | 26 | | $V_{GS}$ = 10V, ④ |
| $t_{d(on)}$ | Turn-On Delay Time | —— | 11 | —— | ns | $V_{DD}$ = 75V |
| $t_r$ | Rise Time | —— | 53 | —— | | $I_D$ = 14A |
| $t_{d(off)}$ | Turn-Off Delay Time | —— | 19 | —— | | $R_G$ = 6.8Ω |
| $t_f$ | Fall Time | —— | 15 | —— | | $V_{GS}$ = 10V ④ |
| $C_{iss}$ | Input Capacitance | —— | 890 | —— | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | —— | 220 | —— | | $V_{DS}$ = 25V |
| $C_{rss}$ | Reverse Transfer Capacitance | —— | 46 | —— | | $f$ = 1.0MHz |
| $C_{oss}$ | Output Capacitance | —— | 1460 | —— | | $V_{GS}$ = 0V, $V_{DS}$ = 1.0V, $f$ = 1.0MHz |
| $C_{oss}$ | Output Capacitance | —— | 95 | —— | | $V_{GS}$ = 0V, $V_{DS}$ = 120V, $f$ = 1.0MHz |
| $C_{oss}$ eff. | Effective Output Capacitance | —— | 200 | —— | | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 120V ⑤ |

## Avalanche Characteristics

| | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $E_{AS}$ | Single Pulse Avalanche Energy② | —— | 170 | mJ |
| $I_{AR}$ | Avalanche Current① | —— | 14 | A |
| $E_{AR}$ | Repetitive Avalanche Energy① | —— | 14 | mJ |

## Diode Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | —— | —— | 24 | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ① | —— | —— | 96 | | |
| $V_{SD}$ | Diode Forward Voltage | —— | —— | 1.5 | V | $T_J$ = 25°C, $I_S$ = 14A, $V_{GS}$ = 0V ④ |
| $t_{rr}$ | Reverse Recovery Time | —— | 110 | —— | ns | $T_J$ = 25°C, $I_F$ = 14A |
| $Q_{rr}$ | Reverse RecoveryCharge | —— | 450 | —— | nC | di/dt = 100A/μs ④ |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$+$L_D$) | | | | |

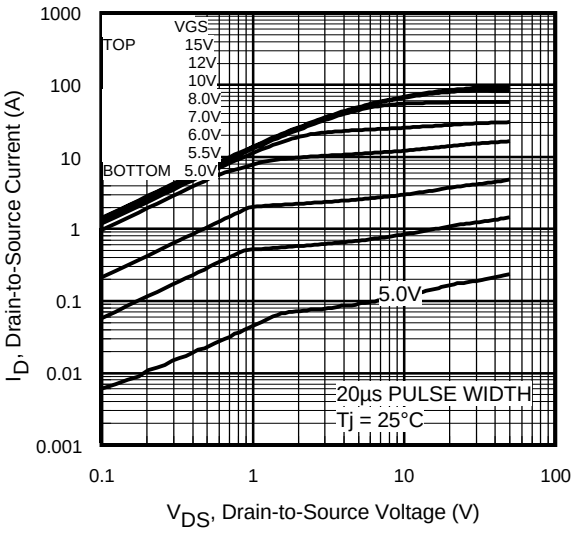



**Fig 1.** Typical Output Characteristics

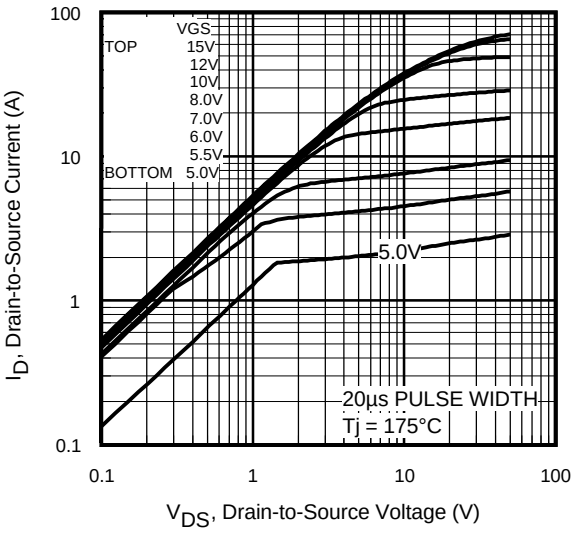



**Fig 2.** Typical Output Characteristics

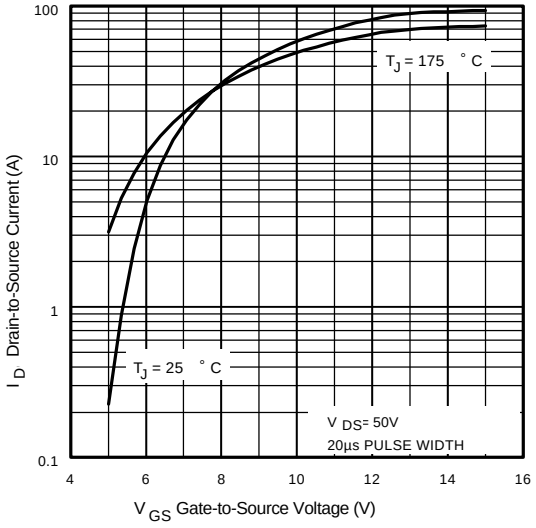



**Fig 3.** Typical Transfer Characteristics

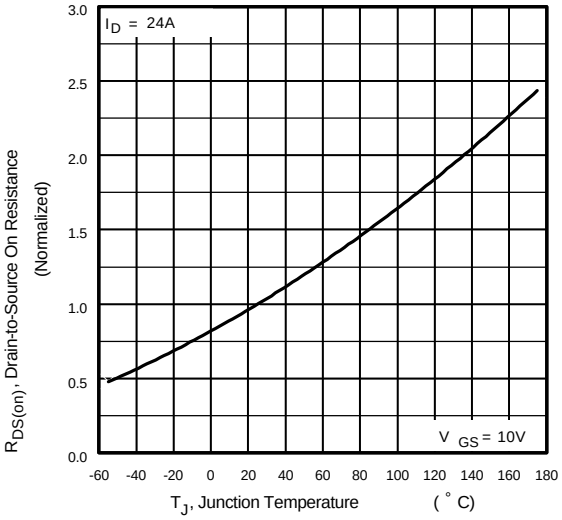



**Fig 4.** Normalized On-Resistance Vs. Temperature

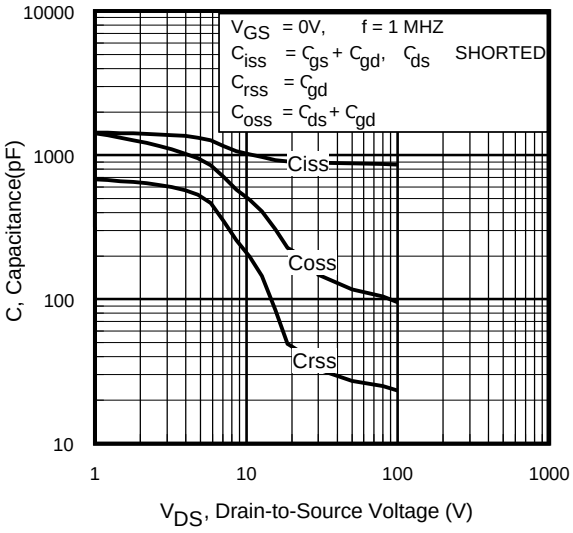



**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

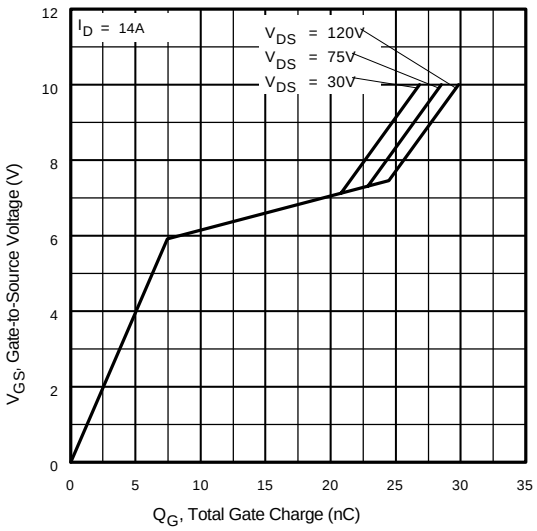



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

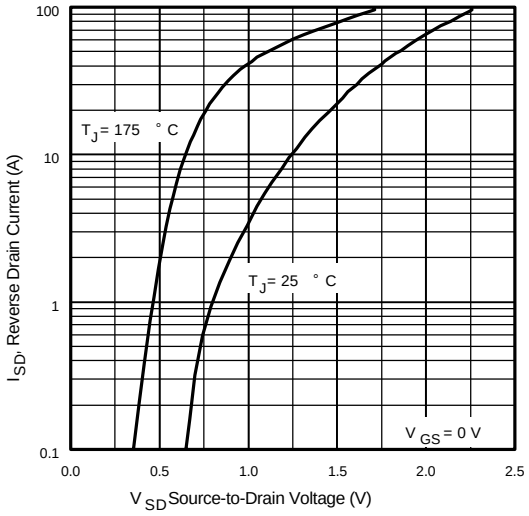



**Fig 7.** Typical Source-Drain Diode Forward Voltage

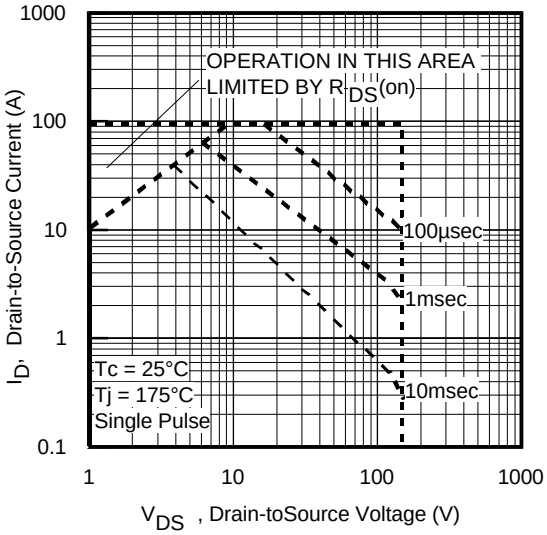



**Fig 8.** Maximum Safe Operating Area

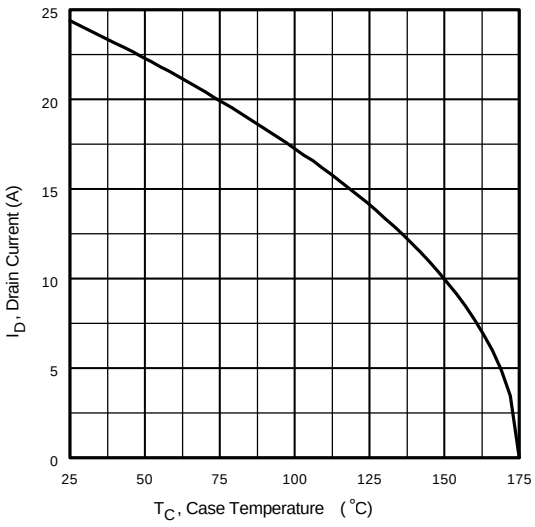



**Fig 9.** Maximum Drain Current Vs. Case Temperature

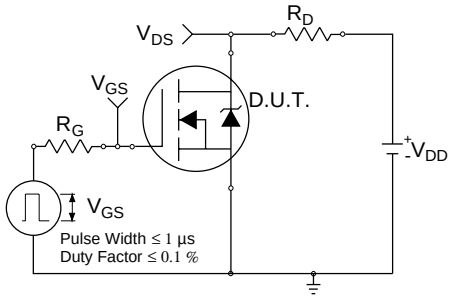



**Fig 10a.** Switching Time Test Circuit

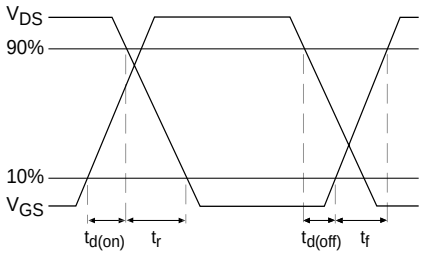



**Fig 10b.** Switching Time Waveforms

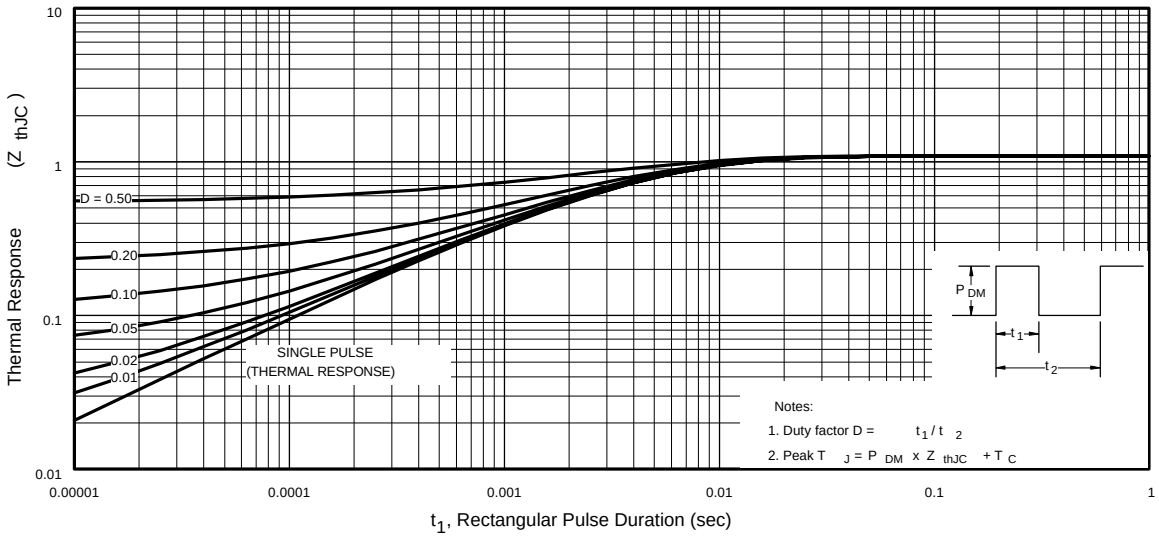



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

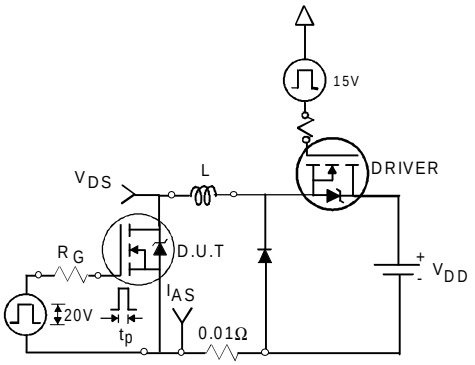



**Fig 12a.** Unclamped Inductive Test Circuit

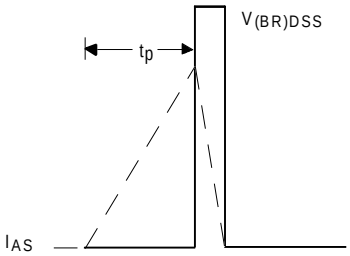



**Fig 12b.** Unclamped Inductive Waveforms

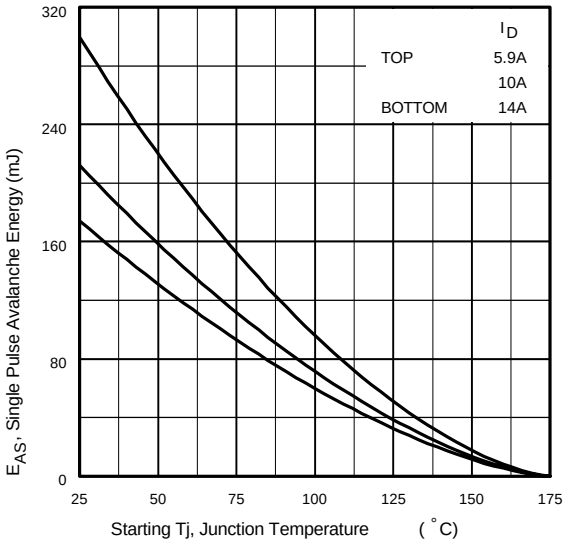



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

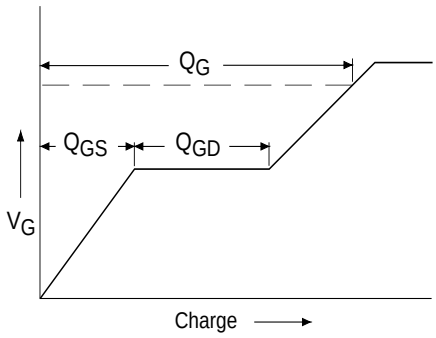



**Fig 13a.** Basic Gate Charge Waveform

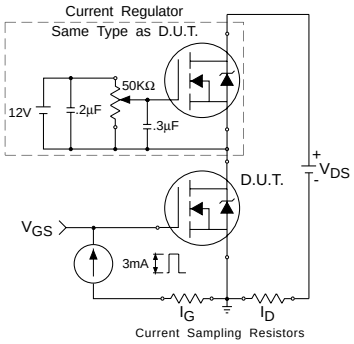
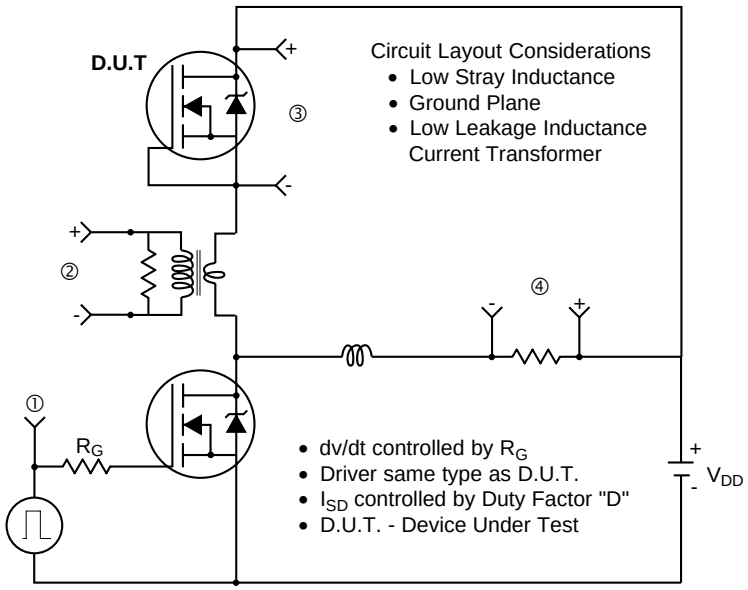
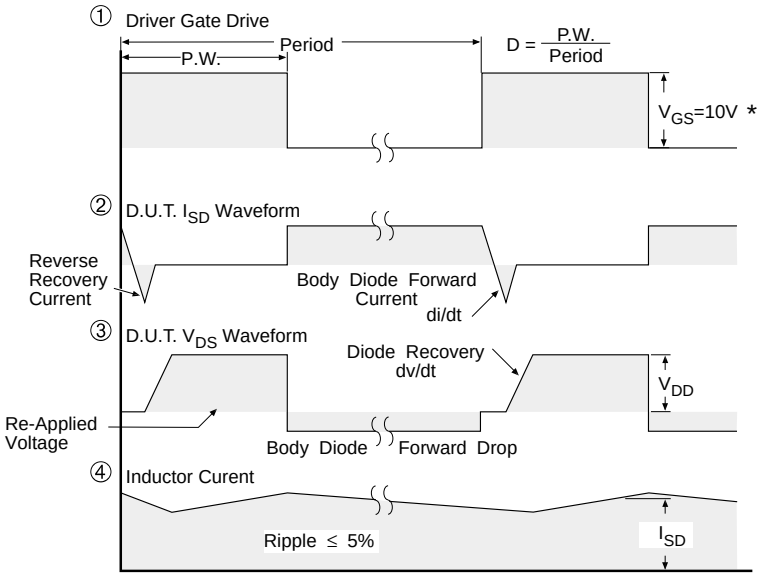



**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



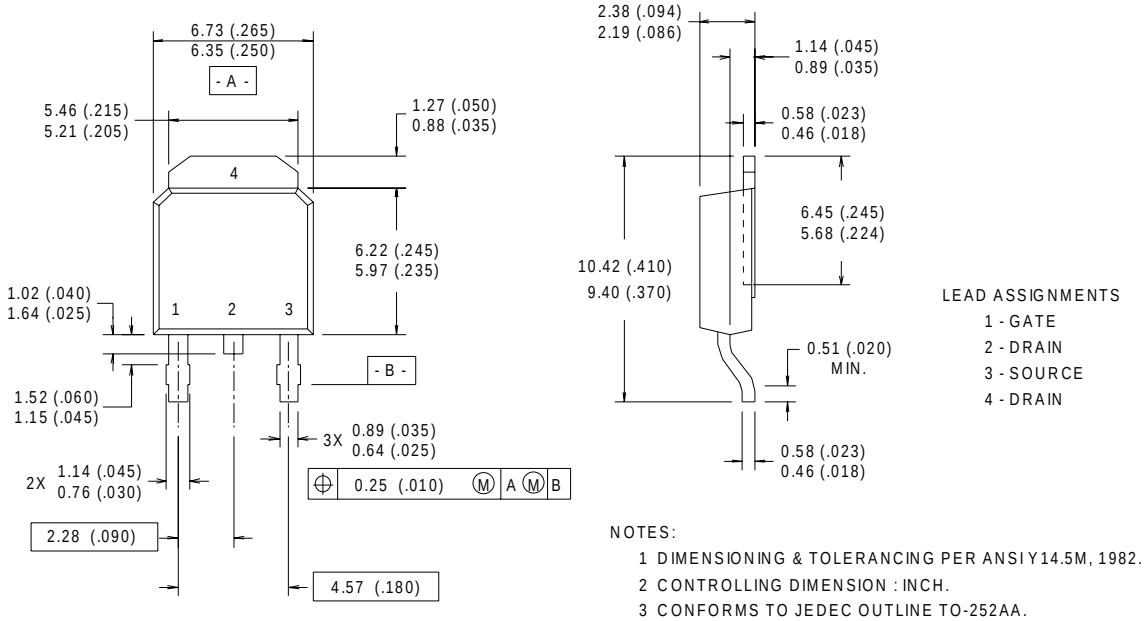




* $V_{GS}$ = 5V for Logic Level Devices

**Fig 14.** For N-Channel HEXFET® Power MOSFETs

## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)

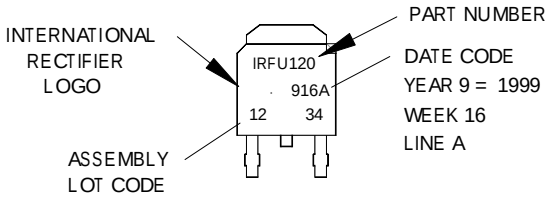



LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

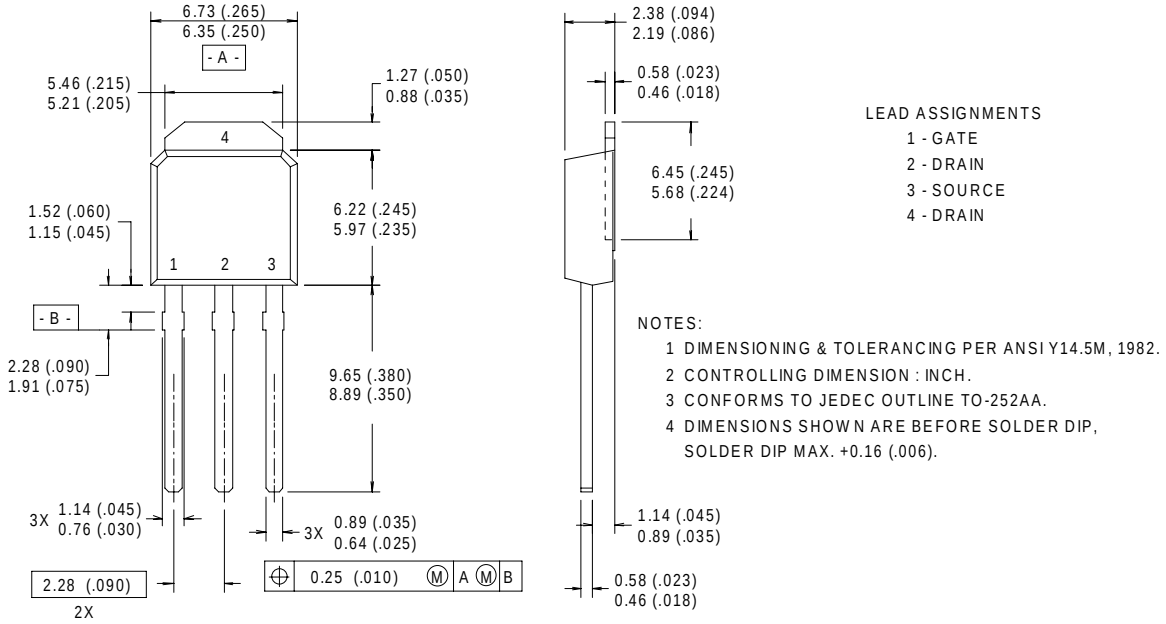
## D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"



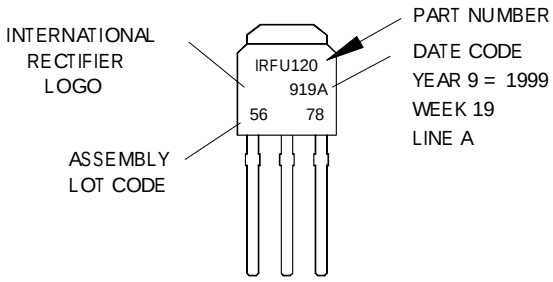
## I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



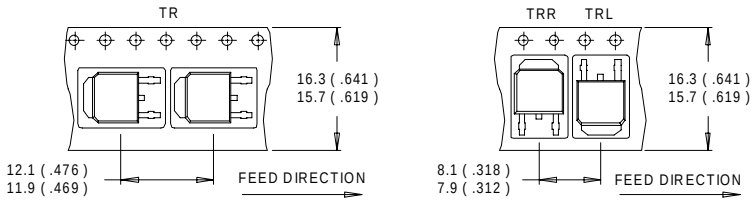

## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 1999
IN THE ASSEMBLY LINE "A"

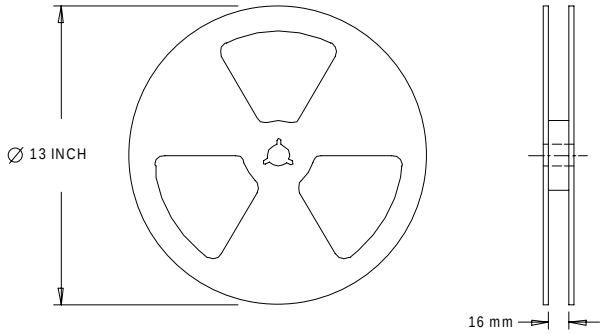


## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)




NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.




NOTES :
1. OUTLINE CONFORMS TO EIA-481.

**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting $T_J$ = 25°C, L = 1.7mH $R_G$ = 25Ω, $I_{AS}$ = 14A.

③ $I_{SD} \leq$ 14A, di/dt ≤ 380A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C.

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ $C_{oss}$ eff. is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.