

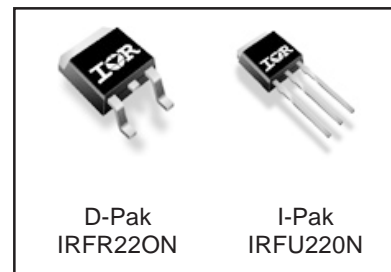
**Applications**

- High frequency DC-DC converters

$V_{DSS}$	$R_{DS(on)}$ max (mΩ)	$I_D$
200V	600	5.0A

**Benefits**

- Low Gate to Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective  $C_{OSS}$  to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	5.0	A
$I_D$ @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	3.5	
$I_{DM}$	Pulsed Drain Current ①	20	
$P_D$ @ $T_C = 25^\circ\text{C}$	Power Dissipation	43	W
	Linear Derating Factor	0.71	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ③	7.5	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

**Typical SMPS Topologies**

- Telecom 48V input Forward Converters

Notes ① through ⑤ are on page 10

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# IRFR/U220N

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## Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	200	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.23	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA ④
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	600	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 2.9A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> = 200V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 160V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V

## Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	2.6	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 2.9A
Q <sub>g</sub>	Total Gate Charge	—	15	23	nC	I <sub>D</sub> = 2.9A
Q <sub>gs</sub>	Gate-to-Source Charge	—	2.4	3.6		V <sub>DS</sub> = 160V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	6.1	9.2		V <sub>GS</sub> = 10V,
t <sub>d(on)</sub>	Turn-On Delay Time	—	6.4	—	ns	V <sub>DD</sub> = 100V
t <sub>r</sub>	Rise Time	—	11	—		I <sub>D</sub> = 2.9A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	20	—		R <sub>G</sub> = 24Ω
t <sub>f</sub>	Fall Time	—	12	—		V <sub>GS</sub> = 10V ④
C <sub>iss</sub>	Input Capacitance	—	300	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	53	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	15	—		f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	300	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 1.0V, f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	23	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 160V, f = 1.0MHz
C <sub>oss eff.</sub>	Effective Output Capacitance	—	46	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 160V ⑤

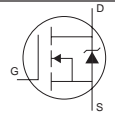
## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy②	—	46	mJ
I <sub>AR</sub>	Avalanche Current①	—	2.9	A
E <sub>AR</sub>	Repetitive Avalanche Energy①	—	4.3	mJ

## Thermal Resistance

	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	—	3.5	°C/W
R <sub>θJA</sub>	Junction-to-Ambient (PCB mount)*	—	50	
R <sub>θJA</sub>	Junction-to-Ambient	—	110	

## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	5.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	20		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 2.9A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	90	140	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 2.9A
Q <sub>rr</sub>	Reverse Recovery Charge	—	320	480	nC	di/dt = 100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

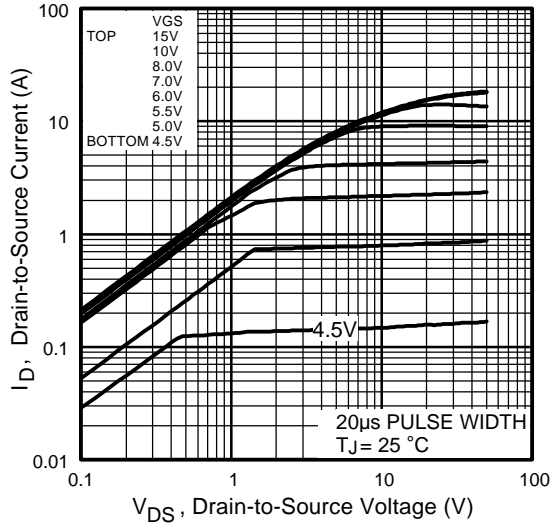


Fig 1. Typical Output Characteristics

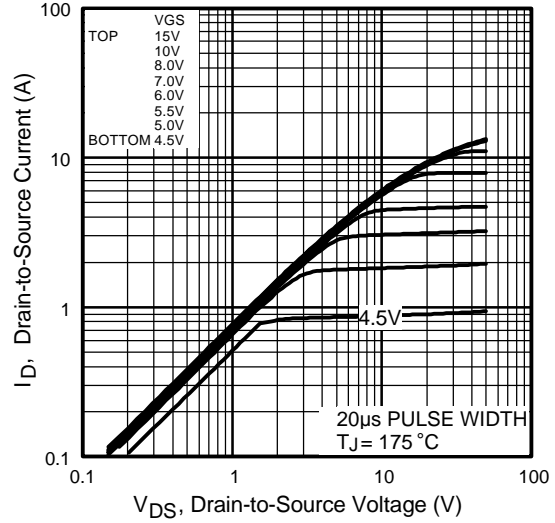


Fig 2. Typical Output Characteristics

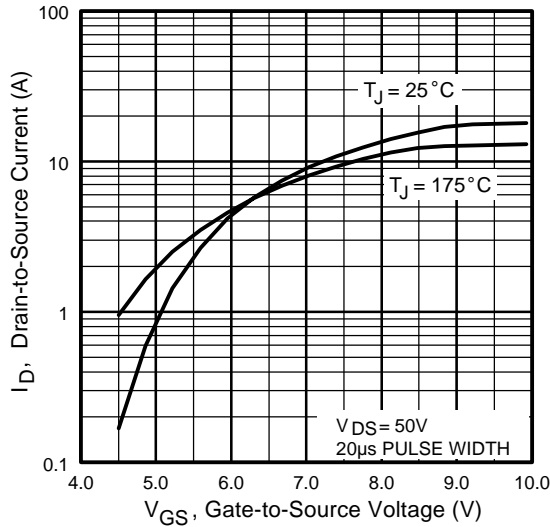


Fig 3. Typical Transfer Characteristics

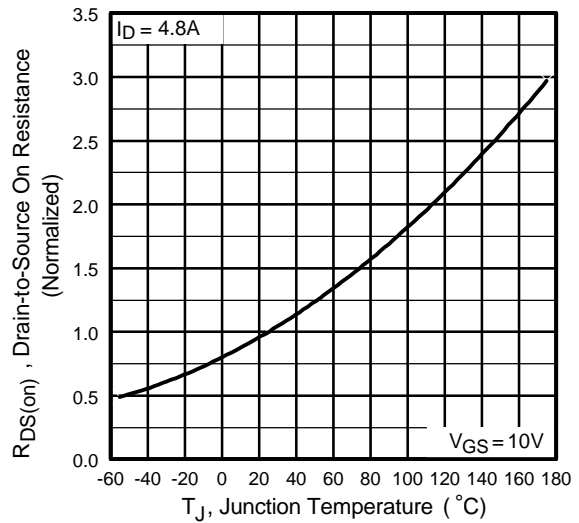
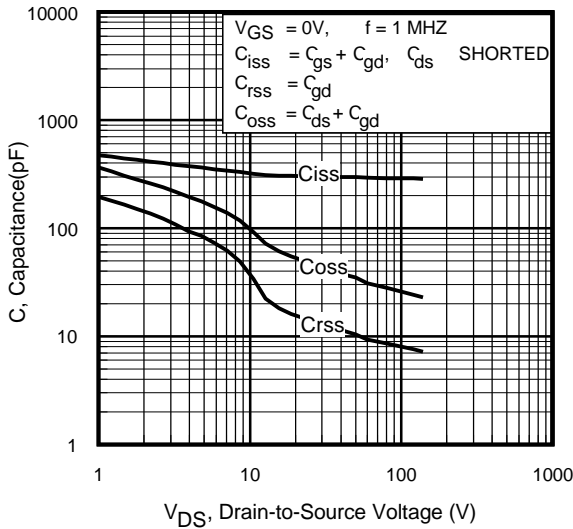
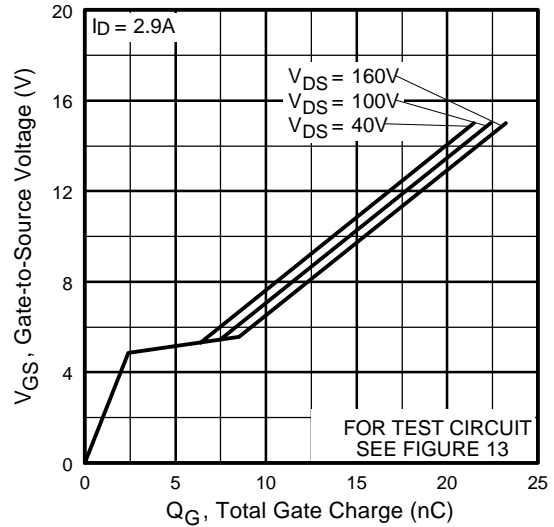


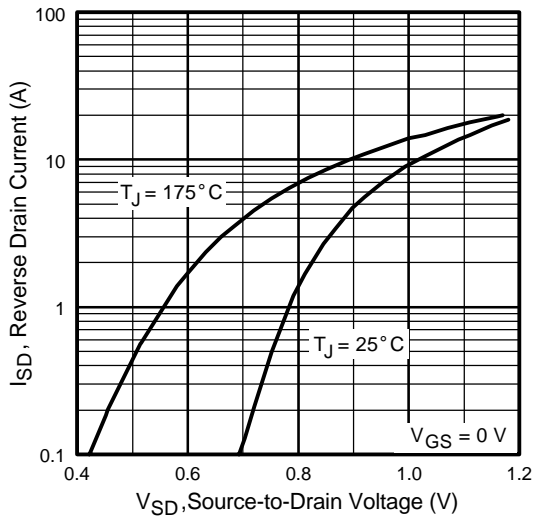
Fig 4. Normalized On-Resistance Vs. Temperature



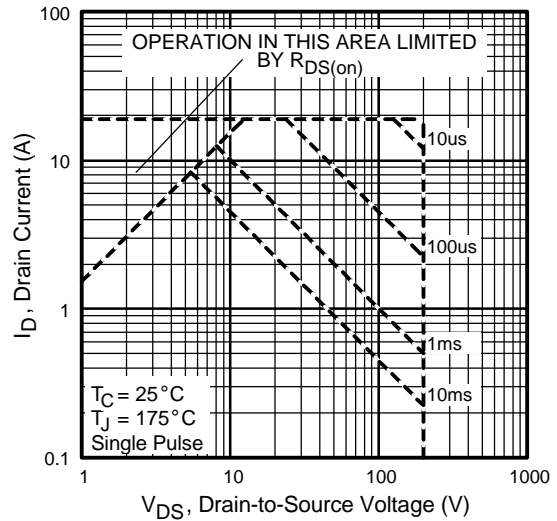
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



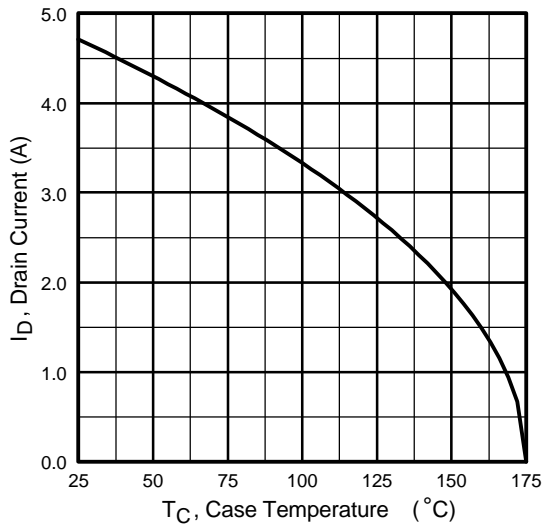
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



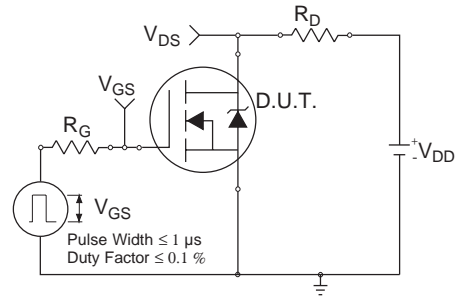
**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area



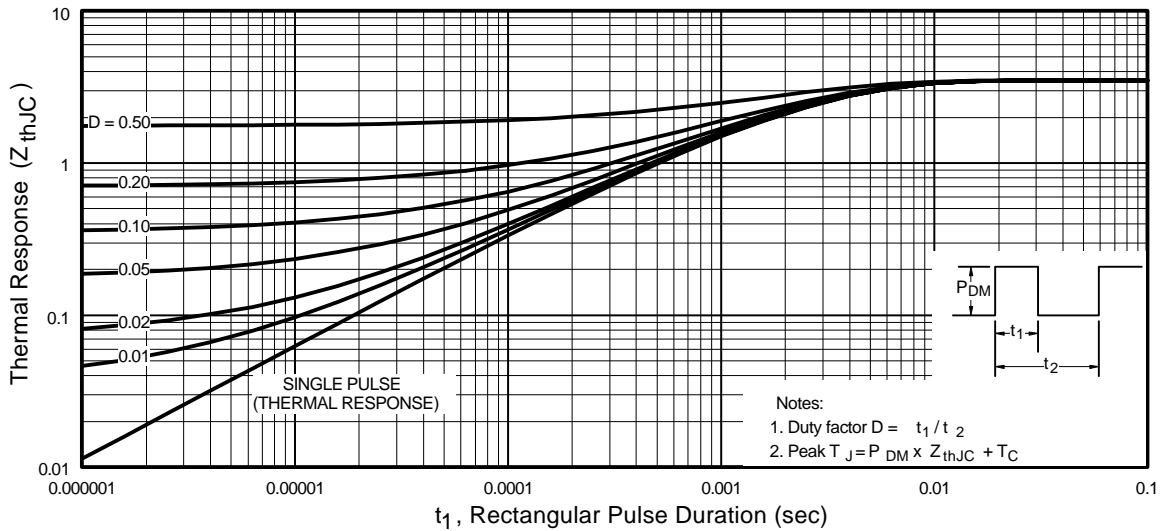
**Fig 9.** Maximum Drain Current Vs. Case Temperature



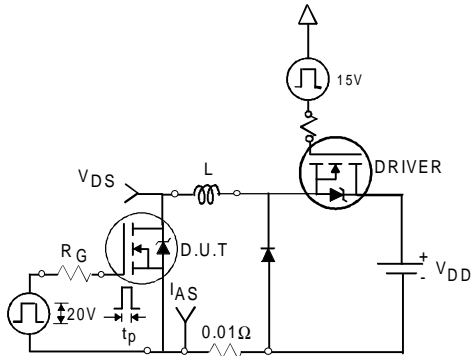
**Fig 10a.** Switching Time Test Circuit



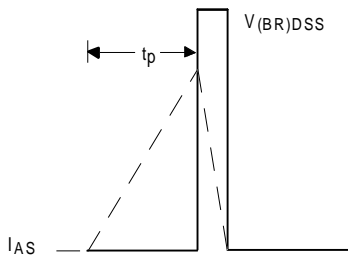
**Fig 10b.** Switching Time Waveforms



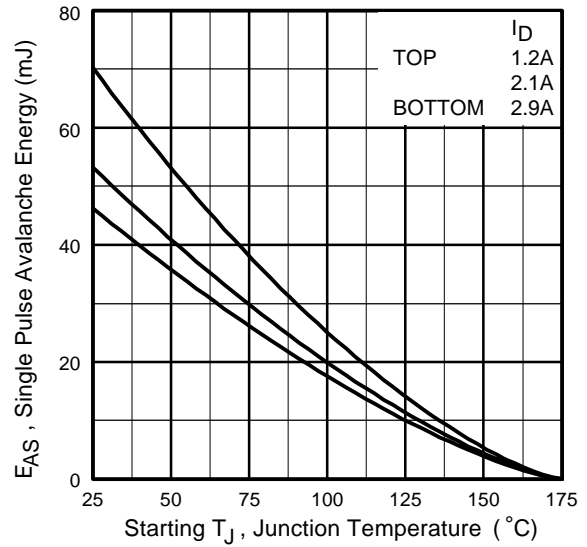
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



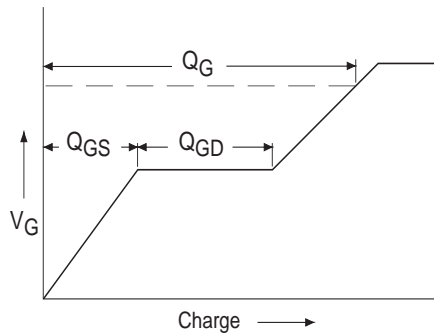
**Fig 12a.** Unclamped Inductive Test Circuit



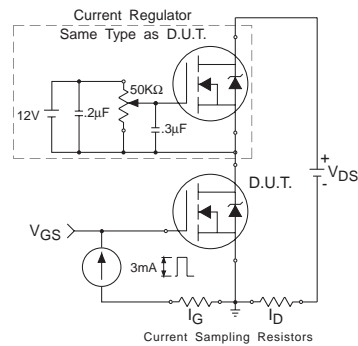
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

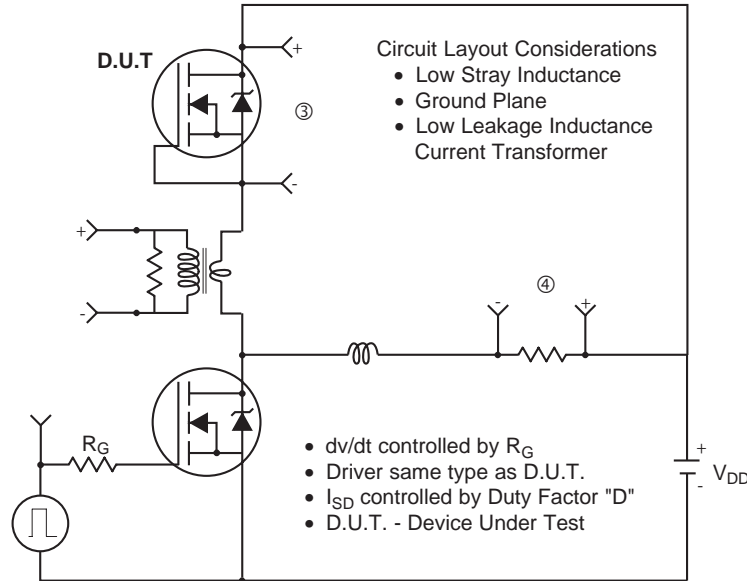


**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

**Peak Diode Recovery dv/dt Test Circuit**



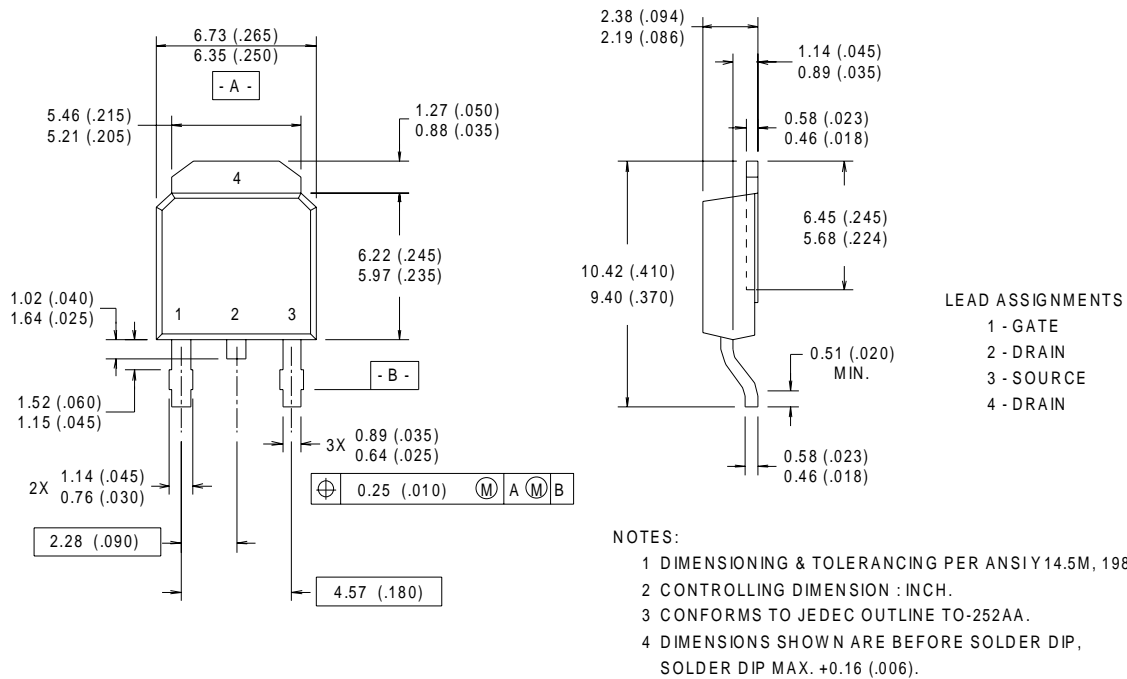
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFET® Power MOSFETs

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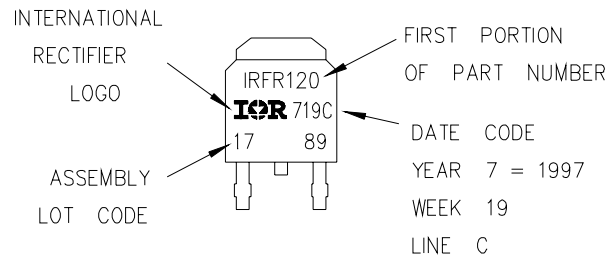
## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



## D-Pak (TO-252AA) Part Marking Information

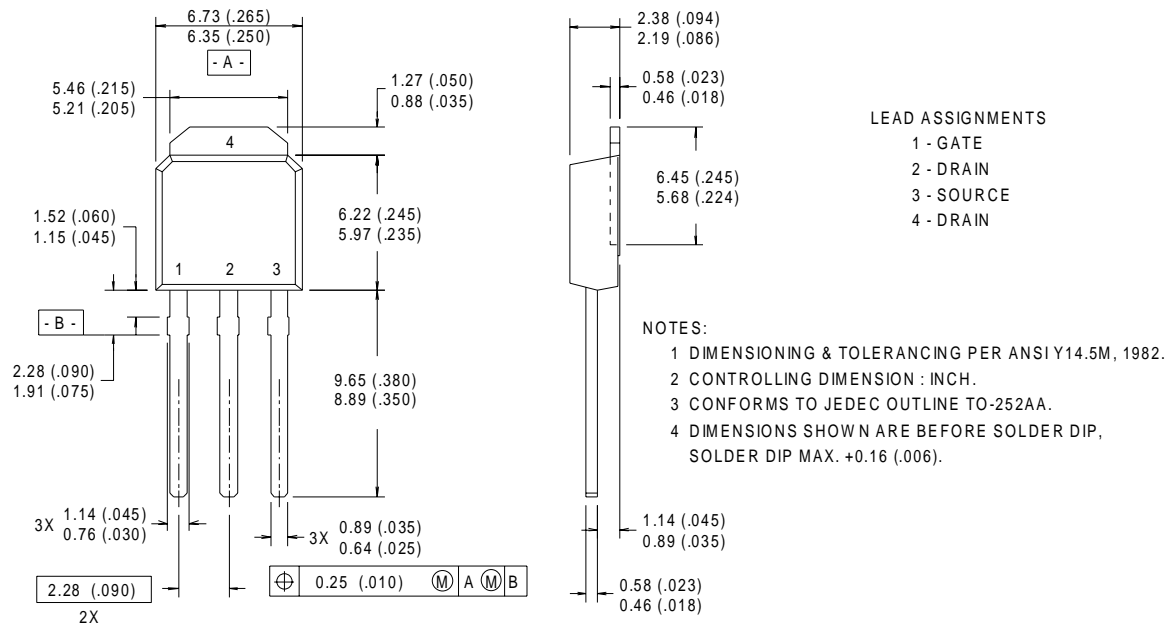
EXAMPLE: THIS IS AN IRFR120  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"





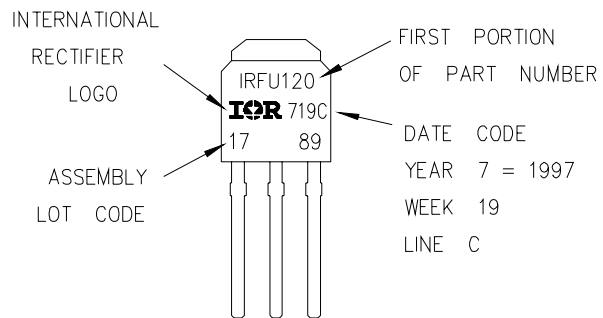
## I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"

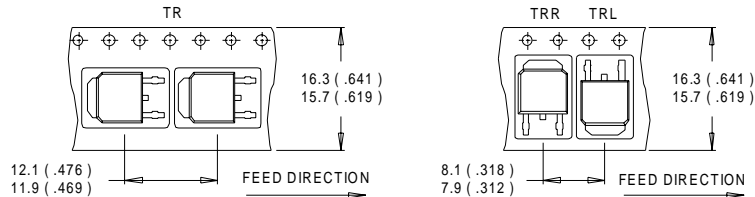


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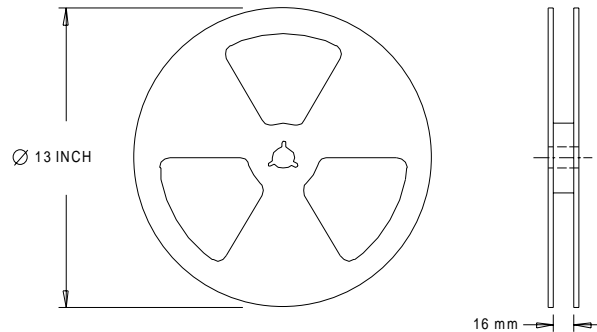
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## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
  2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
  3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. OUTLINE CONFORMS TO EIA-481.

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
  - ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 11\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 2.9\text{A}$ .
  - ③  $I_{SD} \leq 2.9\text{A}$ ,  $di/dt \leq 320\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 175^\circ\text{C}$
  - ④ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
  - ⑤  $C_{oss}$  eff. is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- \* When mounted on 1" square PCB (FR-4 or G-10 Material).  
For recommended footprint and soldering techniques refer to application note #AN-994.

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